Multimodal Portable Functional Brain Imaging Chip

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Abstract **- Near-infrared spectroscopy is a non-invasive technology that uses source-detector pairs for measuring bio-signals such as hemodynamics. Continuous-wave near-infrared spectroscopy(CWNIRS) was widely used for signal measurement due to its simple implementation and system portability. However, this method is not suitable for absolute optical property measurement which is critical to deriving accurate tissue property. Frequency-domain NIRS(FDNIRS) and time-domain NIRS(TDNIRS) are solutions for this problem. FDNIRS operates at high speed compared with CWNIRS, which increases its hardware complexity. To solve the system bulkiness, an integrated circuit system design was implemented for FDNIRS. Fabricated FDNIRS IC used a delay-locked loop (DLL) and a low sampling rate analog-to-digital converter (ADC) to extract amplitude and phase delay information of the NIRS signal. IC system realizes a portable, real-time measurement system.**

Keywords**—DLL, FDNIRS, Near-infrared spectroscopy**

I. INTRODUCTION

Near-Infrared Spectroscopy (NIRS) is a technology for measuring bio-signal by injecting near-infrared light into our bodies. A typical application for NIRS is hemodynamics measurement, where it is a change in oxygen saturation in brain blood resulting from neuron activation. NIRS measurement system consists of a near-infrared source and a detector pair. Typical NIRS sources use a laser emitter and a photodiode for a detector. Compared with other systems which can measure brain activities such as MRI, NIRS has strength in portability and shorter time resolution. Spatial resolution can be enhanced by implementing more source-detector channels. Also, its non-invasive measurement allows convenient signal measurement.

The primary goal of NIRS measurement is to reconstruct a bio-signal from the human body based on measuring the optical property of tissue. There are two optical properties measured in NIRS. Each definition is based on the physical movement of injected photons from the laser source inside the tissue. The absorption coefficient (μ_a) indicates the absorption probability of a photon per unit length. Not all photons can reach the detector. Photons can be absorbed by human tissue, and the amount of absorption depends on the physical property of the tissue. The scattering coefficient (μ_s') specifies the scattering probability of a photon per unit length. Similar to photon absorption, a photon can scatter through human tissue depending on tissue property. In other words, human tissue has measurable optical properties, and NIRS enables the calculation of these characteristics. There are three different ways of measuring these properties: continuous-wave NIRS (CWNIRS), frequency-domain NIRS (FDNIRS), and time-domain NIRS (TDNIRS). The principle of each method is depicted in Fig. 1. [1]

Among three different NIRS techniques, continuous-wave NIRS (CWNIRS) is most commonly utilized due to its simple implementation. In CWNIRS, a laser source with constant intensity is injected into the human tissue. A photodetector detects the reflected signal intensity. Relative optical property can be extracted by measuring the difference in signal intensity by applying Modified Beer-Lambert's Law (MBLL). Before MBLL calculation, optical density is measured by following equations (1) and (2). [2] I and I_0 denote measured light density detected from RX and initial light density injected through TX, respectively. DP stands for photon diffuse pathlength. OD is optical density and λ_1 stands for a wavelength of light.

$$I = I_0 e^{-\mu_a \times DP} \tag{1}$$

$$OD^{\lambda_1} = -\ln \frac{I(\lambda_1)}{I_0(\lambda_1)} \tag{2}$$

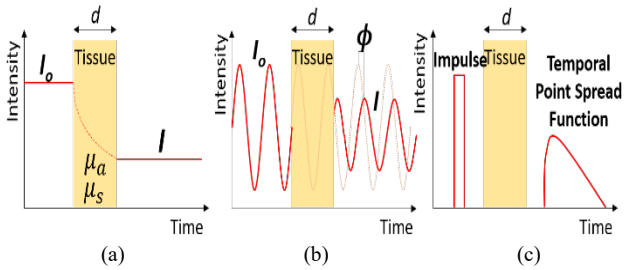

Fig. 1. Three different methods of NIRS; (a) CWNIRS measures difference of intensity (b) FDNIRS method measures both intensity and phase delay information (c)TDNIRS method is based on measuring impulse response of laser

Unlike CWNIRS technique, frequency-domain NIRS (FDNIRS) and time-domain NIRS (TDNIRS) techniques can extract absolute optical properties. As shown in Fig. 1(b), FDNIRS measures phase delay with amplitude change. Regarding the fact that CWNIRS only measures amplitude

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change, FDNIRS obtains two variables: amplitude (I) and phase delay (ϕ).[3]

$$\phi \propto -\left(\frac{(\mu_e c)^2+\omega^2}{\mu_s^{`2}}\right) \times sin(tan^{-1}\left(\frac{\omega}{2\times\mu_e c}\right)) \quad (3)$$

$$I \propto exp(-d \times \mu_a \times \mu_s') \quad (4)$$

Equation (3) shows the relationship between absolute optical property and phase delay. Similarly, equation (4) indicates the correlation between absolute optical property and amplitude. In (3), c stands for the speed of light. Both absorption coefficient and scattering coefficient can be obtained by solving equations (3) and (4). The signal injected from the source must obtain frequency information for measurement. Signal around 100MHz is typical for this application. 100MHz is equal to 10ns photon delay in the time domain. Since it is known that photon travels inside the human tissue no longer than 10ns, this is a reasonable region for target measurement.

Although FDNIRS system dominates CWNIRS technique from the perspective of absolute optical property extraction, FDNIRS techniques are not widely utilized. The main reason is system bulkiness. The fundamental problem comes from the signal-to-noise ratio (SNR) limitation issue. This can be clarified through a relationship between photodiode sensitivity and bandwidth trade-off. Junction capacitance (C_j) of the photodiode can be written as shown in equation (5):

$$C_j = \frac{\epsilon_{Si}\epsilon_0 A}{W_d} \quad (5)$$

$$W_d = \sqrt{2\epsilon_{Si}\epsilon_0\mu\rho(V_A + V_{bi})} \quad (6)$$

$$f_{3dB} \propto \frac{1}{RC_j} \quad (7)$$

Where depletion depth W_d is shown in equation (6). In equations (5) ~ (7), ϵ_o stands for permittivity of free space, ϵ_{Si} is permittivity of silicon, A is area of capacitor plate, V_A is early voltage, V_{bi} is built-in potential barrier, μ stands for permeability, and ρ stands for resistivity. As demonstrated in equation (7), photodiode bandwidth $f_{3dB}$is inversely proportional to the capacitance and resistance of the photodiode. To obtain high-speed operation which is required in FDNIRS, the photodiode must have smaller junction capacitance assuming the same resistance. However, the effective area of the photodiode must be small for this requirement. Another option would be applying a higher bias voltage. A smaller effective area means lower sensitivity of the photodiode. This is why conventional FDNIRS systems had to be bulky.

For the conventional FDNIRS system, avalanche photodiode (APD) was utilized for higher sensitivity [4]. APD implementation also needs bulky fiber optics, long calibration time, and high voltage operation near 100 volts. The single APD module itself needs a built-in printed circuit board (PCB) system. Without integrated circuit technology, the designer must implement custom blocks for front-end detection on PCB. To overcome these issues, this research proposed an integrated circuit design to solve the system bulkiness of the FDNIRS system. To be more specific, the FDNIRS system used a photodiode instead of APD. Systematic efforts to overcome SNR limitations will be discussed in part II. Also, a delay-locked-loop (DLL) was implemented for synchronous phase delay measurement. Discussions will be focused on the design strategy of the integrated circuit (IC). A deeper investigation of the conventional FDNIRS system will be shown and IC design will show how to solve existing problems.

II. EXPERIMENTS

A. Conventional FDNIRS Design

As mentioned before, conventional FDNIRS devices predominantly utilized avalanche photodiode fiber optics. Since integrated circuit design did not apply in this field, engineers used printed circuit board (PCB) design. Fig. 2 shows the block diagram of a traditional FDNIRS device.

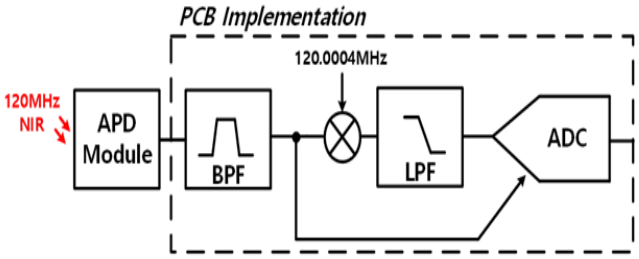
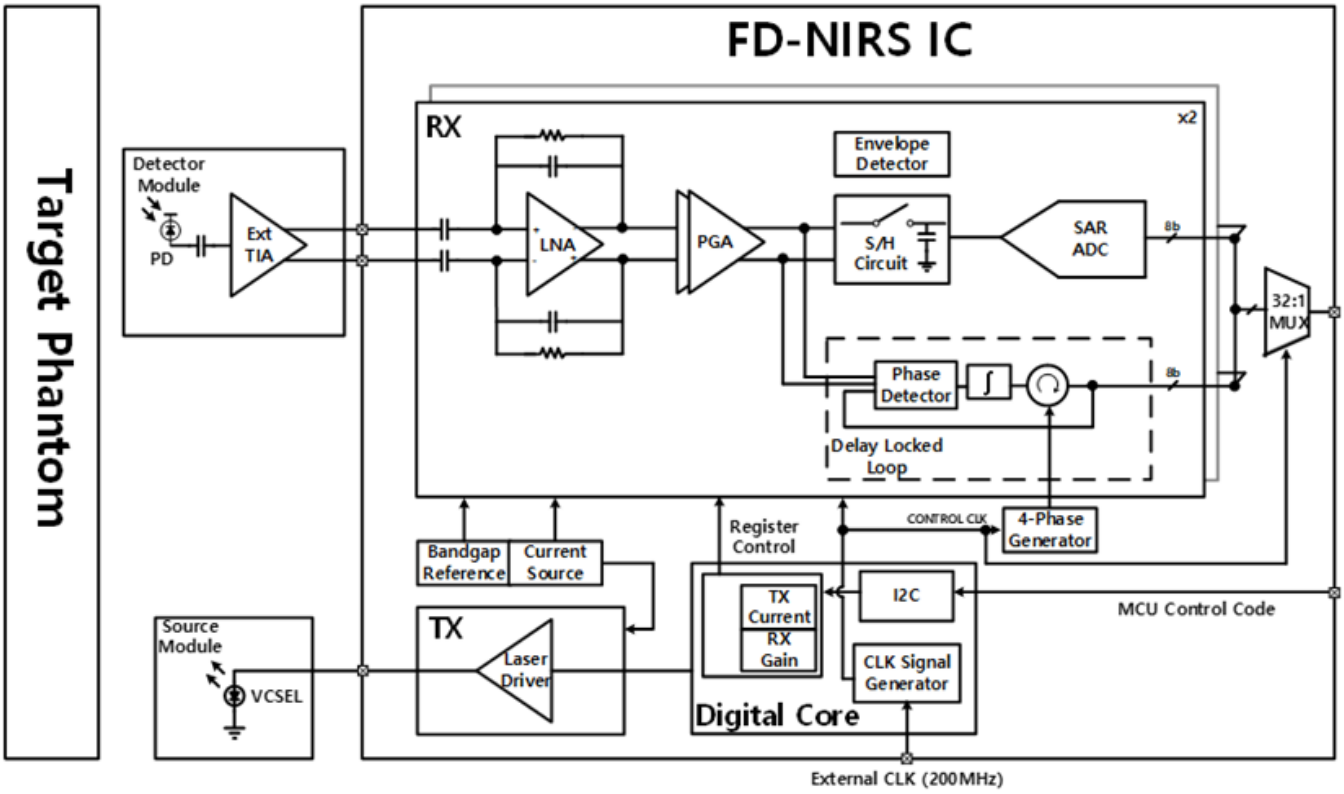


Fig. 2. Conventional FDNIRS measurement unit

As shown in Fig. 2, PCB module design is implemented in multiple components. After a signal is received through the APD module, the band-pass filter (BPF) filters signals near 120 MHz. After BPF, the signal travels through two different paths. One directly passes an analog-to-digital converter (ADC) for amplitude measurement. The other signal passes through a mixer. This signal is multiplied by 120.0004 MHz signal to extract the phase component of the signal. By applying a low-pass filter, we can only get the phase component by rejecting the high-frequency signal. Some applications do not implement mixers for phase delay extraction. Instead, a high sampling rate ADC was utilized [5]. In this method, the main idea is to process the analog waveform itself to the digital signal processing core. This method extracts phase delay information asynchronously. Also, high sampling rate ADC implementation requires more hardware complexity.

The main controversies in conventional FDNIRS design are as follows. First is the APD front-end module. APD module needs high voltage operation of more than 100 volts due to its operation principle. By implementing a small-size photodiode, we can reduce this hardware complexity, but SNR will be the main issue. The second issue is amplitude extraction through ADC. As mentioned before, we need a high sampling rate ADC for amplitude extraction in the previous method. More ideas can be applied to reduce the sampling rate. Finally, there are more contribution points to extracting phase delay information synchronously by implementing a delay-locked loop (DLL).



B. Proposed FDNIRS Design

Fig. 3 shows the overall functional block diagram of the proposed system. Off-chip of the system consists of a small-size photodiode, SAW filter, and trans-impedance amplifier (TIA) at the receiver and vertical cavity surface emitting laser (VCSEL) at the transmitter. Source and detector pair are directly attached to human skin for hemodynamics measurement.

The signal from the source directly enters the RX block. The RX front-end includes a low-noise amplifier (LNA) and a two-stage programmable gain amplifier (PGA). LNA is implemented for signal rejection of unwanted range. PGA is controlled by off-chip control bits to obtain variable gain according to target measurement. The waveform at PGA output propagates to a track-and-hold circuit for amplitude measurement and DLL for phase delay measurement. Track-and-hold circuit is needed for peak sampling, and sampled signal passes an 8-bit successive approximation analog-to-digital converter (SAR ADC). For phase delay measurement, 8-bit DLL is implemented. DLL consists of the phase detector, digital integrator, and phase interpolator. Total signals from ADC and DLL are accumulated through a 32:1 multiplexer (MUX).

An on-chip TX laser driver drives VCSEL, where a digital core controls the TX laser driver. The digital core is a critical block for overall chip control. An external control signal for the chip is a clock signal and micro-controller unit (MCU). The clock signal generator inside the digital core handles the clock signal for DLL phase delay measurement and SAR ADC timing control. MCU coded control signal is stored in the I2C register control unit. These control signals are critical for switches implemented on-chip. Bandgap reference (BGR) and current source are also designed for the overall current and voltage supply on chip.

The chip was processed in TSMC 0.18um 1P6M CMOS process. The die size is 5mm by 5mm. RX core supply was 1.8V, and TX driver supply was 3.3V. The detailed specification of the chip is organized in table I

TABLE I. FDNIRS IC chip specification

RX	Gain control range	32dB ~ 85dB
	Input referred noise (@ 100MHz)	21nV/√Hz
	3dB bandwidth	150MHz
	ADC resolution	8-bit SAR ADC
TX	Driving current	5mA ~ 25mA

C. FDNIRS Receiver Design

RX front-end block of FDNIRS IC consists of LNA and PGA. LNA rejects signal range out of 100MHz. Although an off-chip SAW filter was implemented for SNR enhancement, on-chip LNA is necessary for additional noise optimization. PGA is implemented for additional gain enhancement. Fig. 4 shows the overall RX block design.

External TIA has 74dB gain, LNA was designed with 20dB gain, and PGA was designed with 6 to 30dB gain each. Two-stage PGA was implemented for higher gain. For LNA design, a capacitive feedback structure was chosen. Most bio-signal detection adapts capacitive feedback structure for high input impedance and low input-referred noise.

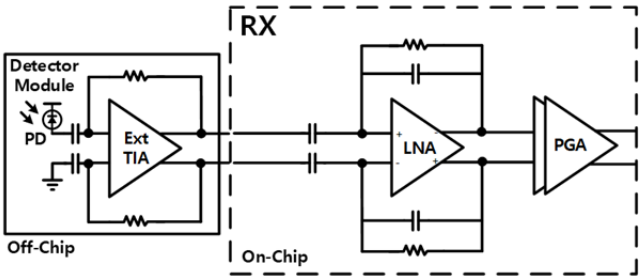


Fig. 4. Analog Front-End of FDNIRS IC

Fig. 5 shows a single LNA block diagram. In a capacitive feedback structure, a resistor in the feedback path is necessary for the DC bias path. DC level will not be determined without this resistance. However, in typical biomedical front-end design, a large value of resistance is used to minimize the low cut-off frequency. When investigating the low cut-off frequency of bandpass filter structure, large resistance leads to low cut-off frequency. Bio-signal is often dealt with under 1Hz frequency. To meet this requirement, some applications use resistance higher than 1G-ohm. There are circuit techniques to overcome this issue, but this case does not deal with high on-chip resistance. The proposed system deals with signals above 50MHz, so on-chip poly-silicon resistance is enough. As shown in Fig. 5, the proposed system implemented 100k-ohm resistance for resistance in the LNA feedback path

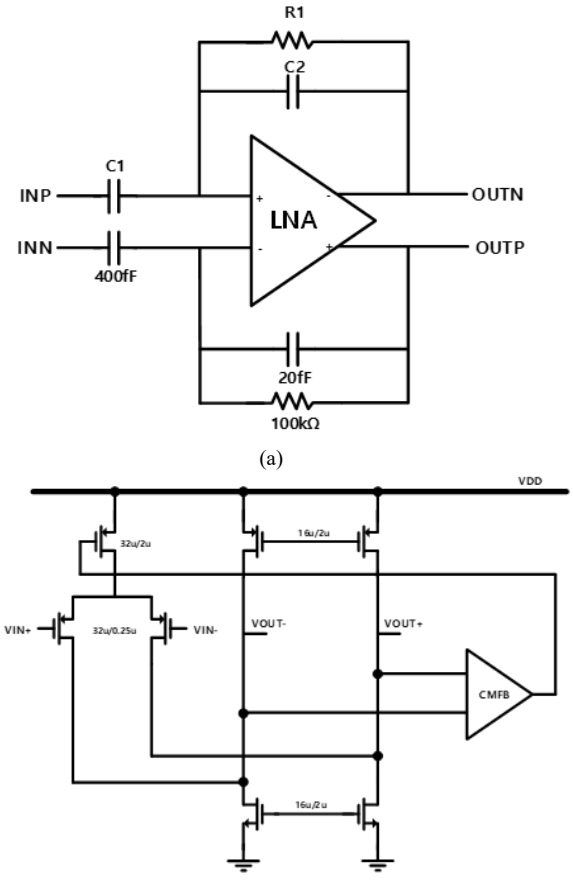
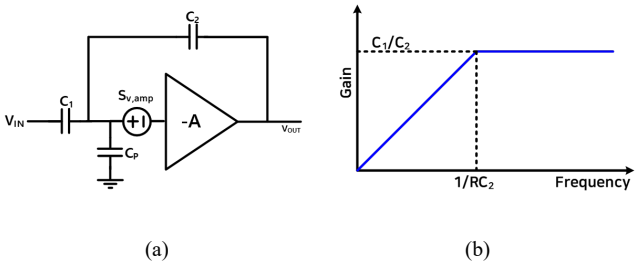


Fig. 5. LNA design of FDNIRS IC; (a) LNA with feedback structure (b) LNA amplifier core design



(a) (b)

Fig. 6. Noise source analysis of capacitive feedback amplifier; (a) Noise source of amplifier (b) Low frequency Bode plot of LNA

Fig. 6(a) shows a capacitive feedback amplifier structure with a noise source $S_{v,amp}$, and parasitic capacitance C_p. Signal gain can be written as equation (8) and noise gain can be written as (9). two equations show that a large enough input capacitance, which is C_1 in Fig. 6(a), is needed for low input-referred noise and high SNR.

$$A_{sig} = -\frac{C_1}{C_2} \tag{8}$$

$$A_{noise} = -\frac{C_1+C_2+C_p}{C_2} \tag{9}$$

High-frequency thermal noise is dominant in the FDNIRS system. For typical biomedical circuit applications, low-frequency flicker noise is dominant, but this is not the case. Thus, the input capacitance of 400fF was enough for the proposed system design regarding chip area and overall noise level.

Fig. 5(b) shows the core design of the LNA block. The core block utilized typical PMOS folded cascode structure. PMOS folded cascode structure was chosen for the high DC level of the input common-mode range. A large PMOS width-to-length ratio design strategy was utilized for lower thermal noise. Closed-loop gain of the LNA was 18dB at 100MHz frequency. The phase margin of the core design was 74° which is stable enough for the operation. 3dB passband of the LNA was 40MHz to 150MHz.

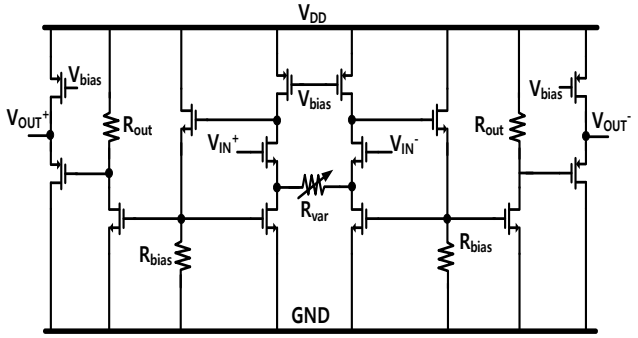


Fig. 7. Schematic of PGA core design

Unlike typical PGA design, the proposed PGA was designed in an open-loop structure for higher gain [6]. This strategy was inevitable to meet the SNR condition resulting from low photodiode sensitivity. The feedback structure of the amplifier does not guarantee the wanted gain level. The

voltage bias circuit was designed for constant common mode voltage. The overall gain of the PGA is controlled by the variable resistor implemented at the source of PGA input. While R_{out} remains at 40k-ohm, the value of the variable resistor varies from 1k-ohm to 16k-ohm. This results in the gain range of 8dB to 32dB. Equation (10) shows the gain calculation of the PGA.

$$A_v = -\frac{R_{out}}{R_{var}} \tag{10}$$

Fig. 8 shows the functional block diagram of DLL[7]. DLL consists of a bang-bang phase detector[8], signal integrator, and phase interpolator. The output clock signal from the phase interpolator and zero crossing point of an input signal is matched through the loop. In other words, the phase is locked between an amplified signal, with minimum SNR of 10dB, and a phase interpolator. The integrator modulates the output phase of the phase interpolator. The comparator inside the phase detector modulates the output bit of the integrator by detecting the leading or lagging between the clock and signal phase. A four-phase generator is used for reference signal generation for both DLL and TX transmission. The phase interpolator receives a direct signal from the four-phase generator as shown in Fig. 9.

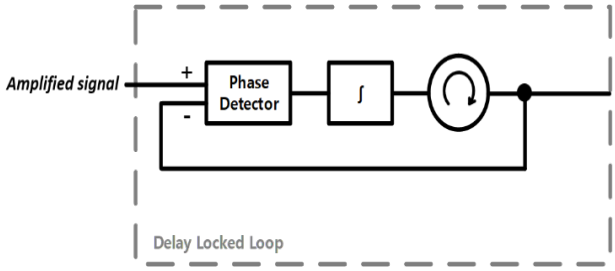


Fig. 8. Functional block diagram of delay-locked loop (DLL)

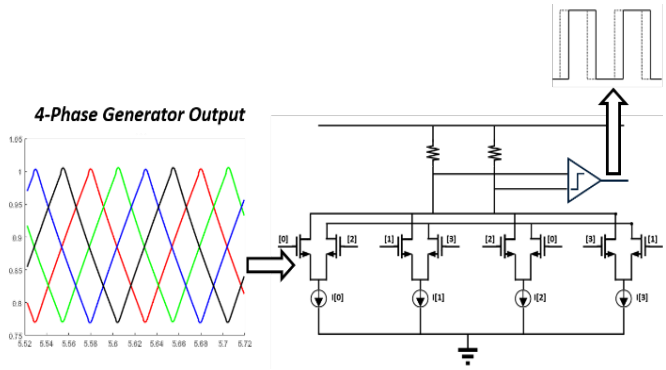


Fig. 9. Operation of phase interpolator inside the DLL block

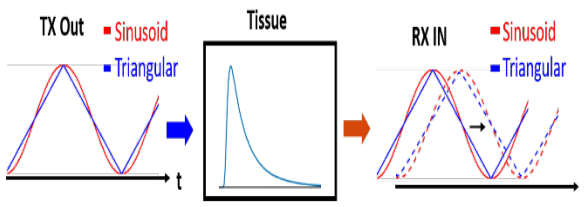


Fig. 10. Triangular waveform generation

Four-phase generator output is implemented as a triangular waveform. Typical laser transmission is generated in a sine wave. The sine wave is a single-tone waveform, so it is easy to analyze in the frequency domain. However, a complex hardware system is required for sine-wave generation. Instead, a triangular waveform was generated in the proposed design. Compared with a sine wave, a triangular waveform contains non-linearity, but it does not need a complex hardware design for implementation. When the triangular waveform is applied to human tissue, the output appears as shown in Fig. 10. Group delay can be detected, but it does not affect the overall system operation even if a triangular waveform is applied. From this triangular four-phase generator, each transistor in the phase interpolator is controlled by an 8-bit current source controller. Four phase generator originates from a 200MHz clock signal. 8-bit current control equals 1LSB at 1.4°.

D. FDNIRS Transmitter Design

TX block of the FDNIRS IC is implemented to control the off-chip vertical cavity surface emitted laser (VCSEL). The bandwidth of this device is up to 1GHz, so it is suitable for the proposed application. VCSEL is controlled by current. VCSEL has a threshold current for operation. TX laser driver must drive both threshold condition, which is the DC current level, and the actual power level of the VCSEL, which is the AC signal of the current.

Fig. 11 shows an overall schematic of the FDNIRS TX laser driver. The digital core controls the input of the laser driver. The clock generator and TX control code register are two different control blocks for TX. Clock generator is the fundamental signal generating block for both RX and TX. The four-phase generator in DLL input originates from this clock generator block. The signal from the clock generator passes the charge pump to generate a 100MHz differential triangular waveform for driving the AC signal for the transmitter. TX control code register controls the current digital-to-analog converter (IDAC) and voltage level shifter. IDAC defines DC and AC current levels for laser drivers. The source signal generated from the charge pump is combined with this control logic. Level shifter shifts 1.8V domain VDD to 3.3V. 1.8V domain is not suitable for laser current driving dynamic range.

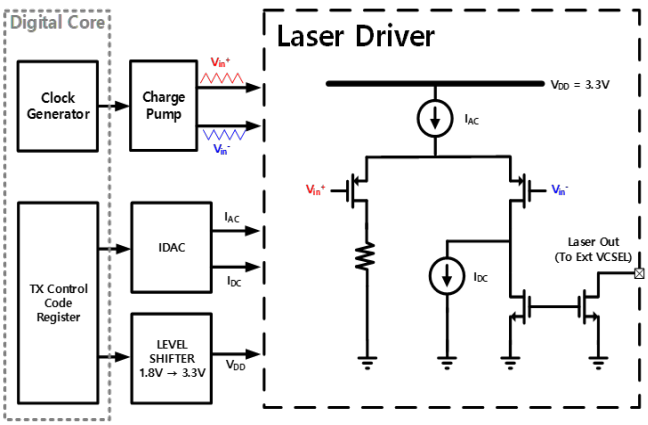
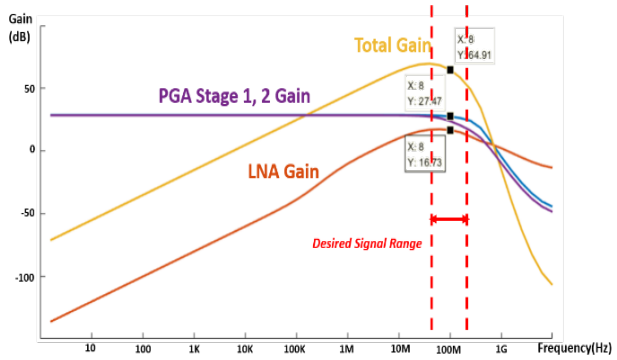


Fig. 11. FDNIRS IC TX laser driver schematic

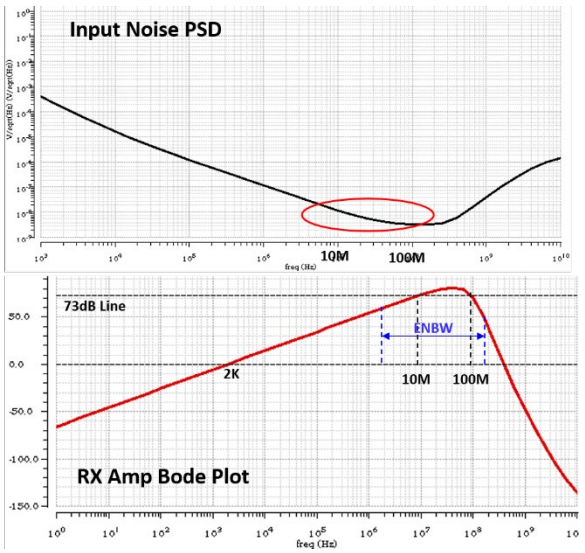
III. RESULTS AND DISCUSSIONS

Fig. 12(a) shows a post-simulation result of overall analog front-end block gain inside the RX block. The peak gain of LNA is around 17dB at 100MHz. LNA omits unwanted signals around 100MHz. PGA was implemented in a double-stage open-loop structure. Each block obtained a gain of a maximum of 27dB. Total gain ranges from 32dB to 85dB. The variable resistor in PGA is controlled with 10 bits. This gain range is enough with 200uV to 80mV input swing at off-chip TIA output. Fig. 12(b) shows input noise PSD along with RX amplifier gain Bode plot. As shown in the input noise PSD, thermal noise in the first stage LNA is the dominant noise source. Typical flicker noise is not considered in the proposed design, so a chopping circuit is not needed. Input referred noise of total analog front-end is 21 nVrms. Regarding the noise condition, it is shown that the design requirement was met.

After the signal is amplified through the front-end amplifier block, the signal is passed to ADC for amplitude detection and DLL for phase delay measurement. For amplitude measurement, a track-and-hold circuit was implemented for peak sampling. As a result, an 8-bit 100 MSps SAR ADC was implemented.

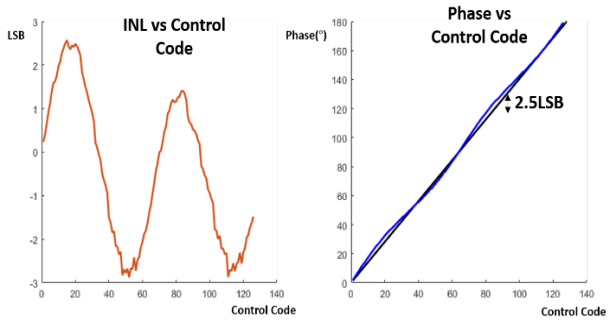


(a)



(b)

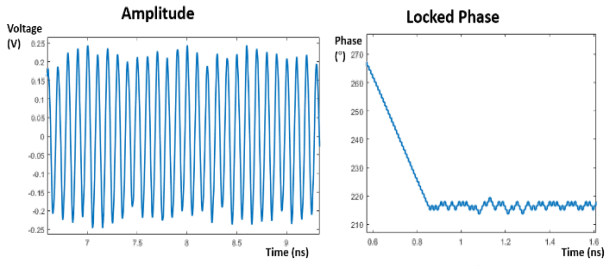
Fig. 12. Simulation result of FDNIRS RX; (a) Overall gain Bode plot (b) Input noise PSD and RX amplifier Bode plot



(a) (b)

Fig. 13. DLL simulation result; (a) INL of DLL output (b) DNL of DLL output

Fig. 13 shows the overall performance result of the DLL operation. When inspecting the INL of DLL in Fig. 13(a), the maximum INL was 3 LSB. Fig. 14 shows the result of overall RX operation with noise injected post-layout simulation. With noise injection, the peak sampling point of PGA output trembled. This phenomenon is also shown at phase output. To adjust this effect, a back-end DSP algorithm must be implemented to process the output signal.



(a) (b)

Fig. 14. RX unit transient result; (a) RX signal amplitude output (b) RX locked phase output

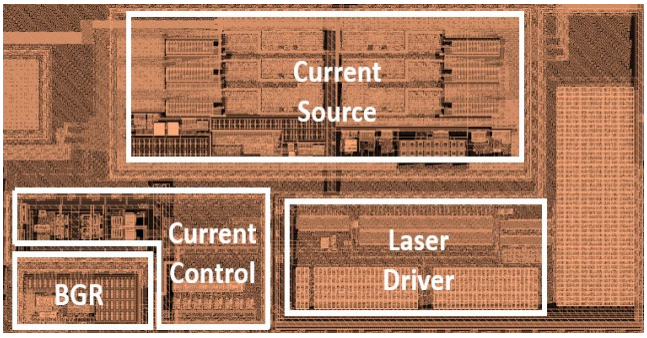


Fig. 15. FDNIRS TX floorplan

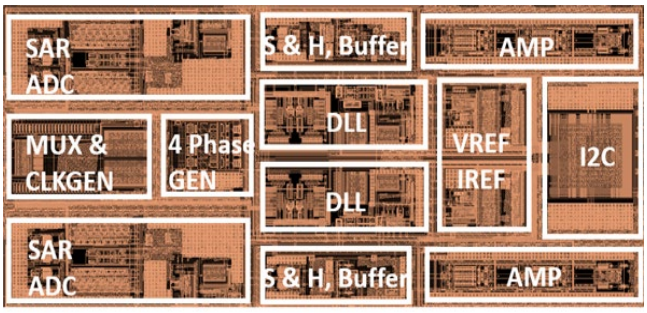


Fig. 16. FDNIRS RX floorplan

Fig. 15 shows the floor plan of the fabricated FDNIRS TX channel. The current source and BGR were designed for overall chip source distribution. A laser driver was implemented on the down-left side of the area. The current controller on the left of the laser driver transmits directly to the laser driver. Fig. 16 shows the floor plan of the fabricated FDNIRS RX channel. Two RX channels were implemented. These channels were implemented symmetrically. All blocks were implemented with a careful isolated guard-ring design for a low-noise layout. Four-phase generator is also implemented inside the RX channel area. Finally, digital control cores such as MUX, clock generator, and I2C communication interface are also implemented near RX channels.

Table II shows a summary of the overall fabricated IC specification and FDNIRS IC specification. This chip utilized a 0.18um process. The FDNIRS IC system was implemented on the remaining area of the revised version of the previous CWNIRS IC system. The whole CWNIRS IC system was fabricated on a 5mm by 5mm silicon die. FDNIRS IC consumed about 2.5mm by 2.5mm area. Due to its small area compared with the CWNIRS IC system, only two RX channels and one TX channel were designed. The whole chip utilized a 1.8V domain, while only the TX domain utilized 3.3V. The same domain was implemented on-chip I/O system. CWNIRS IC operates at a 32MHz external clock, while FDNIRS IC operates at a 200MHz external clock.

TABLE II. Overall IC specification and FDNIRS IC specification

Overall chip specification		
Process	TSMC 0.18um 1P6M CMOS	
Die size	5mm x 5mm	
Supply	RX core:1.8V TX: 3.3V	
Operating Frequency	32MHz (CWNIRS IC), 200MHz (FDNIRS IC)	
FDNIRS IC		
RX	**Gain control range**	32dB ~ 85dB
	Input referred noise (@ 100MHz)	21nV/√Hz
	3dB bandwidth	150MHz
	ADC resolution	8-bit SAR ADC
	Power consumption	0.94 mW/CH
TX	**Driving current**	5mA ~ 25mA
	Power consumption	18.8mW @minimum current driving

IV. CONCLUSION

Unlike conventional CWNIRS systems, the FDNIRS method can obtain absolute optical property, which leads to accurate bio-signal measurement. These methods give richer information than CWNIRS. However, FDNIRS was not widely adopted due to its bulkiness. To overcome this fundamental problem, this work tried to design a portable system. For the FDNIRS method, in particular, an integrated circuit system was designed and fabricated. The proposed system was able to obtain portability through photodiode and VCSEL pair. Although phase resolution is lower than other measurements, it was proven that this margin is enough for absolute optical property measurement. Further works are needed for both FDNIRS system design. For FDNIRS IC, actual chip testing and performance evaluation must be progressed.

TABLE III. Comparison table for proposed work

Comparison	**[3]**	**[9]**	**This work**
Main architecture	Laser(fiber), Photo-multiplier, Mixer	Laser(fiber), APD, High speed ADC	VCSEL, Photo-diode, DLL
System size	> 50 cm^3	> 100 cm^3	< 10 cm^3
Phase resolution	< 0.1º	< 0.1º	< 1.4º
Portability	X	X	O
System calibration	O	O	△

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REFERENCES

[1] Scholkmann, F., Kleiser, S., Metz, A. J., Zimmermann, R., Mata Pavia, J., Wolf, U., & Wolf, M. “A review on continuous wave functional near-infrared spectroscopy and imaging instrumentation and methodology.” *NeuroImage*, vol. 85, no. 1, pp. 6–27, Jan. 2014.

[2] J. -K Choi, J. -M. Kim, G. Hwang, J. Yang, M. -G. Choi and H. -M. Bae, “Time-Divided Spread-Spectrum Code-Based 400fW-Detectable Multichannel fNIRS IC for Portable Functional Brain Imaging,” *IEEE Journal of Solid-State Circuits*, vol. 51, no. 2, pp. 484-495, Feb. 2016.

[3] Sergio Fantini et al., “Frequency-domain multichannel optical detector for noninvasive tissue spectroscopy and oximetry,” *Optical Engineering*, vol. 34, no. 1, pp. 32-42. Jan. 1995.

[4] Raeef Istfan, Steven LaRochelle, Rachita Chaudury, Darren Roblyer, “A miniature frequency domain diffuse optical optode for quantitative wearable oximetry”, SPIE BIOS, San Francisco, California, United States, 2019, 108742B

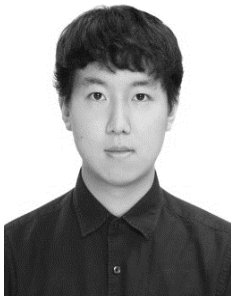
[5] Buttafava, M., Martinenghi, E., Tamborini, D., Contini, D., Mora, A. D., Renna, M., Torricelli, A., Pifferi, A., Zappa, F., & Tosi, A. “A Compact Two-Wavelength Time-Domain NIRS System Based on SiPM and Pulsed Diode Lasers,” *IEEE Photonics Journal*, vol. 9, no. 1, pp. 1–14, 2017.

[6] B. Calvo et al., "1.8V-100MHz CMOS Programmable Gain Amplifier", *IEEE International Symposium on Circuits and Systems*, Island of Kos, Greece, May 2006, pp. 263-266.

[7] Jaehyeok Yang et al., "Phase-Rotator Based All-Digital Phase-Locked Loop for a Spread-Spectrum Clock Generator," *IEEE Transactions on Circuits and Systems*, vol. 61, no. 11, Nov. 2014.

[8] Tongning Hu et al., "Analysis and Design of Bang-Bang PD-Based Phase Noise Filter," *IEEE Transactions on Circuits and Systems*, vol. 64, no. 10, Oct. 2017.

[9] Alyssa Torjesen, Raeef Istfan, Darren Roblyer, "Ultrafast wavelength multiplexed broad bandwidth digital diffuse optical spectroscopy for in vivo extraction of tissue optical properties," *Journal of Biomedical Optics*, vol. 22, no. 3, 036009, Mar. 2017.



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