Fully Integrated Triple-Mode Ka-Band Power Amplifier with Vertical-Horizontal Combined Transformer for 5G NR Applications

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***Abstract* – This paper presents a fully integrated triple-mode Ka-band power amplifier with a vertical-horizontal combined transformer for 5G NR applications, in 65 nm bulk CMOS process. With discrete power control using the proposed vertical-horizontal combined transformer, the triple-mode PA achieves enhanced efficiency performance in the power back-off region. The fully integrated triple-mode PA achieves 18.4-, 21.9-, and 23.5-dBm saturated output powers with 27.2, 34.9, and 41.5% peak PAEs in low power (LP), middle power (MP), and high power (HP) modes, respectively. The triple-mode PA can reduce the current consumption in LP the and MP modes.**

***Keywords*—5G, 65-nm, CMOS, High Efficiency, Ka-band, Power amplifier (PA), Power combiner, Triple-mode control**

I. INTRODUCTION

With the increasing demand for large amounts of data communication, more efforts have been made for 5G new radio (NR) wireless communications. Additionally, several studies on the integration of 5G mm-wave transceivers have been actively studied [1]-[18]. Most 5G mm-wave transceivers is should be implemented in portable devices; thus, a highly integrated method is desirable to minimize package form factor. Owing to the high-level integration in CMOS, designs of wireless transceivers using CMOS technology have been in the spotlight.

A power amplifier (PA) is a circuit in the final stage of the wireless transceiver. The input signal should be amplified to ensure a long transmission range. 5G NR signals typically have a wide bandwidth and high peak-to-average power ratio (PAPR). Thus, to satisfy linear specifications such as EVM and ACPR with these signals, PA should operate in a large back-off region from the saturated output power. The output power satisfying the linear requirements decreases.

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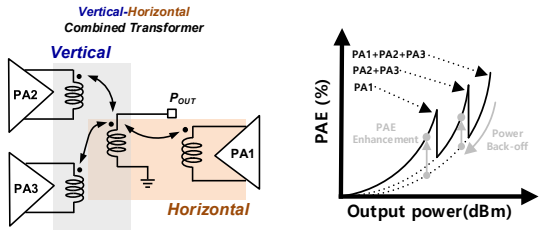
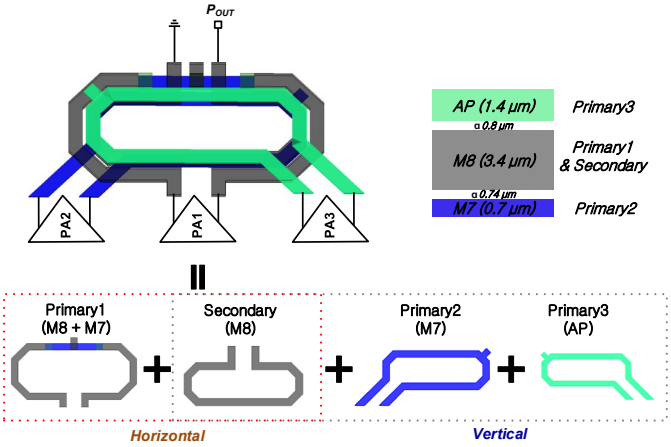


Fig. 1. (a) Block diagram of the proposed mm-wave multi-mode PA with vertical-horizontal combined transformer, (b) PAE versus output power with a using vertical-horizontal combined transformer

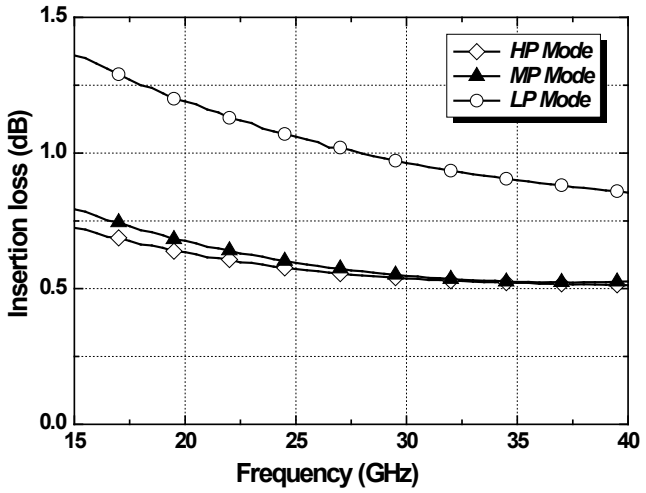
With the power combining method, the saturated output power and the linear output power can be increased. Among the power combining structures, transformer-based power combining methods have been widely used for fully integrated designs [1]-[13], [16]-[21]. Because the primary and secondary windings are spatially separated, the dc current flows only through the primary winding. Additionally, integrated transformers typically provide a balun function that converts differential signals into single-ended signal at the final output load.

Among the output combining transformer-based PA, series power-combining transformers (SCTs) and parallel power-combining transformers (PCTs) have been widely used [9]-[14], [19], [20], [22]-[24]. Compared to the SCT configuration, the PCT can be integrated into a relatively smaller area. Furthermore, there are imbalance problems in the input impedance provided by the SCT owing to the parasitic capacitance between the primary and secondary windings. For the construction of the PCT in few gigahertz range, the multi-turn secondary winding has typically been used and multiple primary windings interwind with the secondary winding in a lateral configuration [20], [21]. However, because a multi-turn secondary winding causes low Q and provides non-optimal low impedance to the power device in the mm-wave frequency range, the two primary windings cannot be interwound in a lateral configuration. In [17], two primary windings are placed below and above the one-turn secondary winding to form a two-input PCT configuration. Compared with previous PCT structure, a vertical-horizontal combining structure is adapted in the proposed structure. In this structure, three primary windings

are placed horizontally and vertically to form a three-input PCT configuration. Compared with typical dual-mode PAs, the proposed architecture provides triple-mode operation (low, middle, high power modes).



(a)



(b)

Fig. 2. (a) Exemplary layout of the proposed power combining network, (b) simulated insertion loss of proposed power combiner

On the other hand, PA is one of the major power consumers in 5G mm-wave transceivers. To increase the battery usage time of portable devices, PA should operate efficiently. PA operates more probably in the low-output-power range than in high-output-power range [25]. Thus, the multi-mode PA, which operates with lower current consumption than the single-mode PA in the low-output-power region, has been studied [20]-[23]. Multi-mode operation is advantageous for extending the battery usage time of portable devices. In this work, a multi-mode PA with the proposed transformer is introduced to reduce the current consumption in low-output-power range. Three individual power amplifiers connected to the three primary windings are operated based on the mode change.

In this paper, we propose a fully integrated triple-mode Ka-band PA with vertical-horizontal combined transformer for 5G NR applications to improve the efficiency performance in the LP and MP modes with a compact size.

In Section II, a detailed description of the proposed power combiner and an explanation of the two-stage CMOS PA design are presented. The post-layout simulation results are presented in Section III. Finally, Section IV presents the conclusions of this work.

	Driver stage (DA)	Power stage (PA)
Supply VDD (V)	1.2	2.4
Gate width (μm)	M5 – M6	M1 – M4
Gate length (nm)	32/65	64/65

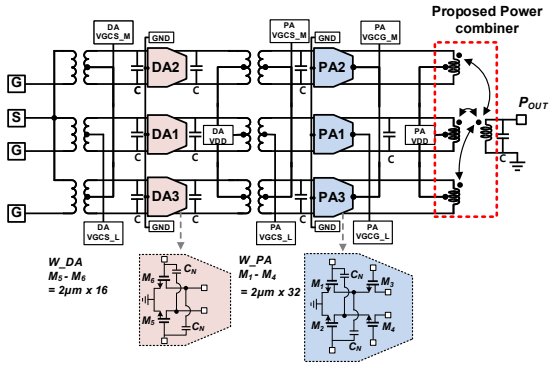


Fig. 3. Detailed schematic of the two-stage CMOS PA with proposed power combiner

II. DESIGN OF THE PROPOSED POWER COMBINER AND KA-BAND POWER AMPLIFIER DESIGN

A. Proposed parallel power combiner using vertical-horizontal combined transformer

The circuit diagram of the triple-mode PA using the proposed vertical-horizontal transformer is shown in Fig. 1(a). The proposed transformer is a parallel-power combining transformer with three inputs. In the proposed transformer, PA1 is connected to primary1, which is placed horizontally. Primary2 and primary3 which are connected to PA2 and PA3 are placed vertically down and up, respectively. Each primary winding is magnetically coupled to a secondary winding.

In LP mode, only PA1 is turned on and the other PAs are turned off. In MP mode, both PA2 and PA3 are turned on and PA1 is turned off. The HP mode requires all PA (PA1 + PA2 + PA3) to be turned on. Fig. 1(b) shows the PAE enhancement in the back-off region when using multi-mode PA.

Fig. 2(a) shows an exemplary layout configuration of the proposed vertical-horizontal combined transformer with 65-nm bulk CMOS technology. To construct the proposed vertical-horizontal transformer, 1.4μm thick aluminum pad (AP) layer, 3.4μm thick M8 copper layer, and 0.7μm thick M7 copper layer are used. As indicated by the red dotted box, primary1 and secondary windings use the same M8 layer to provide horizontal configuration. The primary1 is placed outside the secondary winding. Considering the connection of the output PAD and ground from the secondary winding, part of primary1 uses the M7 layer in the overlap area. The gray dotted box in Fig. 2(a) shows the vertical combination of the primary winding connected to PA2 and PA3. Unlike primary1, primary2 and primary3 are vertically placed below and above the secondary winding, respectively. The

M7 layer is used for primary2 and the AP layer for primary3. Using a compact vertical-horizontal combined transformer, it is possible to make a power combining transformer smaller in size, compared with previously studied power combining structures [20], [21]. Additionally, the proposed power combiner reduces current consumption in the MP and LP modes. Thus, it can be operated more efficiently if the PA should operate at a low-output-power level. The metal width of the three primary windings and secondary winding is 8μm and the spacing between the two M8 metals for the horizontal structure is 2μm. The size of the proposed transformer is 660μm × 755μm.

To investigate the insertion loss performance of the proposed transformer, an ADS electromagnetic (EM) simulation was performed. Fig. 2(b) shows the simulated insertion loss of the proposed vertical-horizontal combined transformer. In the HP mode, the insertion loss is 0.54 dB at the targeted frequency 28 GHz. The insertion losses in the MP and LP modes are 0.56 dB and 0.98 dB at 28 GHz, respectively. The proposed transformer provides low-loss performance and the insertion losses are less than 1 dB for all three cases.

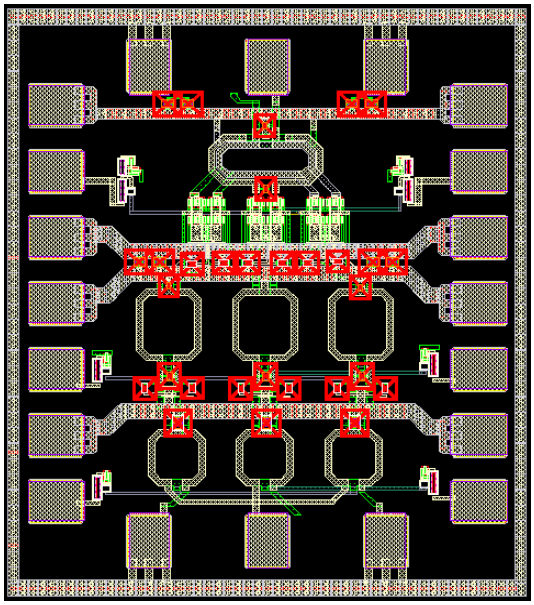


Fig. 4. Layout photograph of the proposed CMOS PA

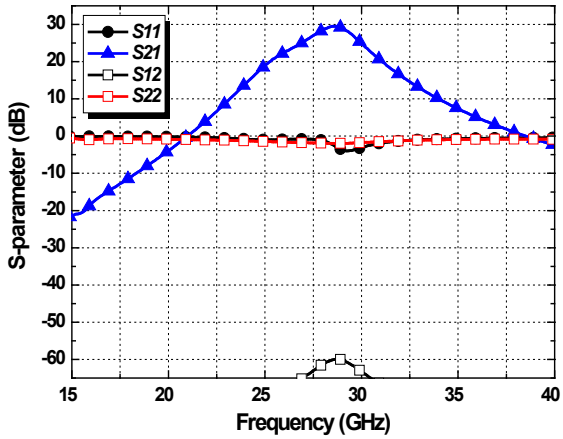


Fig. 5. Simulated small-signal S-parameters

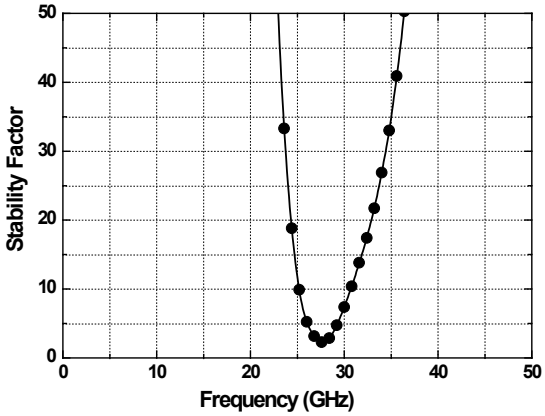


Fig. 6. Simulated stability factor

B. Design of Ka-band CMOS PA

Fig. 3 shows a schematic of the proposed triple-mode PA with a vertical-horizontal combined transformer. The schematic consists of a two-stage configuration as input transformers, inter-stage transformers, and the proposed parallel power combining transformer. The driver stage (DA) is used to provide a sufficient gain for the overall power amplifier. Three power stages (PA1, PA2, and PA3) and three driver stages (DA1, DA2, and DA3) are operated based on the multi-mode operation.

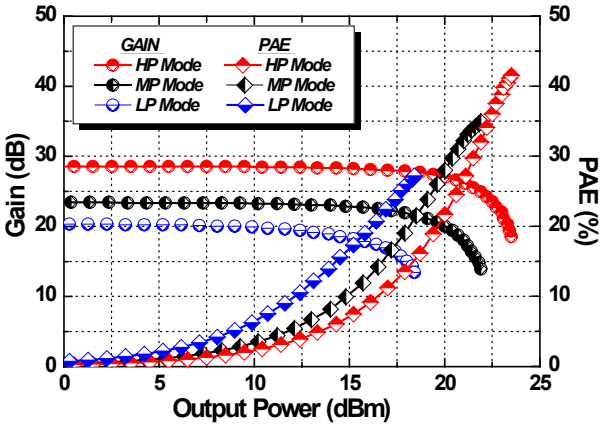


Fig. 7. Simulated gain and PAE versus output power in triple-mode at 28 GHz

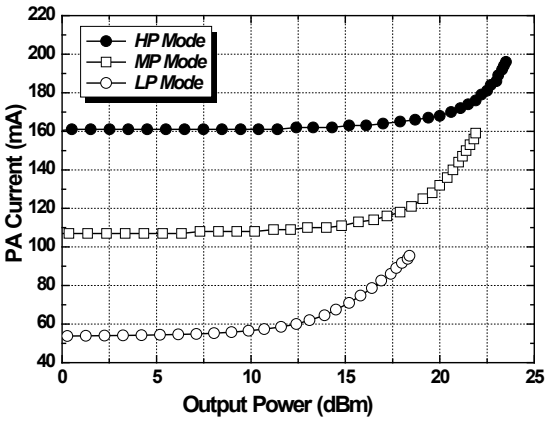


Fig. 8. Simulated current consumption of PA stages in triple-mode

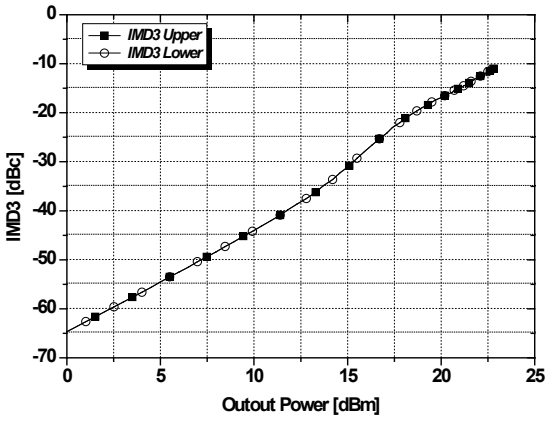


Fig. 9. Simulated IMD3

The bias conditions of PA2 and PA3 which operate in the MP mode, are the same (CS gate bias: PA VGCS_M and CG gate bias: PA VGCG_M). The bias of PA1 that operates in the LP mode is applied with the CS gate bias of PA VGCS_L and CG gate bias of PA VGCG_L. Similar to the bias conditions of the PAs, the gate bias of DA2 and DA3 are applied with DA VGCS_M, while the gate bias of DA1 is applied with DA VGCS_L.

For the configuration of the power stages, a cascode topology is applied with 2.4-V supply voltage. The device size of the common-source (CS) and common-gate (CG) devices is W/L = 128μm /65 nm in M1, M2, M3, and M4, respectively. For the configuration of the driver stages, CS topology is applied with 1.2-V supply voltage. The W/L size of M5 and M6 is 64μm /65 nm.

III. POST-LAYOUT SIMULATION RESULTS

The proposed PA with a vertical-horizontal parallel power combiner was designed using 65 nm CMOS technology. The layout of the designed PA is shown in Fig. 4. The total chip size is 660 × 755μm^2, including the dc supply pads and ground pads. Furthermore, the chip does not require additional off-chip matching because it includes input and output matching networks.

The simulated S-parameter results are shown in Fig. 5. S21 shows that the gain of PA is 28.5 dB at 28 GHz. Fig. 6 shows that the simulated stability factor is greater than one from 15 GHz to 40 GHz. The 1-tone simulation results for the PA with the proposed output power combiner are shown in Fig. 7. The simulated power gains of the proposed multi-mode PA are 20.3, 23.4, and 28.5 dB in LP, MP, and HP modes, respectively. The saturated output power, P_{SAT}, are 18.4, 21.9, and 23.5 dBm with peak PAE, PAE_{peak}, of 27.2, 34.9, and 41.5% in the LP, MP, and HP modes, respectively. The PAE results for each mode included the power consumption of the DA stages.

Fig. 8. shows the current consumption of the PA stages in triple-mode versus the output power at 28 GHz. When PA operates in the MP mode, the current consumption improved by 27.1% at 18.5 dBm output power, e.g. 5-dB back-off, when compared to the operation in the HP mode. The PA current at 18.5 dBm output power reduced from 166 mA in the HP mode to 121 mA in the MP mode. Compared to the HP and LP modes at a 13.5 dBm output power, e.g. 10-dB back-off region, the current consumption of the proposed triple-mode PA improved by 61.1% because the PA current decreased from 162 mA to 63 mA.

Therefore, thanks to the proposed vertical-horizontal combined transformer provides low insertion loss in a small size, the PA with the proposed transformer can achieve a high P_{SAT} of more than 23 dBm and PAE_{peak} of 41.5%. The IMD3 results are shown in Fig. 9.

Table I presents a comparison with other reported fully integrated 5G CMOS PAs in the mm-wave band. The proposed fully integrated triple-mode PA achieves not only a high P_{SAT} and PAE_{peak} in the HP mode but also the highest PAE in both the 5-and 10-dB back-off regions, PAE_{5dB} and PAE_{10dB}. A figure of merit (FOM) represents overall performance of the PA. The proposed PA shows the highest FOM among the previously reported KA-band CMOS PAs in table I.

TABLE I. Comparison of the proposed PA with the reported Ka-band CMOS PAs.

	This Work[#]	[16]	[17]	[18]
Tech. (nm)	65	65	65	65
Freq. (GHz)	28	28	28	28
Gain (dB)	28.5	18	15.9	15.8
P_{SAT} (dBm)	23.5	18.5	23.2	15.6
$P_{O,1dB}$ (dBm)	19.4	17*	22	14
PAE_{peak} (%)	41.5	27.3	33	41
PAE_{5dB} (%)	21.5	15*	18*	18*
PAE_{10dB} (%)	13	12*	8*	7*
FOM	97.1	79.8	83.2	76.4
Chip size (mm^2)	0.49	0.45	0.78	0.35*

FOM = P_{sat} (dBm) + Gain (dB) + 10log(PAE[%]×f^2[GHz])
[#]Simulated results
*Graphically estimated.

IV. CONCLUSION

This paper has proposed a triple-mode CMOS PA with a vertical-horizontal parallel-combined transformer using 65 nm CMOS technology. Using the proposed power combiner with a compact size, the triple-mode PA achieves improved efficiency performance with low-current consumption in the middle- and low-output-power regions. The triple-mode PA shows decreased current consumption of 166 mA to 121 mA (HP mode versus MP mode) at 18.5 dBm, e.g. 5-dB back-off, and 162 mA to 63 mA (HP mode versus LP mode) at 13.5 dBm, e.g. 10-dB back-off. Additionally, the proposed PA achieves a 23.5-dBm P_{SAT} and 41.5% PAE_{peak} in the HP mode.

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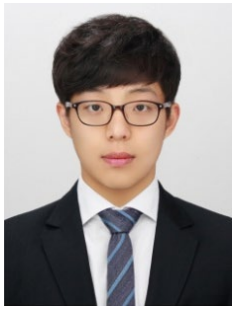

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