A Millimeter-wave CMOS Cross-Polarization Leakage Canceller for Dual-Polarized MIMO Systems

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Abstract **- This article introduces a power-efficient millimeter-wave CMOS cross-polarization canceller for dual-polarized multiple-in-multiple-out (MIMO) systems. The dual-polarized MIMO systems can transmit two independent data streams at the same time using a horizontally polarized and vertically polarized waves. A dual-polarized antenna provides a cross-polarization isolation, which offers spatial diversity. However, the module placement, propagation, and antenna/package non-idealities cause polarization coupling resulting in degradation of the error vector magnitude. To reduce cross-polarization leakage from these non-idealities, a power-efficient passive cross-polarization leakage cancellation path is introduced. The cross-polarization leakage canceller consists of horizontal path (H-path), vertical to horizontal cancellation (V-H C) path, vertical path (V-path), and horizontal to vertical cancellation (H-V C) path. The H-path and V-path consist of the variable gain amplifier (VGA), and the V-H C path and H-V C path consist of reflection type attenuator, 0/90° 1-bit phase shifter, 0/180° 1-bit phase shifter, and 0 to 90° continuous phase shifter. Implemented in 65 nm CMOS, the proposed cross-polarization canceller improved the cross-polarization isolation better than 21.7 dB.**

Keywords**—60 GHz, Attenuator, Cancellation, CMOS, Cross-polarization (X-pol), Dual-polarization, Isolation, Leakage, Millimeter-wave, Multiple-in-multiple-out (MIMO), Phase shifter, Variable gain amplifier**

I. INTRODUCTION

Recently, wireless communications using millimeter-wave bands are emerging for high-speed, multi-user connectivity. Several millimeter-wave transceivers over 10 Gb/s data transmission over the air have been researched [1–5].

To achieve high data rates, a wide variety of techniques such as multiple-in-multiple-out (MIMO), high order modulations [quadrature-amplitude modulation (QAM)], and full-duplex operation [6]. However, complex higher order modulation such as 64 QAM requires higher signal-to-noise ratio (SNR), back-off operation, and high quality of phase noise performance. These limit the communications distance and require complex signal processing. To overcome these limitations, dual-polarized MIMO transceivers are introduced [4–6]. Dual-polarized MIMO uses two independent data streams through the vertical-polarization (V-pol) and horizontal-polarization (H-pol) using a dual-polarized antenna [7-9]. Therefore, Dual-polarized MIMO transceiver transmit X2 data rate compared to single-polarization. The demerit of the dual-polarized MIMO cross-polarization (X-pol) leakage due to non-idealities such as antenna performance, package, module placement and propagation.

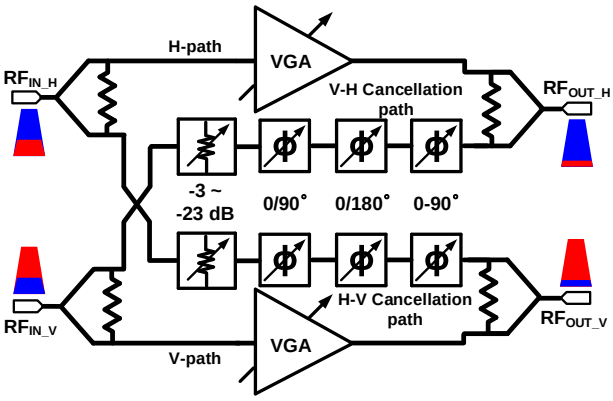

Fig. 1. Block-diagram of the proposed X-pol leakage canceller.

To implement highly efficient and compact millimeter-wave dual-polarized MIMO systems, this paper introduces a power-efficient millimeter-wave CMOS cross-polarization leakage canceller. We use 60 GHz frequency band since the 60-GHz unlicensed band can realize data rates of tens of Gb/s due to its wide bandwidth [3–4]. The X-pol leakage should be better than 20 dB to support single-carrier 16 quadrature amplitude modulation [6]. With a power-efficient passive cross-polarization leakage cancellation path, X-pol leakage is cancelled out using additional X-pol leakage cancelling path, which improves X-pol isolation. The proposed X-pol canceller shows X-pol isolation better than 21.7 dB.

II. CIRCUIT DESIGN

A. Cross-polarization canceller architecture

A power-efficient and high accuracy X-pol leakage cancellation circuit is introduced to improve the data rate, system power efficiency, and error vector magnitude (EVM).

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The block diagram of the proposed X-pol leakage canceller is shown in Fig. 1. The X-pol leakage canceller consists of two power dividers, horizontal-path (H-path), vertical-path (V-path), horizontal to vertical cancellation path (H-V C path), vertical to horizontal cancellation path (V-H C path), and power combiner. H-path and V-path consist of variable gain amplifier (VGA) and H-V C path and V-H C path consist of reflection type attenuator, 0/90° 1-bit phase shifter, 0/180° 1-bit phase shifter, and 0 to 90° continuous phase shifter. In the normal RX mode, reflection type attenuator is set to have the lowest gain while cancellation paths are operating in the X-pol cancellation mode to minimize the X-pol by the magnitude and phase control.

B. Power divider/combiner

The X-pol leakage canceller should provide high isolation between V-/H-paths and H-V/V-H C paths to prevent the unwanted feedback signal between RF_{IN_H}/RF_{IN_V} and RF_{OUT_H}/RF_{OUT_V} in Fig. 1. Fig. 2(a) shows the power divider/combiner. For high isolation, low-loss, and compact size, the power divider is based on the Wilkinson power divider and employs coupled inductors with a shunt capacitor [10]. The coupled inductors increase inductance in even-mode operation, which reduces insertion loss, due to lower parasitic resistance, and chip area from compact layout and smaller inductor size. In odd-mode operation, inductance of the coupled inductors is reduced, so a shunt capacitor is required for compensation of matching and isolation. Fig. 2(b) shows the simulated and measured insertion losses of the power divider. The coupled inductor contributes a smaller inductor size resulting in lower insertion loss. Excluding a power dividing loss of 3 dB, the measured insertion loss was 0.3–0.7 dB for 50–67 GHz. The measured isolation is more than 14 dB from 50 to 67 GHz as shown in Fig. 2(c).

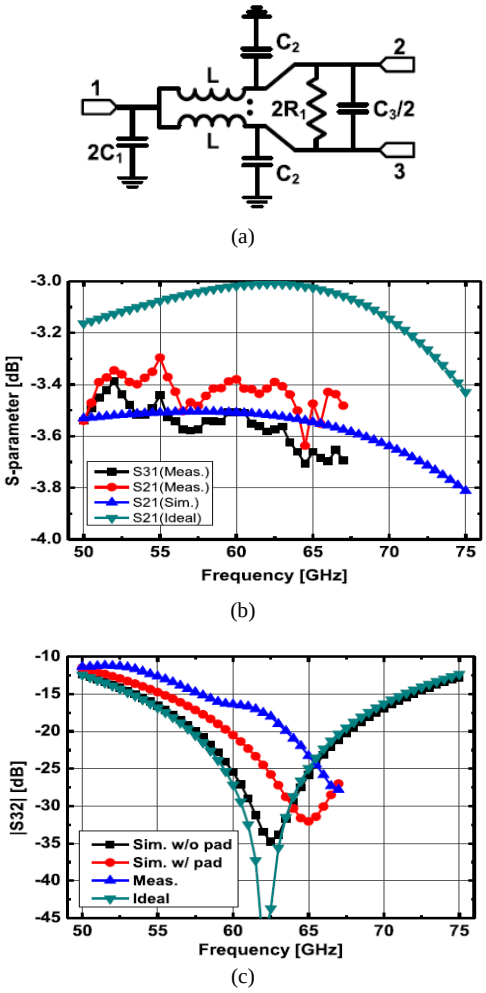


Fig. 2. Low loss and compact power divider; (a) schematic (b) ideal, simulated, and measured insertion losses (c) ideal, simulated and measured isolation [10].

C. Variable gain amplifier

Fig. 3 shows the simplified schematic of the proposed 60 GHz VGA with current-steering cascode. The current-steering cascode VGA uses inductors, L5 and L9, between sources of M4 and M6 and drains of M1 and M5 for low impedance variation, which contributes a lower phase variation during the gain control.

The proposed VGA is designed to provide a variable gain with a high gain and low noise. For the optimum noise figure of the VGA, transistors M1 and M5 adopt an unit finger width of 1 μm and source inductors, L4 and L8. For proper noise figure, power gain and power handling capability, a total transistor width of 20 μm are chosen for M1, M4, M5, and M6.

The proposed VGA is designed to have a simulated gain of 4/10 dB with 1-bit gain control at 60 GHz and a phase variation less than 5° for 56–67 GHz. The simulated input and output return losses are better than 10 dB for 57–66 GHz.

D. Reflection type attenuator

Fig. 4 shows the simplified schematic of the proposed 60 GHz reflection type attenuator. The proposed attenuator consists of a transformer-based 90° hybrid coupler and transistors at the reflection load. The transformer-based 90° hybrid coupler is employed to achieve a low loss and compact size and uses top two thick metal layers for low loss design [11]. The proposed transformer-based 90° hybrid coupler occupies a 110 μm × 80 μm footprint only. The proposed transformer-based 90° hybrid coupler is designed at a center frequency of 61.5 GHz and provides 90° phase difference between the thru and coupled ports with a phase error better than ±1.5° for 56–67 GHz.

To provide variable attenuation, NMOS shunt transistors are used at the reflection load and gate bias is controlled, which varies resistance of the reflection load resulting variable attenuation. The floating body and gate bias technique in the transistors is used for lower parasitic capacitance resulting lower loss [12].

The proposed attenuator is designed to have a gain of -3 to -23 dB at 60 GHz. The simulated input and output return losses are better than 10 dB for 56–67 GHz. The simulated gain flatness is better than 0.5 dB for 56–67 GHz.

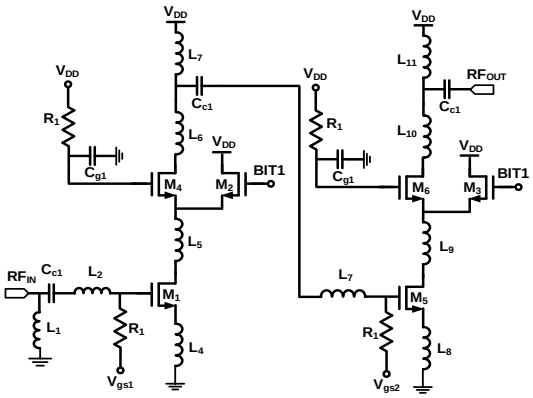


Fig. 3. Schematic of the variable gain amplifier.

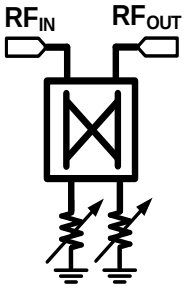


Fig. 4. Schematic of the reflection type attenuator.

E. Phase shifters

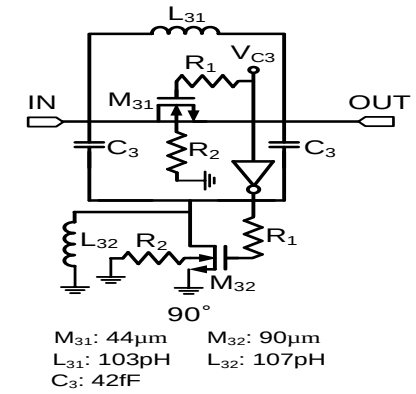
Fig. 5 shows the simplified schematic of the proposed 60 GHz phase shifters. The phase shifter consists of 0/90° 1-bit phase shifter, 0/180° 1-bit phase shifter, and 0 to 90° continuous phase shifter and covers full-360° phase shifting. The 0/90° and 0/180° phase shifters use fully custom-designed capacitors for low insertion loss and small process variation [13]. The 0/90° phase shifter uses switched-filter type for low loss and compact design while the 0/180° phase shifter adopts high-pass/low-pass type to reduce chip area and insertion loss.

Fig. 5(c) shows the simplified schematic for the reflection type phase shifter, which provides fine phase shifting with low insertion loss and chip area [11]. The coupler is same with the transformer-based 90° hybrid coupler of Fig. 4. The reflection load includes varactors to provide phase shifting with low gain variation.

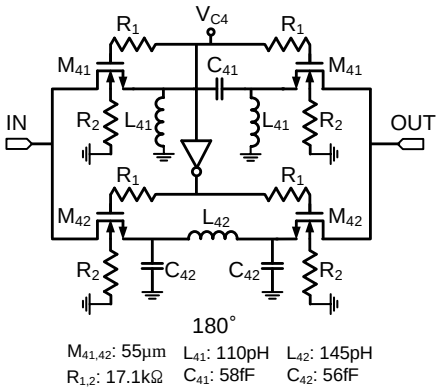
F. Cross-polarization canceller design

Fig. 6 shows the layout of the proposed 60 GHz CMOS X-pol leakage canceller. Designed in 65 nm CMOS, the proposed X-pol leakage canceller consumes 22mW from a supply voltage of 1V and occupies an area of 1.06 × 1.22 mm^2 including the bond pads.

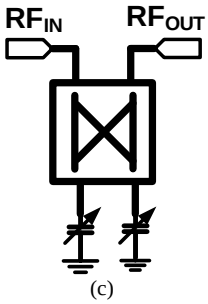
The proposed X-pol leakage canceller is designed to have a simulated gain of 0/7 dB with 1-bit gain control at 60 GHz and a phase variation less than 5° for 56–67 GHz. The simulated input and output return losses are better than 10 dB for 57–66 GHz. X-pol leakage less than -10 dB can be removed with V-H C path and H-V C path operation modes.



(a)



(b)



(c)

Fig. 5. Phase shifters; (a) 1-bit 0/90° [13] (b) 1-bit 0/180° [13] (c) continuous 0 to 90°.

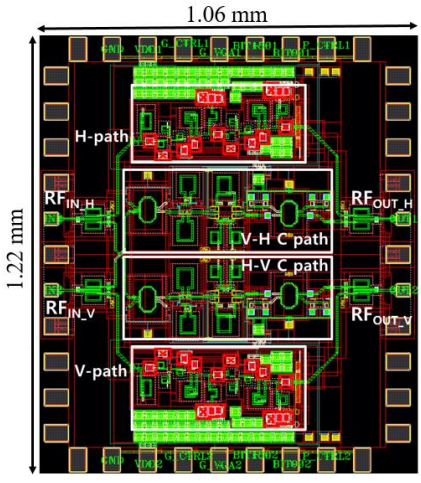


Fig. 6. Layout of the proposed X-pol leakage canceller.

III. EXPERIMENTAL RESULTS

The proposed X-pol leakage canceller with a power-efficient passive X-pol leakage cancellation path was implemented in a standard 65-nm CMOS technology. The X-pol leakage canceler dissipates a DC power of 22 mW from a supply voltage of 1 V. The fabricated chip is measured via on-wafer probing with ground-signal-ground pads. The S-parameter was measured with an Agilent E8361A vector network analyzer and the results were calibrated using the Picoprobe SOLT (short-open-load-thru) calibration substrate. The GSG pad loss is less than 1 dB and included in measurement result.

Fig. 7 shows the measured signal gain and X-pol leakage gain of the X-pol leakage canceller relative to input power. The measured gain of the proposed X-pol leakage canceller is -1 dB to 6 dB for signal path and -3 dB to -21 dB for canceller path at 60 GHz. The canceller path provides 360° phase shifting. The proposed X-pol leakage canceller provides X-pol leakage better than 21.7 dB.

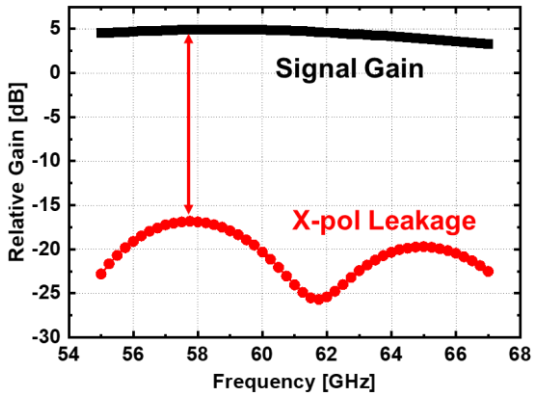


Fig. 7. Measured signal gain and X-pol leakage gain of the X-pol leakage canceller relative to input power.

Fig. 8 shows the measured input and output return losses of the proposed X-pol leakage canceller. The measured input and output return losses were better than 10 dB for 56–67 GHz.

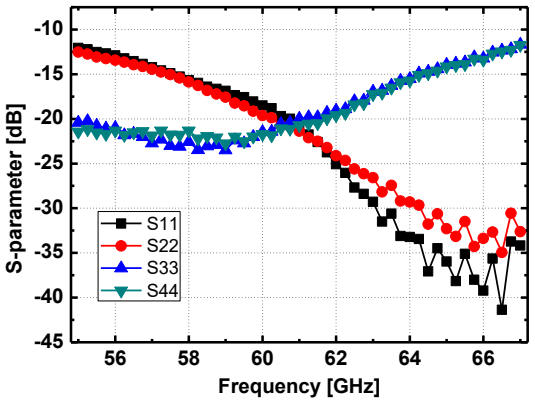


Fig. 8. Measured input and output return losses of the proposed X-pol leakage canceller.

IV. CONCLUSION

A 60 GHz CMOS X-pol leakage canceller for dual-polarized MIMO systems was designed and implemented using a standard 65-nm CMOS technology. With a power-efficient passive X-pol leakage cancellation path, the proposed X-pol leakage canceller provides high X-pol isolation better than 21.7 dB. The measurement results indicate that the proposed X-pol leakage canceller is suitable for energy efficient and compact MIMO Systems.

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