A 300-GHz Phase Shifter and High-Power VCO for Phased Array Applications

Eun Jung Kim[1], Hyun Joon Kim and Sang Geun Jeon[a]
Department of Electrical Engineering, Korea University
E-mail : [1]ejkim96@korea.ac.kr

***Abstract* – This paper presents a 300-GHz phase shifter and a fundamental high-power VCO designed using a 250-nm InP double heterojunction bipolar transistor (DHBT) technology. The phase shifter employs a 180° reflection-type phase shifter (RTPS) and a 1-bit 180° active switched-type phase shifter (STPS) to achieve a 360° phase shift range. The STPS includes an active single-pole double-throw (SPDT) switch for compensating insertion loss of the passive components and providing gain. The simulation shows that the phase shifter achieves a full 360° phase shift over the frequency range from 220 to 320 GHz. The peak average gain is 1.3 dB at 285 GHz and the 3-dB bandwidth is 50 GHz. In addition, the common-base cross-coupled VCO core employs a coupled-line feedback to minimize the loss caused by via interconnections. To further increase the output power, the differential signal from the output buffer is combined by a slotline power combiner. By modeling the microstrip-to-slotline transition, the equivalent circuit and impedance matching of the combiner is analyzed. The simulated output power is 8.4 dBm at 300 GHz and the dc power consumption is 90 mW. This leads to a peak dc-to-RF efficiency of 7.2 %. The VCO exhibits a simulated frequency tuning range of 20 GHz (300–320-GHz).**

***Keywords*—Active switch, High output power, Phased array, Phase shifter, Power combiner, Terahertz band, Voltage-controlled oscillator (VCO)**

I. INTRODUCTION

Recently, there have been several phased-array systems reported operating at the mm-wave and THz frequency regime [1]–[3]. Despite the limitation of device speed at high frequencies, benefits such as high data throughput and high data security by using wide unlicensed frequency band attracts many industries and circuit designers. However, aside the device performance, free-space path loss (FSPL) increases significantly at these frequency regions. Large scalable phased-array systems are therefore desired for increasing the equivalent isotropic radiated power (EIRP).

A phase shifter is a core circuit block that controls the phase of each channel of the phased-array system. Several topologies of the phase shifters in the 300-GHz band have been reported in recent years [4]–[6]. However, due to the significant passive loss and limited device speed at the high frequency of terahertz, most active phase shifters provide no gain while consuming considerable dc power. On the other hand, most passive phase shifters suffer from large insertion loss and a limited phase shift range of less than 360°. In this paper, a 180° reflection-type phase shifter (RTPS) and a 1-bit switched-type phase shifter (STPS) using an active switch are combined to provide a full 360° phase shift and compensate large insertion loss.

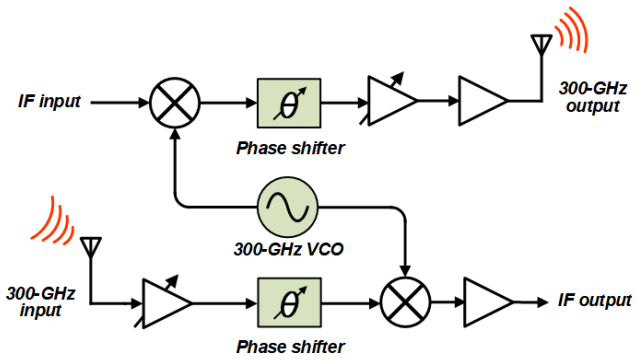


Fig. 1. Simplified block diagram of a 300-GHz phased-array transmitter.

An LO signal source is a key component for driving the frequency up- and down-conversion mixers. In general, an amplifier-multiplier chain (AMC) is usually used for providing the LO signal above 200 GHz. However, a considerable amount of dc power and chip area is consumed due to drive amplifiers and power amplifiers (PAs), which increases the design complexity. Therefore, an on-chip fundamental VCO with sufficient output power is an attractive solution over power hungry and relatively bulky AMCs as depicted in Fig. 1. The VCO requires not only a wide frequency tuning range, but also a high output power to maximize the conversion gain of the mixer. In this paper, a coupled-line based VCO core and a slotline power combiner are introduced for high LO power generation at 300 GHz.

This paper presents a 300 GHz phase shifter and a high-power VCO for phased array application. Section II provides a brief introduction of the device technology. A detailed phase shifter and VCO design are presented in Section III and Section IV, respectively. In Section V, the simulation results of the phase shifter and VCO are provided. Lastly, Section VI summarizes this paper.

a. Corresponding author; sgjeon@korea.ac.kr

Manuscript Received Mar. 16, 2022, Revised Sep. 20, 2022, Accepted Sep. 26, 2022

II. TECHNOLOGY DESCRIPTION

The proposed 300-GHz phase shifter and high-power VCO are designed in the Teledyne 250-nm InP double heterojunction bipolar transistor (DHBT) process technology. The 4x0.25 μm^2 transistor provides f_T of 370 GHz and f_{max} of 640 GHz. This process also provides four metal layers (M1-M4) with a 3-μm top metal, a metal-insulator-metal (MIM) capacitor with a silicon nitride (SiN_x) capacitor dielectric and a Nichrome (NiCr) thin-film resistor.

III. 300-GHz PHASE SHIFTER DESIGN

Fig. 2 shows the schematic of the proposed phase shifter. It consists of a 180° RTPS presented in [7] and a 1-bit 180° STPS. The RTPS provides a continuous 180° phase shift with a single control voltage. The STPS provides 0°/180° phase inverting. It consists of two active SPDT switches, a low-pass filter (LPF) and a high-pass filter (HPF). Compared to the conventional switched line topology which uses a long transmission line of λ/2 for 180° phase delay, the LPF and HPF are adopted for the 180° delay component to reduce the amplitude difference between 0° and 180° states and reduce chip area. In addition, the SPDT switch employs an active topology to compensate the loss of the passive components.

A. 300-GHz Active Switch Design

Due to the unilateral nature of the active device, the transmit SPDT switch and the receive SPDT switch are designed respectively. Both active SPDT switches employ a two-stage common-base (CB) topology to improve gain and isolation. The direction in which the signal passes is determined by applying a voltage to the transistor base of the second stage. Also, the first CB transistor is self-biased through a large resistor between collector and base so that an appropriate voltage is applied. The emitter length of all transistors is determined to be 3μm, which is the minimum design rule defined by the technology, for low dc power consumption. A transmission line and a short stub are used for input matching of both switches to provide 50-ohm port matching and a dc ground path at the same time. For the output stage matching, a transmission line and short stub are used. In addition, a 10-ohm resistor is added in series to the short stub to increase the stability and expand the output matching bandwidth.

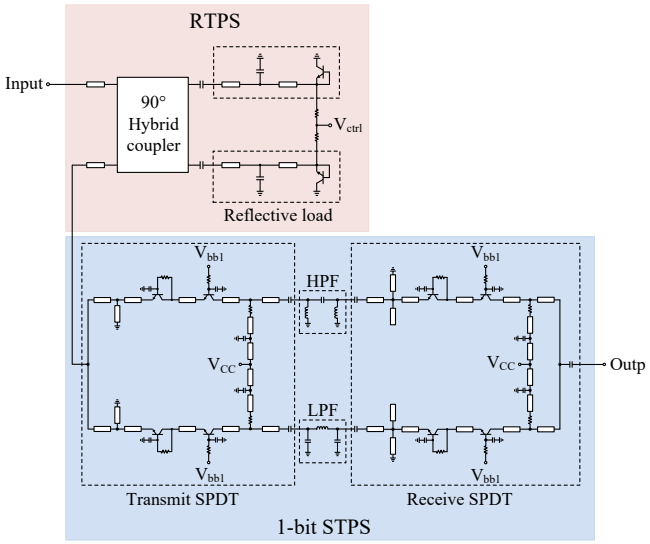


Fig. 2. Schematic of the proposed phase shifter.

B. LPF and HPF Design

The LPF and the HPF are designed based on lumped elements. Both filters are adopted a π-type structure and the equation of the lumped element values are given by [8]

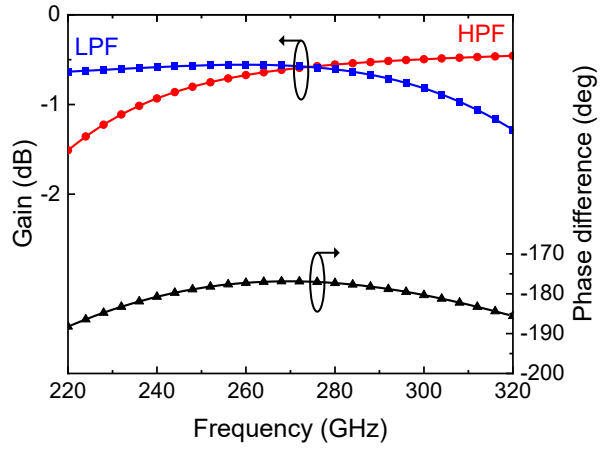
$$L_{HPF\_pi} = \frac{Z_0 sin(\phi)}{\omega(1 - cos(\phi))} \quad (1)$$

$$C_{HPF\_pi} = \frac{1}{\omega Z_0 sin(\phi)} \quad (2)$$

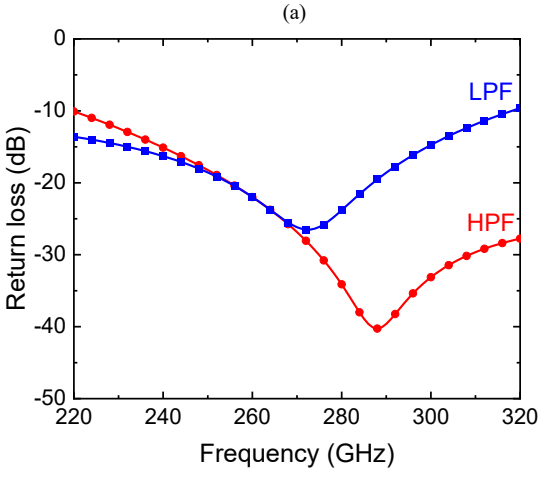
$$L_{LPF\_pi} = Z_0 \frac{sin(\phi)}{\omega} \quad (3)$$

$$C_{LPF\_pi} = \frac{1 - cos(\phi)}{\omega Z_0 sin(\phi)} \quad (4)$$

According to equations (1)-(4), the required inductance and capacitance for LPF and HPF configuration are calculated as 30 pH and 12 fF at 280 GHz, respectively. The inductor is implemented using a high impedance



(a)



(b)

Fig. 3. Simulated (a) amplitude and phase difference and (b) return loss of the low-pass filter and high-pass filter.

transmission line, and a metal-insulator-metal (MIM) capacitor is used. In order to optimize each component, electromagnetic (EM) simulations were carried out using Agilent ADS Momentum.

The simulated amplitude and phase difference of the LPF and the HPF are shown in Fig. 3(a). The simulated amplitude of both filters is -1.5 to -0.5 dB over the frequency range from 220 to 320 GHz. The phase difference ranges from 177 to 188°. Fig. 3(b) shows return loss of the LPF and HPF. The return loss is better than 9.6 and 10.1 dB at the LPF and HPF, respectively, from 220 to 320 GHz.

IV. HIGH POWER VCO DESIGN

A. Coupled-Line VCO

Fig. 4(a) shows the simplified circuit blocks of the 300-GHz high-power VCO. To achieve higher output power, the differential fundamental signal is combined using a slotline power combiner, which will be explained section III-B. As shown in Fig. 4(b), a common-base coupled-line cross-coupled topology is employed, which was first introduced in [9]. Common-base LC cross-coupled oscillators using InP HBT technology have been reported to provide higher oscillation-frequency than common-emitter configuration [10], which is more suitable for designing a fundamental oscillator above the sub-THz band.

A feedback network using coupled lines allows compact layout while having the benefits of removing dc block capacitors. Therefore, additional loss by vias for dc block capacitor interconnections can be eliminated, which improves the feedback loop gain and output power. While the coupled-line length is fixed for oscillation frequency, output power varies with different coupling factor C, as shown in Fig. 5. In our design, coupling factor of 0.3 is chosen so that the simulated core power is 5.5 dBm at 300 GHz. The varactor (Q_{var}) using a base and emitter tied HBT device is implemented between the core emitter and coupled-line for frequency tuning. The length of TL_{var} was adjusted for maximum tuning range.

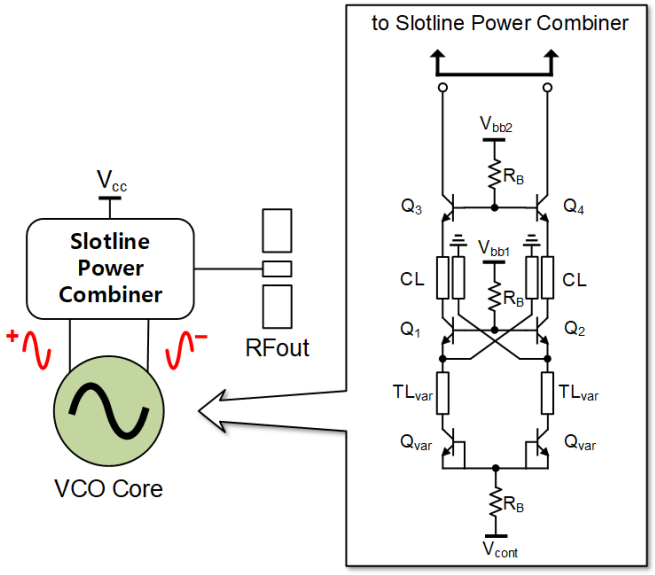


Fig. 4. (a) Simplified circuit block diagram and (b) schematic of the coupled-line VCO core and common-base output buffer.

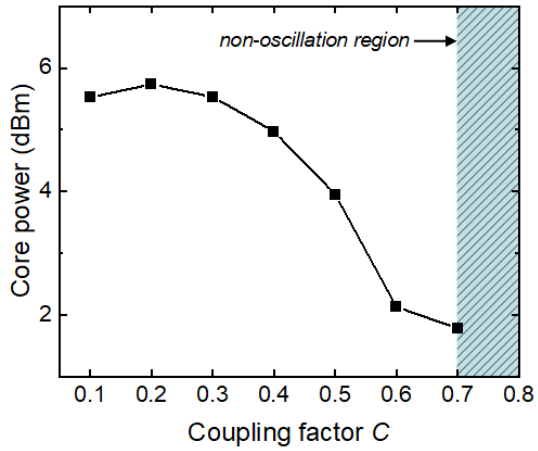


Fig. 5. Simulated fundamental signal power from the oscillator core with different coupling factor C.

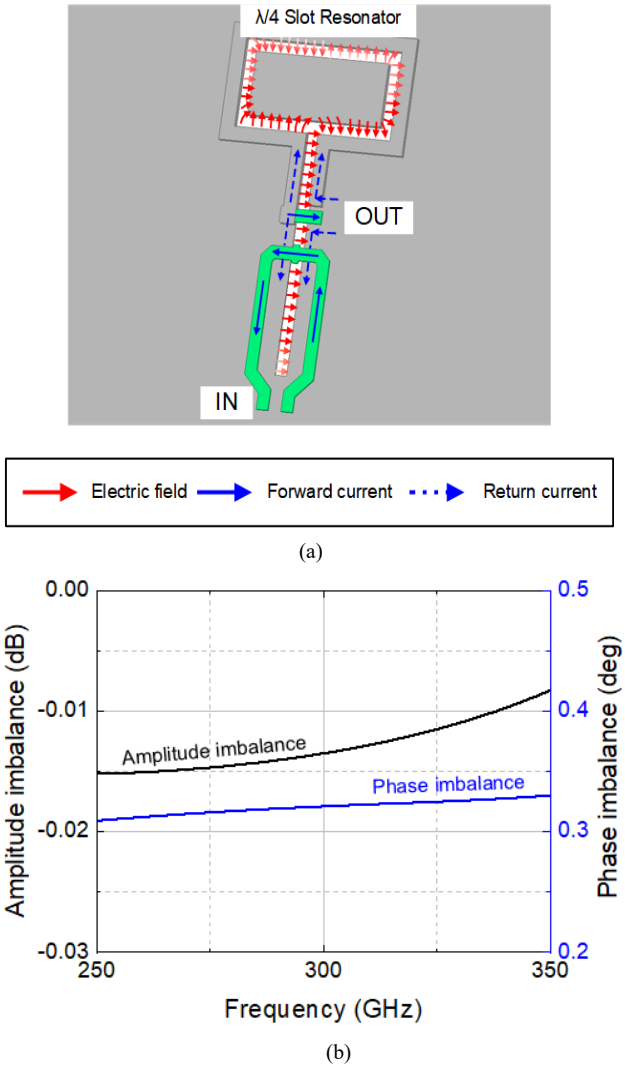


Fig. 6. (a) 3-D view and electrical field distribution of the proposed slotline power combiner. (b) Simulated amplitude and phase imbalance performance.

B. Slotline Power Combiner

Conventional mm-wave on-chip power combiners utilize transformers using separate transmission lines for the primary and secondary coils [11]–[13]. However, as the frequency increases into the THz range, parasitic capacitance between the coil causes imbalance, resulting poor power combining performance due to imbalanced load impedance seen from the transistor output. There are recent reports using slotline based power combiners which shown excellent amplitude and phase imbalance over a wide frequency range [14], [15]. In this section, a wideband balanced and low input impedance slotline power combiner is introduced.

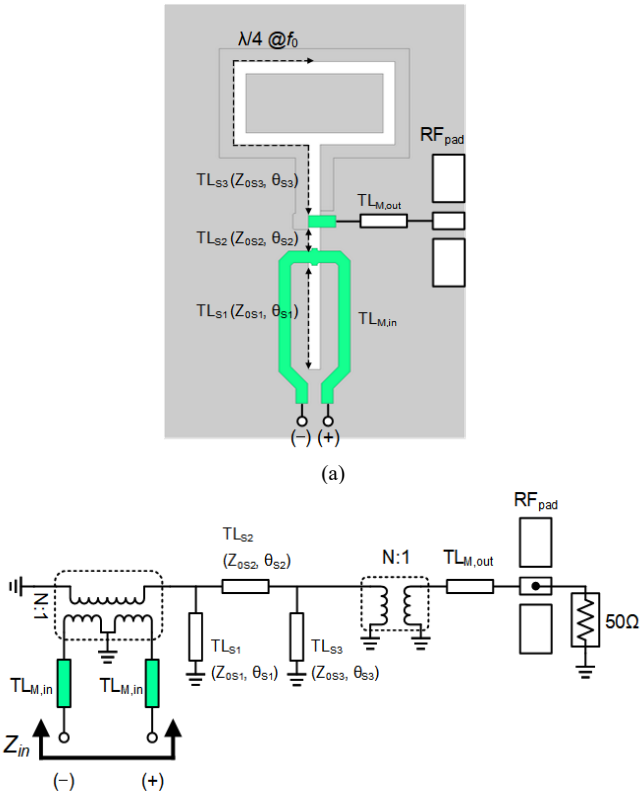


Fig. 7. (a) Top view and (b) equivalent circuit of the slotline power combiner.

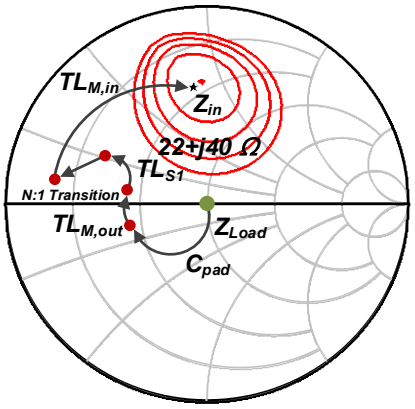


Fig. 8. Simulated output power contours of the output buffer and impedance transformation trajectory of the slotline power combiner at 300 GHz.

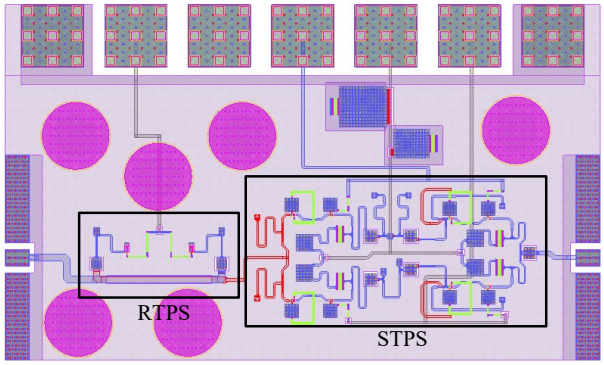


Fig. 9. Layout of the phase shifter.

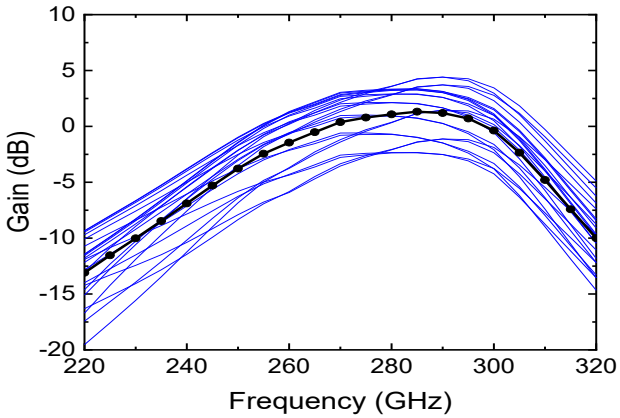


Fig. 10. Simulated gain performance of the phase shifter.

The proposed slotline power combiner is shown in Fig. 6(a). Differential output signal from the common-base buffer (Q_3 and Q_4) is combined to a single-ended signal at the microstrip-to-slotline transition and propagates along the slotline. The time-varying electric field of the combined signal from the slotline induces a time-varying magnetic field to the output microstrip line, which occurs to the input in the same way. Due to the balanced nature of the slotline and orthogonal electric field between the transition, the out-of-phase balance performance is achieved, as shown in Fig. 6(b).

Magnetic coupling between the microstrip line and slotline is equivalent to a transformer in which a turn ratio n can be derived by the voltage ratio at the coupling point. A short end is created in the slotline TL_{S2} and TL_{S3} in Fig. 7(a) by ending the slot with the ground metal layer, thus leading to a short-circuited stub. The equivalent circuit of the proposed slotline power combiner can be modeled as shown in Fig. 7(b). First, the 50 Ω load impedance is connected to series RF probing pads and microstrip transmission line $TL_{M,out}$, which is inevitable due to on-wafer probing measurements. The microstrip line is then directly short-circuited to the slot to reduce series reactance. Second, microstrip-to-slotline transition transforms the load impedance by a product of N^2. The turns ratio N is verified to be 0.98 by simulation. Since the quarter-wavelength slotline stub TL_{S3} leads to a high impedance, the induced electric field propagates towards TL_{S2} with phase delay of θ_{S3}. Slotline stub TL_{S1} is shorter than a quarter wavelength in order to resonate the output

capacitance of the output buffer. After the slotline-to-microstrip transition, the microstrip line $TL_{M,in}$ also provides inductance to resonate the output capacitance as well. As the output buffer operates in the large-signal region, optimum load-pull matching is required for maximum output power. The impedance seen from the input side of the slotline power combiner is 22+*j*40 Ω which the closely matches the load-pull contours shown in Fig. 8, giving an output power of 8.9 dBm. Therefore, the slotline based combiner not only combines the out-of-phase output signal, but also performs a transformer-like impedance matching network.

V. SIMULATION RESULTS

A. 300-GHz 360° phase shifter

The layout of the phase shifter is shown in Fig. 9. The circuit area including RF and DC probing pads is 713 x 427 μm^2. Fig. 10 presents a simulated gain of the phase shifter. In the 0° and 180° states of the STPS, the control voltage of the varactor of the RTPS changes between -0.5V and +0.5V by 0.1-V step. It is found that the gain ranges from -2.3 to 3.5 dB at 280 GHz. The peak average gain is 1.3 dB at 285 GHz with a 3-dB bandwidth from 255 to 305 GHz.

The simulated phase shift performance is shown in Fig. 11. A continuous phase shift of at least 379° is achieved in the 220 to 320 GHz band. Fig. 12 depicts the simulated input and output return loss for all phase states. The input and output return loss are better than 8.2 and 10.4 dB, respectively, from 220 to 320 GHz. The dc power consumption is 40.5 mW from 3-V supply voltage.

In Table I, the proposed phase shifter is compared with the state-of-the-art phase shifters operating in the 300-GHz band [16]–[18]. This work achieves a 360° phase shift range and provides gain with low dc power consumption.

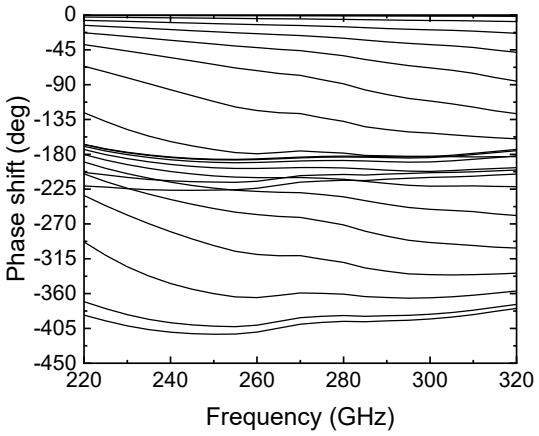


Fig. 11. Simulated phase shift performance.

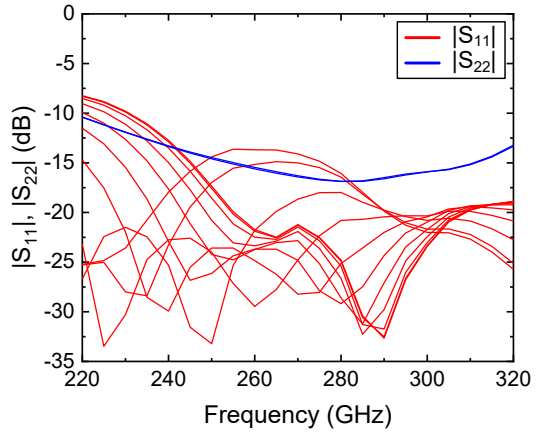


Fig. 12. Simulated input and output matching performance of the phase shifter.

B. 300-GHz High Power VCO

The layout of the 300-GHz coupled-line VCO with a slotline power combiner is depicted in Fig. 13. The VCO consumes an area of 142 × 321 μm^2 excluding RF and dc probing pads.

Fig. 14 shows the simulated oscillation frequency and output power with respect to the varactor control voltage varying from -1.0 to 1.0 V. The VCO exhibits a tuning range of 20 GHz (300 GHz to 320 GHz, 6.4 %) with a peak output power and dc-to-RF efficiency of 8.4 dBm and 7.2 % respectively. The simulated phase noise is -85 dBc/Hz at 10-MHz offset frequency in 300-GHz.

In Table II, the proposed VCO is compared to other InP technology VCOs operating around 300-GHz. This work achieves a high output power and high dc-to-RF efficiency due to differential-to-single combining.

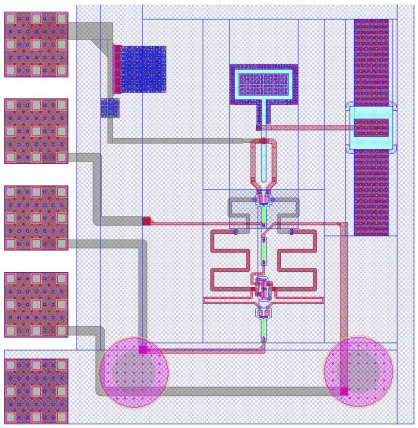


Fig. 13. Layout of the 300-GHz coupled-line VCO with slotline power combiner.

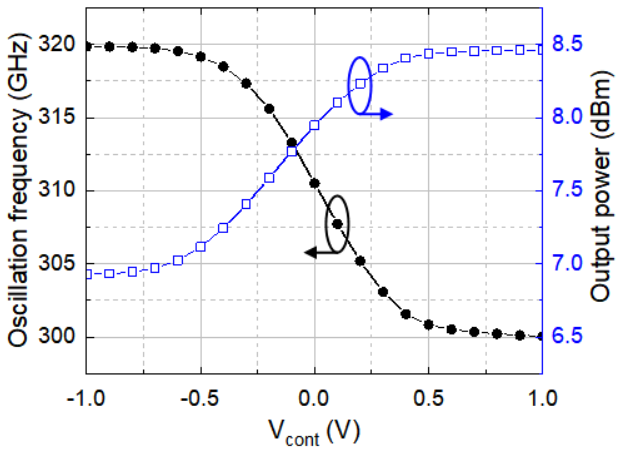


Fig. 14. Simulated oscillation frequency and output power of the VCO versus the varactor control voltage.

TABLE I. Performance Comparison with the state-of-the-art phase shifters in the 300-GHz band

Reference	Technology	Topology	Frequency (GHz)	Min. phase shift range (deg)	Average gain (dB)	P_{dc} (mW)	Size (mm^2)
[16]	0.13-μm SiGe	VSPS	220–250	360	-8 @ 235 GHz	105.6	–
[17]	250-nm InP	VSPS	220–320	360	-15.6 – -11.8	21.8–42	0.23
[18]	50-nm GaAs	RTPS	214–276	118	-7.8 – -7 **	0	0.25
This work*	**250-nm InP**	**RTPS+PI**	**255–305**	**360**	**-2.3 – 1.3**	**40.5**	**0.304**

*Simulation results, **Read from a plot in the article

TABLE II. Performance Comparison with Prior VCOs Operating Around 300-GHz

Reference	Technology	f_{osc} (GHz)	$P_{out,max}$(dBm)	Phase noise (dBc/Hz)	P_{dc}(mW)	DC-to-RF efficiency (%)
[10]	250-nm InP	298.1-316.1	4.8	-	88	3.43
[19]	250-nm InP	272.4-310.8	1.5	-96.4 @ 10 MHz	148	0.95
[20]	130-nm InP	294.9-304.8	4.7	-86.6 @ 10 MHz	75.6	3.9
This work*	**250-nm InP**	**300–320**	**8.4**	**-85 @ 10 MHz**	**72**	**7.2**

*Simulation results, **Read from a plot in the article

VI. CONCLUSION

A 300-GHz phase shifter and a high-power VCO are presented using a 250-nm InP HBT technology. The phase shifter adopts both reflection-type phase shifter and active switched-type phase shifter to achieve a full 360° phase shift range and compensate insertion loss. A two-stage common-base topology is employed to the active SPDT switch to provide gain. The phase shifter exhibits a continuous phase shift of 360° and a peak average gain of 1.3 dB at 285 GHz.

A coupled-line common-base cross-coupled topology is adopted to the VCO core in order to maximize the feedback loop gain from additional loss caused by via interconnections. A slotline power combiner is added to the output buffer to further increase the output power across the frequency range. The VCO generates a 300–320-GHz signal with a peak output power of 8.4 dBm and dc-to-RF efficiency of 7.2%. The proposed phase shifter and high power VCO are expected to be used for a phased-array system.

ACKNOWLEDGMENT

This work was supported by Institute of Information & communications Technology Planning & Evaluation (IITP) grant funded by the Korea government (MSIT) (No. 2021-0-00938, Development of THz band RF core component). The authors would like to thank the IC Design Education Center (IDEC), Korea for the chip fabrication and EDA tool support.

REFERENCES

[1] D. A. Johns and K. Martin, *Analog Integrated Circuit Design,* Jonh Wiley & Sons, p. 188, 1997.

[2] S. H. Jung, N. S. Jung, J. T. Hwang, and G. H. Gho, "An integrated CMOS DC-DC converter for battery-operated systems", *Power Electronics Specialists Conference*, *1999. PESC 99. 30th Annual IEEE*, vol. 1, no. 2, pp. 43, 47, Aug. 1999.

[3] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, Springer, 2001.

[4] Y. Kim, S. Kim, I. Lee, M. Urteaga and S. Jeon, "A 220–320-GHz Vector-Sum Phase Shifter Using Single Gilbert-Cell Structure with Lossy Output Matching," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 1, pp. 256-265, Jan. 2015.

[5] D. Müller, A. Tessmann, A. Leuther, T. Zwick and I. Kallfass, "A H-Band vector modulator MMIC for phase-shifting applications," *2015 IEEE MTT-S International Microwave Symposium*, 2015, pp. 1-4.

[6] D. Müller et al., "Bandwidth Optimization Method for Reflective-Type Phase Shifters," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 4, pp. 1754-1763, Apr. 2018.

[7] E. Kim and S. Jeon, "A Compact 275–320 GHz Reflection-type Phase Shifter," accepted to *IEEE Microwave and Wireless Components Letters*.

[8] *High-Pass Low-Pass Phase Shifters, Microwave101.com*, accessed on Nov. 2021. [Online]. Available: https://www.microwaves101.com/encyclopedias/high-pass-low-pass-phase-shifters.

[9] J. Kim et al., "Terahertz Signal Source and Receiver Operating Near 600 GHz and Their 3-D Imaging Application," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 5, pp. 2762-2775, May 2021.

[10] J. Yun, D. Yoon, H. Kim and J. Rieh, "300-GHz InP HBT Oscillators Based on Common-Base Cross-Coupled Topology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 12, pp. 3053-3064, Dec. 2014.

[11] J. Kim et al., "A Fully-Integrated High-Power Linear CMOS Power Amplifier with a Parallel-Series Combining Transformer," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 3, pp. 599-614, Mar. 2012.

[12] Y. Hsiao, Z. Tsai, H. Liao, J. Kao and H. Wang, "Millimeter-Wave CMOS Power Amplifiers with High Output Power and Wideband Performances," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 12, pp. 4520-4533, Dec. 2013.

[13] K. H. An et al., "Power-Combining Transformer Techniques for Fully-Integrated CMOS Power Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 5, pp. 1064-1075, May 2008.

[14] C. Wang and R. Han, "Dual-Terahertz-Comb Spectrometer on CMOS for Rapid, Wide-Range Gas Detection with Absolute Specificity," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3361-3372, Dec. 2017.

[15] X. Li et al., "A High-Efficiency 142–182-GHz SiGe BiCMOS Power Amplifier with Broadband Slotline-Based Power Combining Technique," *IEEE Journal of Solid-State Circuits*, vol. 57, no. 2, pp. 371-384, Feb. 2022.

[16] M. Elkhouly, S. Glisic, C. Meliani, F. Ellinger, and J. C. Scheytt, "220–250 GHz phased-array circuits in 0.13-μm SiGe BiCMOS technology," *IEEE Transactions on Microwave Theory and Techniques,* vol. 61, no. 8, pp. 3115–3127, Aug. 2013.

[17] Y. Kim, S. Kim, I. Lee, M. Urteaga and S. Jeon, "A 220–320-GHz Vector-Sum Phase Shifter Using Single Gilbert-Cell Structure with Lossy Output Matching," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 1, pp. 256-265, Jan. 2015.

[18] D. Müller et al., "Bandwidth Optimization Method for Reflective-Type Phase Shifters," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 4, pp. 1754-1763, Apr. 2018.

[19] D. Kim and S. Jeon, "A WR-3 Band Fundamental Voltage-Controlled Oscillator with a Wide Frequency Tuning Range and High Output Power," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 7, pp. 2759-2768, Jul. 2019.

[20] D. Kim and S. Jeon, "A 300-GHz High-Power High-Efficiency Voltage-Controlled Oscillator with Low Power Variation," *IEEE Microwave and Wireless Components Letters*, vol. 30, no. 5, pp. 496-499, May 2020.

Eun Jung Kim received the B.S. degrees in electrical engineering from Chungnam National University, Daejeon, Korea, in 2019, where she is currently working toward the Ph.D. degree in electrical and electronics engineering.

Her research interest includes mm-wave and THz circuits.

Hyun Joon Kim received the B.S. degree in electrical engineering from Kwangwoon University, Seoul, Korea, in 2021, where he is currently working toward the M.S. degree in electrical and electronics engineering.

His main interest includes mm-wave and THz circuits.

Sang Geun Jeon received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1997 and 1999, respectively, and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology (Caltech), Pasadena, CA, USA, in 2004 and 2006, respectively. From 1999 to 2002, he was a full-time Instructor in electronics engineering with the Korea Air Force Academy, Cheongju, South Korea. From 2006 to 2008, he was a Research Engineer, where he was involved with CMOS phased-array receiver design. Since 2008, he has been with the School of Electrical Engineering, Korea University, Seoul, where he is currently a Professor. His current research interests include integrated circuits and systems at microwave, mm-wave, and terahertz bands for high-speed wireless communications and high-resolution imaging applications.