A Wideband CMOS Down-conversion Mixer for 5G FR2 Applications

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***Abstract* – This paper presents a wideband complementary metal–oxide–semiconductor (CMOS) down-conversion mixer that supports a frequency range of 24−40 GHz. The proposed design is based on a double-balanced active mixer with wideband active and output baluns. In this design, the transconductance stage of the proposed mixer is composed of a parallel-connected common-gate and common-source amplifier structures for wideband input impedance matching and single-ended-to-differential signal conversion. The output active balun performs differential-to-single-ended conversion as well as a solid output impedance matching to drive a single-ended load of 50 Ω. The selected output intermediate frequency is 10 GHz. The proposed mixer is fabricated using a 65-nm CMOS process. Applying an external local oscillator input power of 5 dBm, the implemented design attains conversion gains of 3.87 dB and 1.5 dB, single sideband noise figures of 13.62 dB and 15.58 dB, input 1-dB compression points of −3.17 dBm and −0.87 dBm, and input referred third-order intercept points of 0.67 dBm and 3.74 dBm in the 28 GHz and 39 GHz bands, respectively. The implemented design consumes 9.75 mW with a nominal supply of 1.0 V. The active area, including pads, measures 0.87 mm × 0.46 mm (0.40 mm^2).**

***Keywords*—5G NR FR2, Active balun, CMOS, Down-conversion mixer, Millimeter-wave, Wideband**

I. INTRODUCTION

To handle the explosive increase of data traffic in mobile communications, the fifth generation (5G) new radio (NR) standard has been globally commercialized with enhanced data-rate and latency characteristics [1]. In particular, 5G frequency range 2 (FR2) bands offer a wide spectrum at the millimeter wave (mmWave) frequency; therefore, various phased-array receiver structures with steerable beam forming have been developed to improve the signal-to-noise ratio performance [2] [3]. However, the aforementioned 5G FR2 bands are allocated differently in each country. Therefore, considering the support of global roaming and frequency diversity, the straightforward phased-array radio frequency (RF) receiver architecture operating in each band (Fig. 1(a)) significantly increases the design complexity. This eventually incurs critical issues with respect to the cost and size of the mobile platform. To reduce the design complexity and cost, design blocks within the phased-array receiver must be designed with wideband characteristics supporting 5G FR2 bands, as depicted in Fig. 1(b). Specifically, a wideband down-conversion mixer in the receiver chain is highly required because only a single local oscillator (LO) generation circuitry that drives the mixer switches is necessary, leading to lower design complexity and power consumption of the receiver. However, the high propagation losses and parasitic components easily deteriorate the wideband mixer performance at mmWave frequencies.

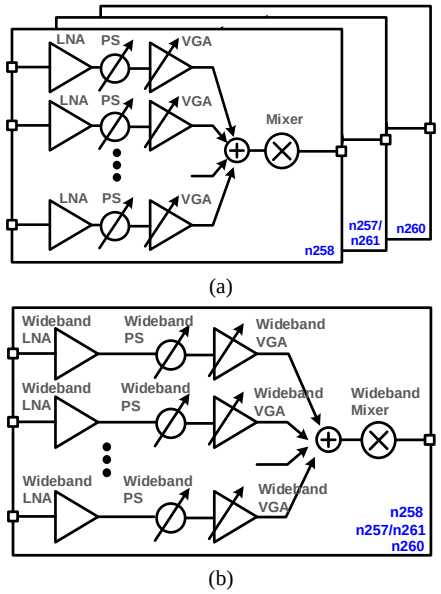

Fig. 1. Multi-band phased-array receiver (a) with narrowband-based blocks and (b) with wideband-based blocks [2], [3]

In this paper, we demonstrate a 24−40 GHz wideband complementary metal–oxide–semiconductor (CMOS) down-conversion mixer, supporting the 5G NR FR2 bands of n257 (26.5−29.5 GHz), n258 (24.25−27.5 GHz), n260 (37−40 GHz), and n261 (27.5−28.35). The applied active baluns at the input and output not only provide wide matching conditions but also maintain the benefits of the double-balanced mixing operation with improved isolation and linearity performance. The remainder of this article is organized as follows. Section II describes the proposed wideband double-balanced down-conversion mixer design with a brief discussion of the matching and gain performance. The experimental results of the implemented mixer design are presented in Section III. Finally, Section IV concludes the paper.

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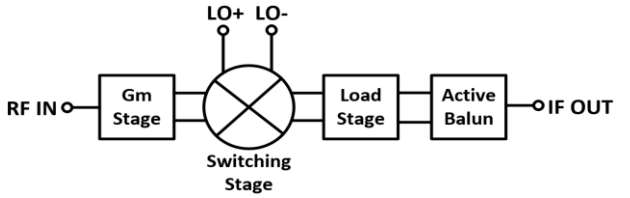
II. CIRCUIT DESIGN

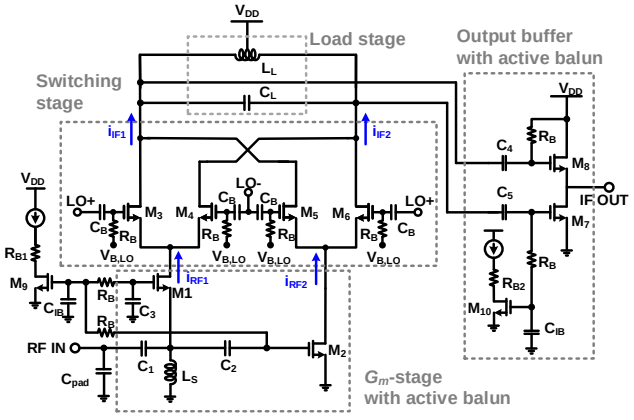
Fig. 1 shows the block diagram and schematic of the proposed wideband down-conversion mixer. The proposed mixer follows a double-balanced active mixer structure, which is composed of a tranconductance (G_m) active balun stage, mixer switching stage with an inductive load, and output balun buffer stage (Fig. 2(a)). For the G_m-stage, parallel-connected common-gate (CG) (M_1) and common-source (CS) (M_2) amplifiers offer wideband input matching and single-ended-to-differential signal conversion. Both M_1 and M_2 are biased through identical current replica circuitry so that the balanced differential output current signals are attained at the drain of the devices. According to the small-signal model of the mixer G_m-stage as shown in Fig. 3, the input impedance of the CG and CS input devices can be expressed as

$$Z_{IN}(s) = \frac{1}{sC_{gs1}} \| \frac{1}{g_{m1}} \| sL_S \| \frac{1}{sC_{gs2}} \| \frac{1}{sC_{PAD}} \quad (1)$$

where g_{mx} and C_{gsx} denote the transconductance and gate-source capacitance of the M_X, respectively, and C_{pad} is the parasitic shunt capacitance of the input pad. The value of L_S can be determined to resonate with the total capacitance



(a)



(b)

Fig. 2. Proposed wideband down-conversion mixer with active baluns; (a) block diagram and (b) schematic

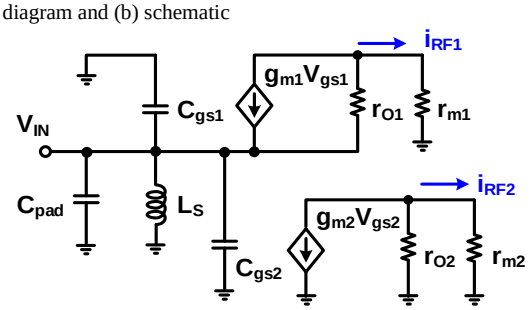


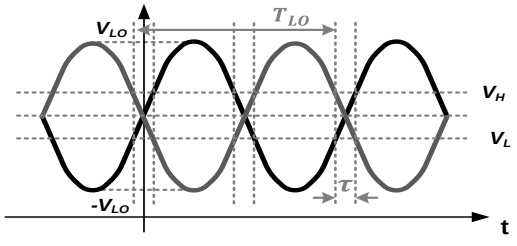
Fig. 3. Small-signal model of the mixer G_m-stage

given by C_{gs1}, C_{gs2} and C_{pad} with a low quality factor (Q-factor), resulting that Z_{IN} is maintained at $1/g_{m1}$ over a wide operating frequency range. Assuming $g_{m1}=g_{m2}=g_m$, $r_{o1}=r_{o2}=r_o$, and $r_{m1}=r_{m2}=r_m$ where r_{ox} and r_{mx} are the output impedance and impedance looking into the mixer switching stage at the drain of M_X, respectively, the differential transconductance gain of the mixer ($G_{m,diff}$) with the matching condition can be calculated as

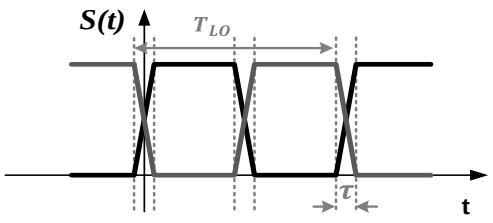
$$A_{G_{m,diff}} = \frac{i_{RF1} - i_{RF2}}{V_{IN}} = \frac{2g_m + 1/r_o}{1 + r_m/r_o} \quad (2)$$

Equation (2) indicates that as r_o increases, the gain tends toward $2g_m$ with improved balanced outputs. The double-balanced mixer switching stage, formed by M_{3-6} converts the RF signal to the intermediate frequency (IF). In this design, an IF of 10 GHz is chosen; therefore, the LO frequency, ranging from 14 to 30 GHz is appropriately selected according to the applied input RF signal frequency. In reality, the conversion gain of the mixer switching stage is largely determined by the amplitude of the LO signal at the gate of the switching devices [4], [5]. Fig. 4 shows the time-varying operations of the mixer switches with respect to the LO signal ($f_{LO}=1/T_{LO}$) and the output IF current. V_H and V_L are defined as threshold voltages, respectively, where mixer switches are completely turned on or off, and τ is the transit time of the switching operation. Therefore, as depicted in Fig. 4(b), the conversion current gain of the mixer switching stage can be modeled as the product of the differential RF currents ($i_{RF1}-i_{RF2}$) and the Fourier series representation of the differential switching operation, $S(t)$. Considering the finite τ, $S(t)$ can be given by

$$S(t) = \left(\frac{8}{\pi\omega_{LO}\tau}\sin\frac{\omega_{LO}\tau}{2}\right)\cos\omega_{LO}t - \left(\frac{8}{9\pi\omega_{LO}\tau}\sin\frac{3\omega_{LO}\tau}{2}\right)\cos 3\omega_{LO}t + \left(\frac{8}{25\pi\omega_{LO}\tau}\sin\frac{5\omega_{LO}\tau}{2}\right)\cos 5\omega_{LO}t + \cdots \quad (3)$$



(a)



(b)

Fig. 4. Time-varying operations of the mixer switches with respect to: (a) LO signal ($f_{LO} = 1/T_{LO}$), (b) output IF current

Hence, the current conversion gain of the mixer switching stage can be obtained by

$$A_{switch} = \frac{i_{IF1} - i_{IF2}}{i_{RF1} - i_{RF2}} = \frac{4}{\pi\omega_{LO}\tau} \sin\frac{\omega_{LO}\tau}{2} \quad (4)$$

According to (4), the conversion gain is a function of $f_{LO}\cdot\tau$ such that a smaller τ entails a higher conversion gain, which approaches 2/π. This indicates that the gain increase necessitates a large amplitude of the LO swing with extra power consumption. In the mixer load, the inductor (L_L) and capacitor (C_L) are utilized to be resonated at 10 GHz IF. The used L_L used retains the Q-factor of more than 20 to optimize the conversion gain and noise performance. Based on (2) and (3), the overall conversion gain of the mixer is given by

$$Gain|_{Mixer} = A_{G_m,diff} \cdot A_{switch} \cdot (1+Q_L) R_L \quad (5)$$

where Q_L and R_L denote the Q-factor of the load LC tank and series resistance of the L_L, respectively. The source-follower-type output active balun buffer stage is included only for test purpose, which offers differential-to-single-ended conversion and a solid output impedance matching for a load of 50 Ω. All the required electromagnetic simulations for the utilized routing paths and parasitic components were conducted using a Cadence EMX tool.

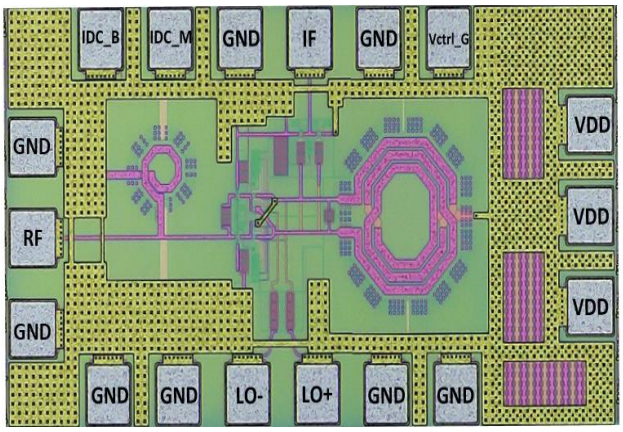


Fig 5. Chip microphotogragh of proposed mixer.

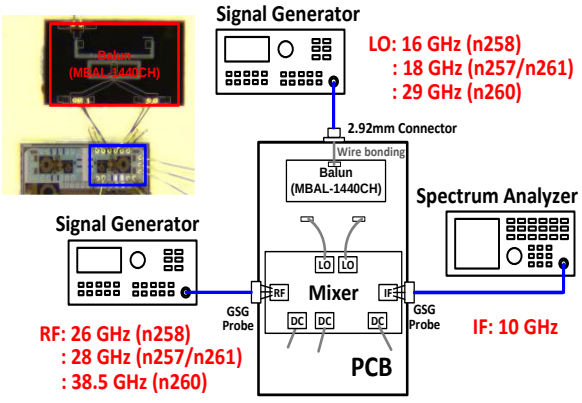


Fig 6. Chip measurement setup for the implemented mixer.

III. EXPERIMENTAL RESULTS

The proposed wideband CMOS down-conversion mixer for 5G NR FR2 applications was fabricated using a 65-nm CMOS technology. Fig. 5 shows the chip microphotograph of the implemented design whose active area, including pads, is 0.87 mm × 0.46 mm (0.40 mm^2). Fig. 6 shows the measurement setup for the implemented design. Signal path measurements were mainly performed using ground-signal-ground (GSG) RF and IF probes in a chip-on-board setup, and the related insertion loss of cables and probes utilized were appropriately compensated at the desired frequency. The required LO signal and bias controls were injected externally via wire bonding. A differential LO signal was generated using a separate die-type off-chip balun (MBAL-1440CH), which was in turn connected to the mixer through

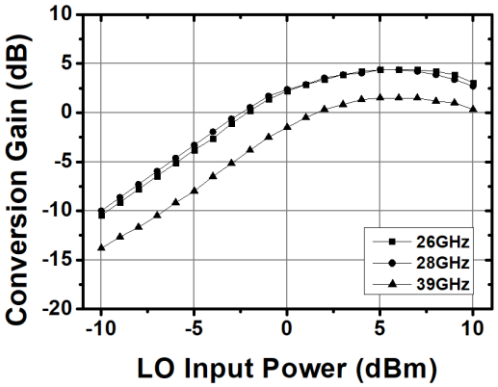


Fig. 7. Measured conversion gains versus LO input power.

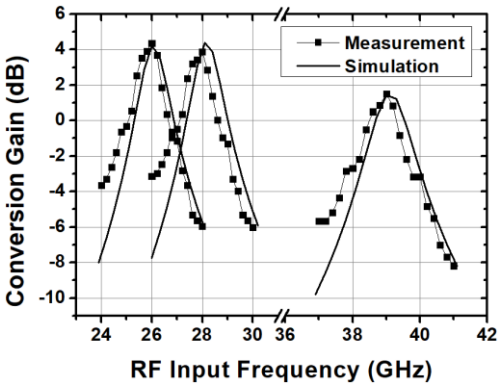
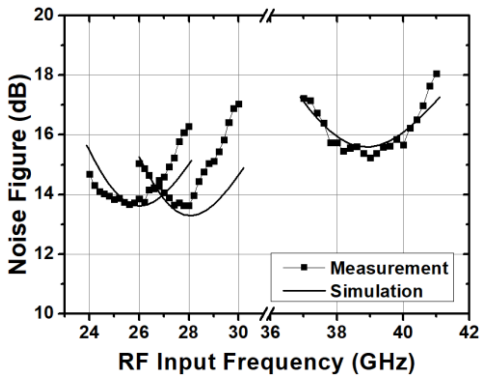


Fig. 8. Simulated and measured conversion gains versus operating frequencies (f_{IF}=10 GHz).



(b)

Fig. 9. Simulated and measured SSB noise figures versus RF input frequencies (f_{IF}=10 GHz)

wire bonding, as shown in Fig. 6. The LO power was set to +5 dBm at the output of the off-chip balun in terms of optimal gain and noise performance. All measurements were conducted at the center frequencies of the 5G FR2 n258, n257/n261, and n260 bands, which are 26 GHz, 28 GHz, and 39 GHz, respectively. The overall power consumption is 9.75 mW with a nominal supply of 1.0 V.

Fig. 7 shows the measured conversion gains versus the LO input power at the output of the off-chip balun. As can be seen, the maximum conversion gains are obtained with a P_{LO} of +5 dBm so that the rest of the mixer performance was evaluated with this P_{LO}. Fig. 8 and 9 show the simulated and measured results of the conversion gains and single sideband (SSB) noise figures (NFs) versus the RF input frequency, respectively. The obtained conversion gains are 4.37 dB, 3.87 dB and 1.5 dB in the 26 GHz, 28 GHz, 39 GHz bands, respectively, with a channel bandwidth greater than 800 MHz, and the attained SSB NFs are 13.6−15.5 dB. Both the conversion gains and NFs exhibits a design trade-off between performance and power consumption. To evaluate the linearity performance of the mixer, input 1-dB compression points (P1dBs) and input-referred third-order intercept points (IIP3s) were also characterized in the application of in-band one-tone and two-tone, respectively. The IIP3 performance is measured with two tones, f_1 and f_2 ($f_1 = f_{RF} + 10\ MHz$ and $f_2 = f_{RF} + 15\ MHz$). Fig. 10 shows the IP1dBs greater than -3.1 dBm and the IIP3s greater than 0.6 dBm at all operating frequencies. Fig. 11 shows the measured S11s and S22s of the proposed mixer at the RF and IF operating frequencies, respectively. As can be seen, utilized active baluns at the mixer input and output maintain the wideband matching characteristics with S11s of less than -12 dB and S22s of less than -16 dB at all corresponding operating frequencies. The measured performance metrics of the proposed mixer are summarized and compared with other state-of-the-art designs in Table I.

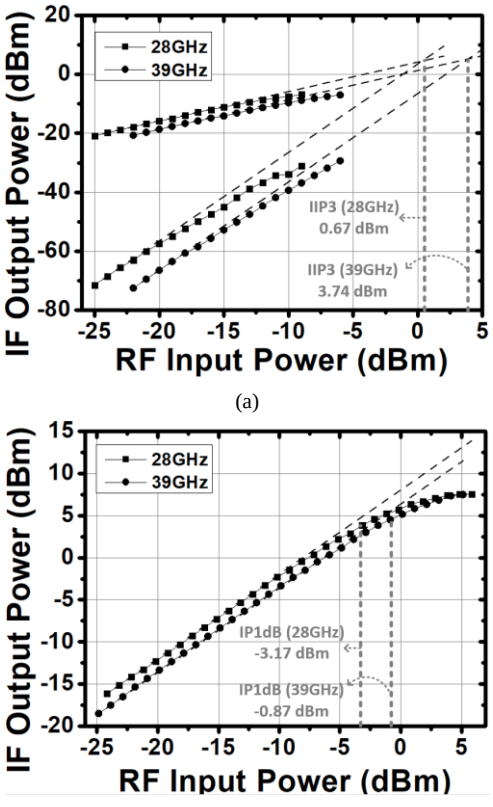


Fig. 10. (a) Measured fundamental and IM3 tones IF output power and (b) measured IF output power versus RF input power.

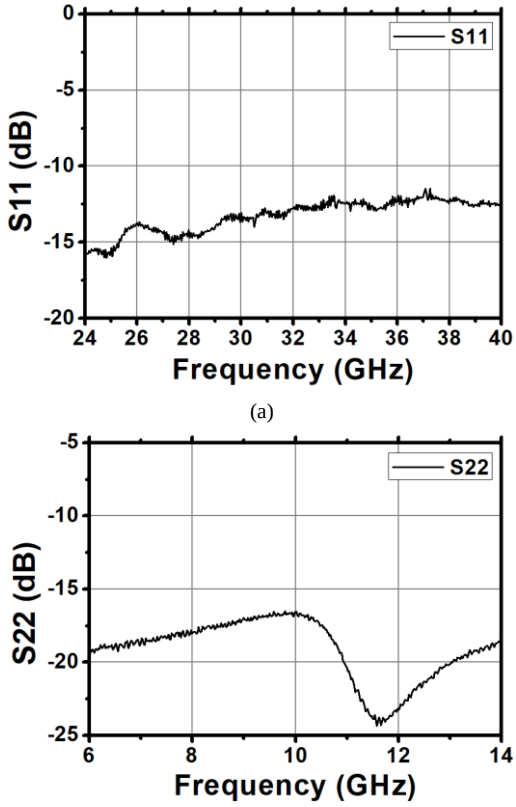


Fig. 11. Measured S-parameters (a) S11, (b) S22.

TABLE I. Comparison and Summary of Performance

Table	This work	[7]	[8]	[9]
Frequency (GHz)	26-39	26.5-29.5	26-34	20-50
Conversion Gain (dB)	4.37 (26G) 3.87 (28G) 1.5 (39G)	10.1	-2.6	0±2
NF (dB)	13.87 (26G) 13.62 (28G) 15.58 (39G)	9.9	13.5	16±0.5
LO Power (dBm)	5	-7	5	0
IIP3 (dBm)	0.67 (28G) 3.74 (39G)	9.2	0.5	9.5
Input P1dB (dBm)	-3.17 (28G) -0.87 (39G)	NA	NA	-1
Power (mW)	9.75	21	20	6
Technology	65nm CMOS	65nm CMOS	90nm SOI CMOS	90nm CMOS
Area (mm^2)	0.4*	0.28**	0.2*	0.49*

*with bonding pads NA: Not avaialble
**with LO buffer

IV. CONCLUSION

We present a CMOS down-conversion mixer that includes active baluns and wideband characteristics for 5G NR FR2 applications. By applying a low Q-factor shunt L_S matching, which resonates with the parasitic capacitance at the input, the parallel-connected CG and CS stages achieve wideband input matching characteristics. Similarly, source-follower output buffer stage offers solid output matching and differential-to-single-ended conversion. The demonstrated design achieves gain and linearity performance that are better than or comparable to other state-of-the-art mixer designs for the 24−40 GHz frequency band.

ACKNOWLEDGMENT

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