A 0.89 μV_{rms} Noise 93 dB High Dynamic Range Low Power 16 Channels Closed-Loop Neural Recording Chip

Jaeouk Cho[1], Janghwan Kim[2], Juntae Jang[1], Hongkyun Kim[1], and Chul Kim[a]

[1, a] Department of Bio and Brain Engineering, Korea Advanced Institute of Science and Technology

[2] Department of Electrical Engineering, Korea Advanced Institute of Science and Technology

E-mail : [1]jjo2883@kaist.ac.kr

***Abstract* - The closed-loop neural stimulation system's biggest concern is an artifact with more than tens of mV occurs due to stimulation. Previous studies have digitized the input signals through the analog-to-digital converter (ADC) after using amplifiers to measure tens of µV neural signals. Since the amplifier reduces the input range, the amplifier's output is saturated when a large stimulation artifact appears. This chip design uses the 2nd-order continuous delta-sigma modulator (DSM) to measure signals without saturation even if stimulation artifacts are entered with the neural signal. Overall, circuit structures were designed with a focus on stable operation even if a sudden large signal came in. Also, it can quickly track the sudden change of signals by adding an auto-ranging algorithm. We present 16 channel neural recording chip with a 65-nm CMOS process and the entire chip area is 1 mm^2 with 49µW power consumption. Input-referred integrated noise from dc to 500 Hz was 0.89 µV_{rms}, and more than 93 dB input dynamic range were guaranteed.**

***Keywords*—Analog-to-digital converter (ADC), Closed-loop neural recording, Delta-sigma modulator (DSM)**

I. INTRODUCTION

Diverse structures have been proposed over the past decades to measure tens of µV neural signals. Among them, the most famous structure is composed of the high gain amplifier with low-resolution ADC [1]-[4]. Neural signals are amplified to the tens of mV range and digitized by the ADC with low resolution. Meanwhile, numerous recent structures intend to use extremely low supply voltages to drive circuits with low power [5]. Thus, the input range of the recording system gets smaller when using the amplifier. In the closed-loop neural recording system, electrical stimulation artifacts are measured together with neural signals. This makes it impossible to measure the neural signal by saturating the output of the amplifier during the stimulation phase [6]. Moreover, when the input signal passes the amplifier, distortion and noise are included which also deteriorates the performance of the output signal. Thus, the structure using the amplifier is not appropriate for the closed-loop neural recording system.

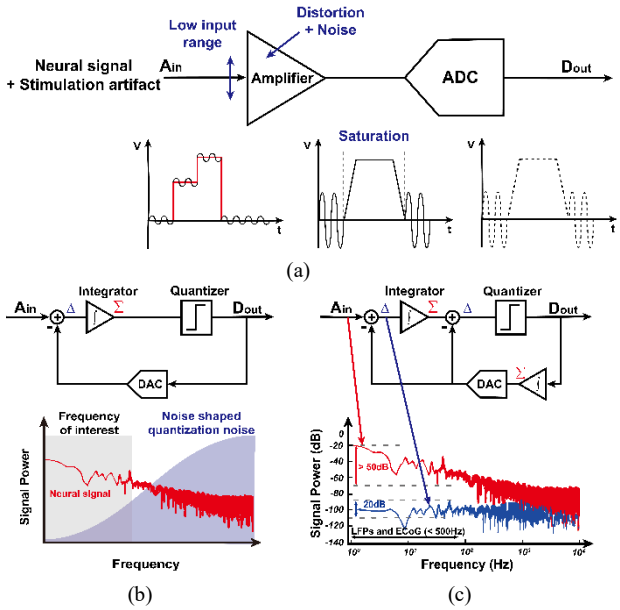


Fig. 1. Previous neural recording structures; (a) Low noise amplifier with low resolution ADC [1], [2] (b) Conventional DSM structure and (c) DSM structure with feedback integrator [7].

In order to digitize a signal without using an amplifier, the quantization noise (Q-noise) level of the ADC must be smaller than the neural signal. ADCs with high resolution or methods that can reduce the size of the Q-noise itself should be used to record neural signals. High-resolution ADC is one way to reduce the Q-noise, but it requires a lot of power and area which is not preferred in the closed-loop system. DSM ADCs can be another solution to reduce in-band Q-noise through noise-shaping characteristics. Especially, continuous-time DSM ADCs have an intrinsic anti-aliasing filtering effect. Because the sampling is conducted behind the integrator which acts as a low-pass filter.

Linearity is one of the important factors in the recording system which is directly related to the harmonics in the output signal. Due to the nonlinearity characteristic of MOSFET, the linearity problem gets more serious as the input signal increases. The feedback path integrator restores the input signal as shown in Fig. 1(c) to lessen the integrator's input [7]. Even if the input signal requires more than 50 dB dynamic range (DR), the required integrator's DR can be reduced to 20 dB by using this structure.

a. Corresponding author; kimchul@kaist.ac.kr

Manuscript Received Feb. 17, 2022, Revised Jun. 23, 2022 & Dec. 21, 2022, Accepted Dec. 29, 2022

This is an Open Access article distributed under the terms of the Creative Commons Attribution Non-Commercial License (http://creativecommons.org/licenses/bync/3.0) which permits unrestricted non-commercial use, distribution, and reproduction in any medium, provided the original work is properly cited.

The output of DSM can be calculated by integrating the result of the quantizer. Previous studies usually use a 1-bit quantizer to simplify the structure and increase the linearity. Thus, if a large sudden signal, such as a stimulation artifact, enters, the system cannot quickly track the signal because of the constant update size of the 1-bit quantizer. The update size of the 1-bit quantizer's output has a trade-off between the speed of tracking the signal and the resolution. This problem can be solved by using a multi-bit quantizer instead of a 1-bit quantizer. However, when a multibit quantizer is used, the linearity of the quantizer itself is getting lower [8].

This paper is an improved version of [9]. We increase the supply voltage to solve the channel stability issue. Also, we redesign the integrator to improve the noise characteristics. The overall structure is the 2nd-order continuous DSM structure for ECoG closed-loop neural recording applications. To make the variable update size depending on the input signal, we changed the updated amount of the 1-bit quantizer bit following the input signal. This structure can achieve the intrinsic linearity of the 1-bit quantizer while obtaining the effect of the multi-bit quantizer.

II. DESIGN AND EXPERIMENTS

A. Circuit design and implementation

Fig. 2. shows the overall circuit architecture of 16 channel neural recording structure. Each channel uses the 2nd-order DSM structure, and it predicts an input signal through a 12-bit capacitive bridge DAC. The feedback path restores the input signals using digital integrators which are composed of the up/down counter. Only the difference in the input signal enters the feedforward integrator. Also, it can track input signals faster by using a variable up/down counter that can change the size of a 1-bit quantizer.

The capacitive sensing structure is used in this design and the common mode of the input terminal is defined through a switch connected to the V_{CM}. The leakage current through the switch can make a serious noise due to the high input impedance node of this system. Therefore, to minimize the leakage current, the switch was designed to have a resistance of about several hundred TΩ when the switch is turned off.

When the input signal passes through the amplifier, the noise from the amplifier is added to the signal. Noise from the amplifier must be minimized to maintain high SNR signal. In a multistage amplifier, noise generated by the back-end amplifier is divided by the gain of the front-end amplifier. Thus, the input-referred noise of the amplifier is mainly determined by the first stage. Fig. 3. shows a simplified version of the 1st stage amplifier to examine the noise generated in the amplifier. In this structure, since flicker noise was removed using the chopping structure, only the thermal noise of the MOSFET is considered and analyzed. The noise of the MOSFET can be expressed as V_{ni}, which is calculated as (1). C_f represents the capacitance viewed toward the capacitive DAC and C_{gs} is the parasitic capacitance between the gate and source of the transistor, which depends on the width (W), overlap capacitance, and oxide capacitance [10]. As shown in (1), the noise created by the MOSFET decreases as the g_m value increases, so as the W/L value increases, the noise decreases. On the other hand,

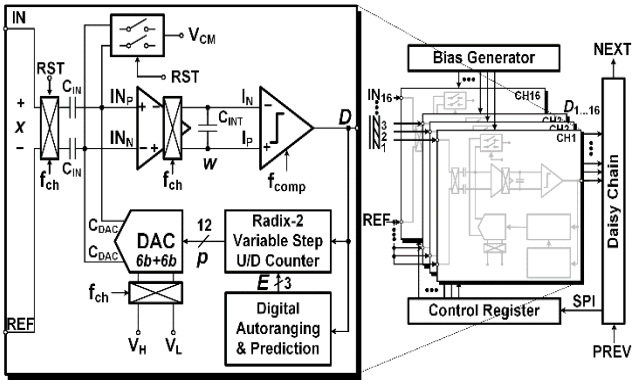


Fig. 2. Entire 16 channel circuit implementation and detailed one channel circuit diagram [11].

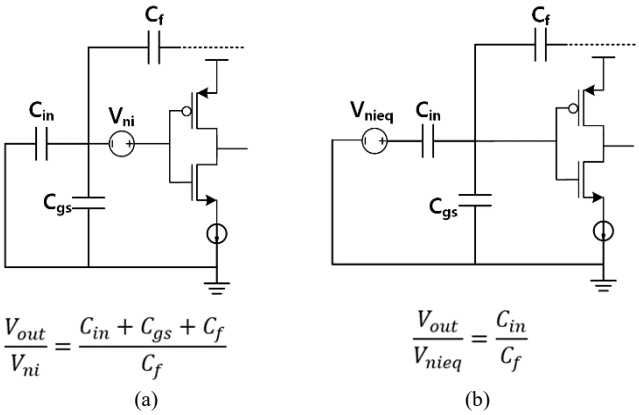


Fig. 3. Simplified capacitive sensing structure; (a) Input referred noise of the amplifier and (b) input transferred noise modeling.

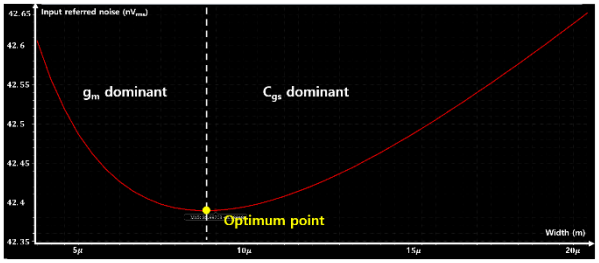


Fig. 4. Cadence simulation result of integrated amplifier's input-referred noise from dc to 500 Hz. It represents the noise according to the width of the amplifier

$$V_{ni}^2 = \frac{8kT}{3}\frac{1}{g_{mn}+g_{mp}} \quad (1)$$

$$g_m = 2K_n\frac{W}{L}(V_{gs} - V_T) \quad (2)$$

$$V_{nieq}^2 = \frac{(C_{in}+C_f+u\cdot W)^2}{C_{in}^2}\frac{L}{W}\frac{8kT}{3}\frac{1}{2K_n(V_{GS}-V_T)} \quad (3)$$

the C_{gs} value increases as the length (L) and width (W) increase and it causes a problem in the capacitive sensing structure. Fig. 3(b) represents the noise transferred to the input terminal and it can be described as (3). Since W and C_{gs} have a linear relationship, the relationship between C_{gs} and W was simplified u·W to see the effect of W in the V_{nieq} [10]. If u·W is smaller than the C_f and C_{in}, the V_{nieq} value becomes smaller when the W is increased. However, u·W

becomes

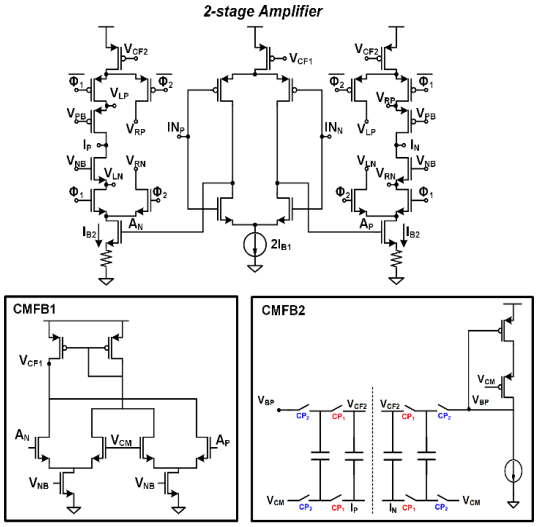


Fig. 5. Designed 2-stage amplifier with different CMFB structures.

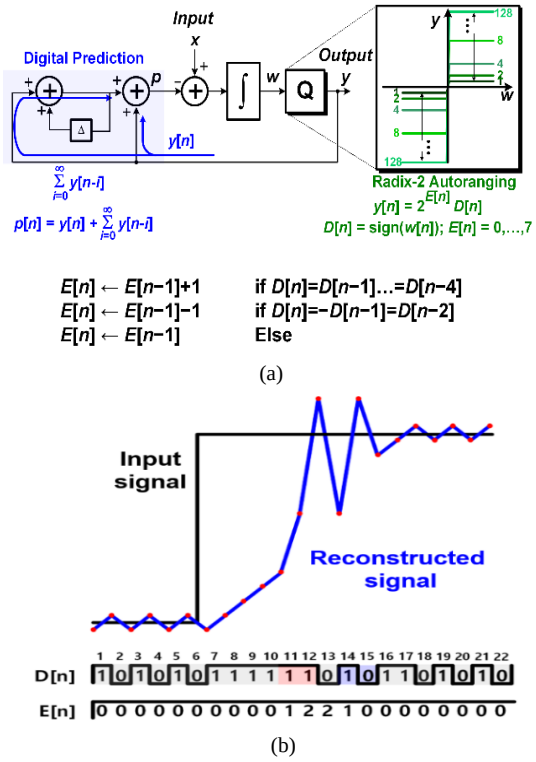


Fig. 6. Proposed auto-ranging structure; (a) Algorithm of auto-ranging and (b) example of an algorithm of auto-ranging.

similar to C_f and C_{in}, the V_{nieq} increases according to the W. Thus, it is necessary to optimize input noise by adjusting the W. Fig. 4. shows the plot of the input noise according to width through cadence simulation, and the design was performed according to the optimal point shown in the figure.

Fig. 5. represents the structure of the 2-stage amplifier. The current source used in the 2nd stage amplifier could be designed as a resistor or current mirror. When using the current mirror as a current source it could be a more stable structure than using a resistor. However, it cannot supply a current variably when a sudden change of signal enters the input. Thus, a resistance that operates well in a more variable environment is adopted as a current source.

The common-mode feedback (CMFB) in the 1st and 2nd stage amplifiers are designed differently. The CMFB of the 1st stage has a differential amplifying structure while the 2nd stage CMFB is accomplished by switched capacitor structure. As the amplified signal enters the 2nd stage of CMFB, a linearity issue would arise when using differential amplifying CMFB. Thus, we choose the switched capacitor CMFB as the 2nd stage CMFB.

In this study, we present auto-ranging algorithms to update the 1-bit quantizer size variably by using the previous signal. The algorithm of auto-ranging is illustrated in Fig. 6(a). The y[n] is the feedback value and can be calculated by 2 to the power of E[n]. The E[n] represents the update size and may increase from 0 to 7. The update size is determined by the result of the previous comparator's output sign which is stored in the D flip-flop. The previous five comparator results are stacked in the D flip-flop and determine the E[n] value. D[n] should have a positive sign more than five times to increase the E[n]. When the large signal comes in, E[n] changes at least after five samples. After that, if the next D[n] is still the same as D[n-1], the value of E[n] increases for each sampling period to quickly catch up with the signal. However, if the D[n] changes 1 and 0 consecutively, this means that the reconstructed signal already followed the input value as shown in Fig. 6(b). To increase the resolution of the signal, E[n] is reduced if the D[n] changes 1 and 0 consecutively more than three times. The purpose of this algorithm is to make E[n] change only when a large signal is entered, maintaining the highest resolution. Fig. 6(b) illustrates an example of a signal restored according to an input signal. When a sudden large input signal comes in, the step size increase, and if the restored signal has a similar value to the input signal, the step size decreases again to have a higher resolution.

B. Measurements

Fig. 7. is a measurement environment for verifying the performance of the designed integrated circuit. The designed chip was directly connected to the printed circuit board (PCB), and the signal generated by the signal generator (APX526) was configured to enter each channel through the chip pad. Power and clock signals are supplied through a field programmable gate array (FPGA), and signals from the chip are processed through the FPGA and MATLAB. The input current was 50 nA, and the 15.6, 31.25, and 62.5 kHz clock signals were used as the sampling frequencies and chopping frequencies.

Fig. 8(a) shows the reconstructed 16-channel results through MATLAB when the sampling frequency and chopping frequency are used as 31.25 kHz. It can be seen that all 16 channels operate well when the input signal was a 1 Hz sine signal of 7.24 mV_{pp}. Fig. 8(b) represents 1 channel′s fast Fourier transform (FFT) result and the 63.4 dB spurious-free dynamic range (SFDR) was calculated. The signal-to-noise distortion ratio (SNDR) results with various inputs are shown in Fig. 9. As shown in the figure, if the signal's amplitude goes beyond -30dBV the SNDR does not increase anymore. Because the auto-ranging function is

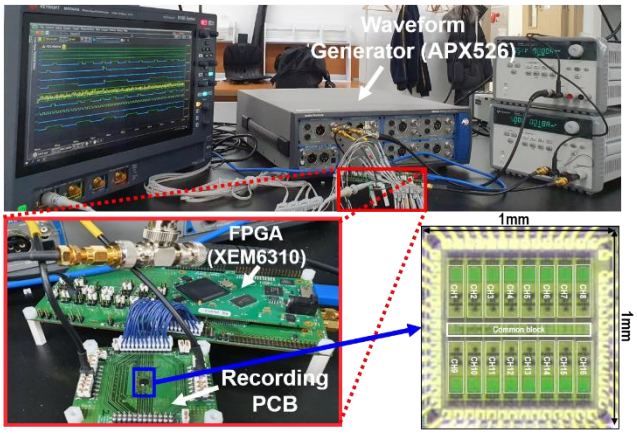
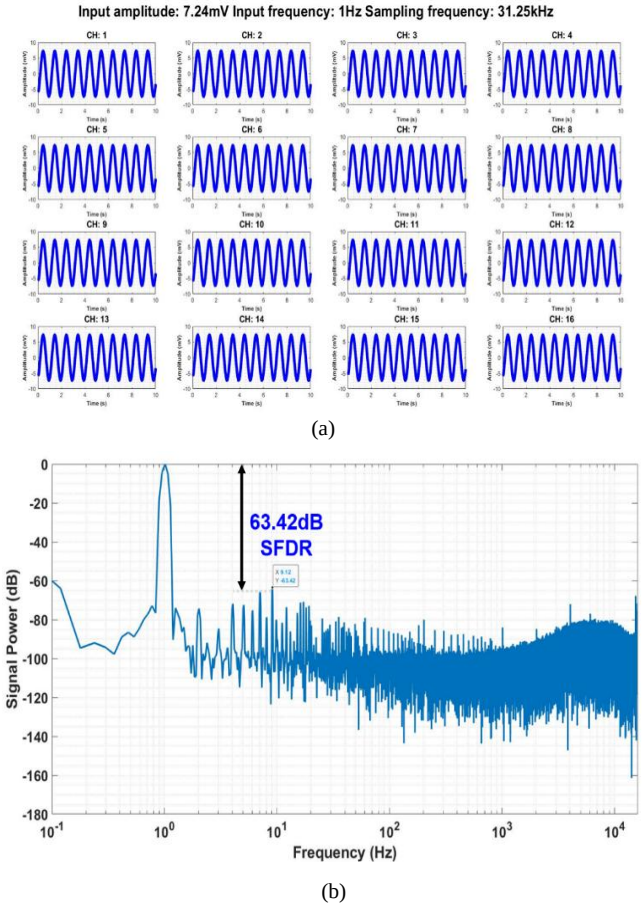


Fig. 7. Environmental configuration for the designed chip measurement.



(a)

(b)

Fig. 8. Recorded signal using the designed chip. (a) Reconstructed 16 channel signals using MATLAB and (b) FFT result of the recorded signal

activated to increase the size of the 1-bit quantizer, degraded output resolution.

As the frequency of the input signal increases, the change amount per unit of time increases, and as a result, the auto-ranging function works even on a small amplitude. Thus, the output signal's SNDR decrease in the high-frequency signal. In Fig. 9. if the signal's frequency goes over 500 Hz, the SNDR of the large amplitude signal is lowered as shown in the graph. However, when measuring a neural signal having less than a few μV, it operates without SNDR reduction. Also, if we increase the sampling frequency we can increase SNDR even high-frequency signals come in.

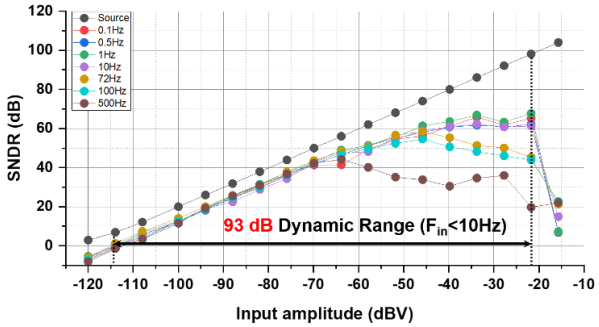


Fig. 9. SNDR result according to the amplitude and frequency of the input signals.

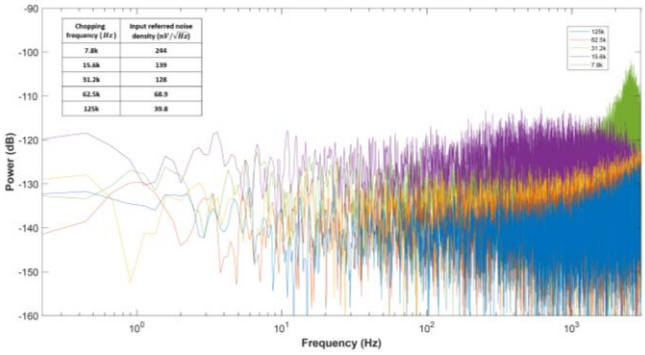
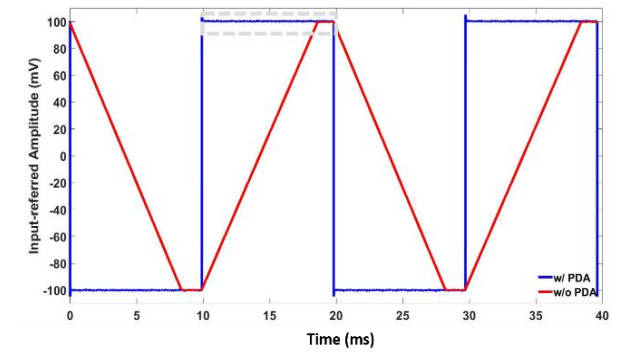


Fig. 10. Input referred noise according to the chopping noise.

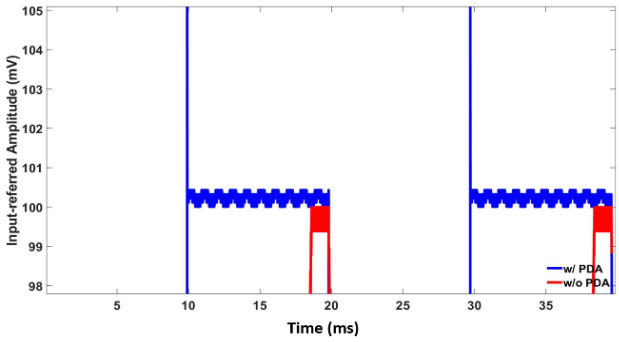
The dynamic range was measured to be 93 dB, which is sufficient performance in recording the neural signal and the stimulation artifacts together. The noise performance according to the chopping frequency is shown in Fig. 10. This result indicates input referred noise according to the chopping frequency when the sampling frequency is 31.2 kHz. It can be seen that overall input referred noise decreases by increasing the chopping frequency. This is because the amount of flicker noise entering the frequency of interest decreases as the chopping frequency increases. To see the performance of the auto-ranging, a 500μV_{pp} sine signal was given with a 100mV_{pp} square signal as an input. As shown in Fig. 11., a waveform that gives a 200mV square signal and a 100μV sine signal at the same time was given as an input to determine whether a neural signal can be measured with a sudden large artifact. Without auto-ranging, the update speed cannot quickly follow the input signal. On the other hand, when using auto-ranging, the system can track a large signal at high speed. After following the square waveform, the sine input signal can be tracked at high resolution with a small update size. Overall tolerable artifact amplitude was measured as ±130 mV.

III. CONCLUSION

In this circuit design, a measurement system that can operate in a closed-loop stimulation system was implemented using a 65 nm CMOS process with a 2nd-order DSM structure. The entire system consists of 16 channels, with a total area of 1 mm^2 and a power consumption of 49 μW. The performance of the circuit has a high dynamic input range of more than 93 dB and has an input referred noise of 0.89 μV_{rms} when chopping



(a)



(b)

Fig. 11. Reconstructed result in which square waveforms and sine waves are combined into input signals without auto-ranging and with auto-ranging.

frequency is 125 kHz. Input referred noise was measured 0.1Hz to 500Hz, which is the frequency band of the ECoG signal. Overall chip performance and comparison table are summarized in Table I. This structure is implemented to be used for closed-loop neural recording by having a high dynamic range and low input referred noise.

TABLE I. Performance Comparison

Performance	This work	[12]	[11]
Process	65nm CMOS	180nm CMOS	40nm CMOS
Supply voltage (V)	1	1	1.2
Power/Ch (μW)	3.06.	6.5	7.3
Input referred noise (nV/√Hz)	39.8	265.6	127
Dynamic range (dB)	93	92.3	90
ENOB (bits)	10.6	13.7	13.3

ACKNOWLEDGMENT

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) (No.2020R1C1C1009878) and has been supported by the ETRI (Electronics and Telecommunications Research Institute)'s internal funds. [21YR2500, Development of Digital Biopsy Core Technology for high-precision Diagnosis and Therapy of Senile Disease]. The chip fabrication was supported by the IC Design Education Center (IDEC), Korea.

REFERENCES

[1] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 958-965, Jun. 2003.

[2] R. R. Harrison et al., "A Low-Power Integrated Circuit for a Wireless 100-Electrode Neural Recording System," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 1, pp. 123-133, Jan. 2007.

[3] D. Han, Y. Zheng, R. Rajkumar, G. S. Dawe and M. Je, " A 0.45 V 100-Channel Neural-Recording IC With Sub-μW/Channel Consumption in 0.18μm CMOS," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 7, no. 6, pp. 735-746, Dec. 2013.

[4] S. Lee et al., "A 110dB-CMRR 100dB-PSRR multi-channel neural-recording amplifier system using differentially regulated rejection ratio enhancement in 0.18μm CMOS," *2018 IEEE International Solid - State Circuits Conference (ISSCC)*, 2018, pp. 472-474.

[5] F. M. Yaul and A. P. Chandrakasan, "A sub-μW 36nV/√Hz chopper amplifier for sensors using a noise-efficient inverter-based 0.2V-supply input stage," *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, 2016, pp. 94-95.

[6] Cho, Jaeouk et al. "Energy-Efficient Integrated Circuit Solutions Toward Miniaturized Closed-Loop Neural Interface Systems," *Frontiers in neuroscience*, 15: 667447, May. 2021.

[7] M. Reza Pazhouhandeh, M. Chang, T. A. Valiante and R. Genov, "Track-and-Zoom Neural Analog-to-Digital Converter with Blind Stimulation Artifact Rejection," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 7, pp. 1984-1997, Jul. 2020.

[8] B. Razavi, "The Delta-Sigma Modulator [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 8, no. 2, pp. 10-15.

[9] Sansen, Willy M. Analog design essentials. Vol. 859. Springer Science & Business Media, 2007, pp. 117–147.

[10] C. Kim, S. Joshi, H. Courellis, J. Wang, C. Miller and G. Cauwenberghs, "Sub- μW Vrms-Noise Sub- μW /Channel ADC-Direct Neural Recording With 200-mV/ms Transient Recovery Through Predictive Digital Autoranging," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 11, pp. 3101-3110.

[11] H. Chandrakumar and D. Markovic, "A 15.2-enob continuous-time ΔΣ adc for a 7.3 μW 200mvpp-linear-input-range neural recording front-end," *2018 IEEE International Solid - State Circuits Conference (ISSCC)*, 2018, pp. 232-234.

[12] J. -S. Bang, H. Jeon, M. Je and G. -H. Cho, "6.5μW 92.3DB-DR Biopotential-Recording Front-End with 360MVPP Linear Input Range," *2018 IEEE Symposium on VLSI Circuits*, 2018, pp. 239-240.

Jae Ouk Cho (Student Member, IEEE) received the B.S. degree in biomedical engineering from Hanyang University, Seoul, Korea, in 2019, and the M.S degree in bio and brain engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea in 2021. Currently, he is working toward Ph.D. degree in bio and brain engineering at KAIST, Daejeon, Korea. His research interests include Neural recording IC and implantable biomedical devices.

Jang Hwan Kim (Student Member, IEEE) received the B.S. degree in biomedical engineering from Korea University, Seoul, South Korea, in 2021, and is currently pursuing the M.S. degree in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea. His research interests include the design and development of retinal prostheses as well as power-efficient neural stimulators with special focus on mixed signal circuits.

Jun Tae Jang (Student Member, IEEE) received the B.S. degree in electrical engineering from Hanyang University, Seoul, Korea, in 2020. Currently, he is working toward M.S. degree in bio and brain engineering at KAIST, Daejeon, Korea. His research interests include Ultrasonic wireless power transfer system and power management ICs.

Hong Kyun Kim (Student Member, IEEE) received the B.S. degree in electrical engineering from Kyunghee University, Suwon, Korea, in 2016, and the M.S. degree from the Graduate School for Green Transportation Engineering, Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 2018. Currently, he is working toward Ph.D. degree in bio and brain engineering at KAIST, Daejeon, Korea. His research interests include wireless power transfer system and power management ICs.

Chul Kim (Senior Member, IEEE) is an assistant professor in the Department of Bio and Brain Engineering and the Program of Brain and Cognitive Engineering at Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea. He received the Ph.D. degree in 2017 from bioengineering, UC San Diego, La Jolla, CA, USA, where he was a postdoctoral fellow from 2017 to 2019. From 2009 to 2012, he was with SK HYNIX, Icheon, South Korea, where he designed power management circuitry for dynamic random-access memory. His current research interests include design of energy-efficient integrated circuits and systems for fully wireless brain-machine interfaces and unobtrusive wearable sensors.

He received a Gold Prize in the 16th Humantech Thesis Prize Contest from Samsung Electronics, Suwon, South Korea, in 2010, and the 2018 Shunichi Usami Ph.D. Thesis Design Award from the Bioengineering Department, UC San Diego. He was the recipient of a 2017, 2018 IEEE Solid-State Circuits Society Predoctoral Achievement Award. He served as a guest editor of IEEE Transactions on Biomedical Circuits and Systems (TBioCAS) for the special issue of ISCAS2020. Since 2020, he has served as an associate editor of TBioCAS, and as a technical program committee for IEEE Custom Integrated Circuits Conference (CICC). Prof. Kim is the co-editor of High-density integrated electrocortical neural interfaces: Low-noise low-power system-on-chip design methodology (Academic Press, 2019).