Ultra-Wideband Pulse Generator with Simultaneous Optimization of Sidelobe Suppression and Essential Bandwidth

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***Abstract* - Impulse-radio ultra-wideband signaling is being widely used in small-distance, low-power, and low-cost applications such as wireless sensor networks (WSN) and wireless personal area networks (WPAN). This paper presents an on-off keying-driven impulse radio ultra-wideband pulse generator aimed at wireless-powered applications. The proposed impulse-radio ultra-wideband pulse generator is built upon a pseudo-digital architecture, with the core cell being implemented using digital gates to achieve the desired timing delay. To eliminate the need for an external pulse-shaping filter, a pulse-shaping scheme based on the power transistor sizing technique is exploited to generate a broadband pulse with triangular envelope; ensuring enhanced sidelobe suppression in compliance with the FCC spectral mask for UWB communications and extended signal bandwidth to utilize the given spectrum more efficiently. The prototype pulse generator is implemented in 65-nm RF CMOS technology with TSMC 65nm GP process. The measurement results show an energy consumption of 34-pJ/pulse with a pulse amplitude of 580-mVpp, a 10-dB bandwidth of 1.14 GHz, and more than 30-dB sidelobe suppression in the DC-2.8 GHz band.**

***Keywords*—Impulse Radio (IR), pulse generator (PG), sidelobe suppression, ultra-wideband (UWB)**

I. INTRODUCTION

Impulse Radio Ultra-Wideband (UWB) transceivers have been an intense area of research since the Federal Communication Commission (FCC) issued a large 7.5 GHz band (3.1-10.6 GHz) for unlicensed spectrum utilization. IR-UWB is a promising technology for high data rate communication and allows definite localization and positioning capabilities along with low power spectral density and very low effective isotropic radiated power (EIRP) levels [1].

The FCC spectral mask for UWB communication maintains a maximum EIRP level of the transmitted pulse below -41.3 dBm per 1MHz resolution bandwidth in DC-960 MHz and 3.1-10.6 GHz. From 0.96-3.1 GHz, different emission levels have been specified for both indoor and outdoor communications to avoid the interference of generated pulse with already present standards (e.g., Wi-Fi at 2.4 GHz), with the most important being the band from 960 MHz to 1.61 GHz and the edge of spectral mask at 3.1 GHz, where the signal level must be 34 dB and 20 dB lower as compared to the maximum allowed EIRP level, respectively, for outdoor communication [1].

The amount of sidelobe suppression required to meet the spectral mask depends on the shape of the pulse. The UWB pulse with a rectangular envelope is only able to provide 13 dB of first sidelobe suppression as compared to the pulse frequency. Hence, an extra filter [2], [3], or some other pulse shaping scheme [4] is required to lower the side-signal level. The triangular envelope, however, provides better suppression, with the first sidelobe being 26 dB lower than the pulse center frequency [5], which is a significant improvement over the rectangular shaping. Alternatively, it can be stated that the triangular shaping possesses inherent band-pass filtering characteristics, which helps eliminate the use of external filters.

Generally, three distinct approaches are adopted to obtain a UWB pulse with the desired characteristics: high-order filtering [6], mixing [7], and edge combination [8]. In the filtering technique, the signal from the pulse generator is delivered to the output through a pulse-shaping filter to meet the spectral regulations. The spectrum mixing approach is similar to the traditional narrowband transmitter and consists of a local oscillator (LO) and a mixer. Both filtering and mixing techniques demand a large on-chip area to accommodate the passive components. The edge-combination approach utilizes delay lines (DL) to generate a UWB pulse to generate a UWB pulse by combining multiple Gaussian monocycles. The propagation delay of an inverter-based DL governs the width of the Gaussian monocycle, and the cascade of such DLs can be utilized to generate a high-order UWB pulse with the shape of the envelope being controlled by the output pulse driver.

In this work, we take a mathematical approach to pulse-shaping envelopes while comparing them in terms of sidelobe suppression and essential bandwidth. The

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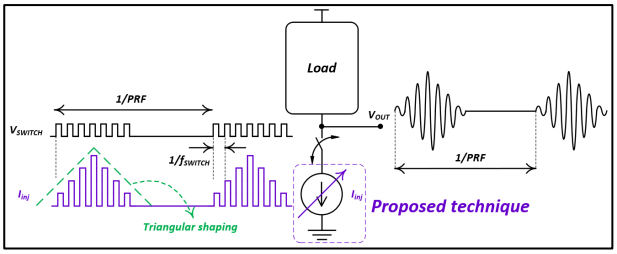

Fig. 1. Schematic illustration of the proposed pulse generator

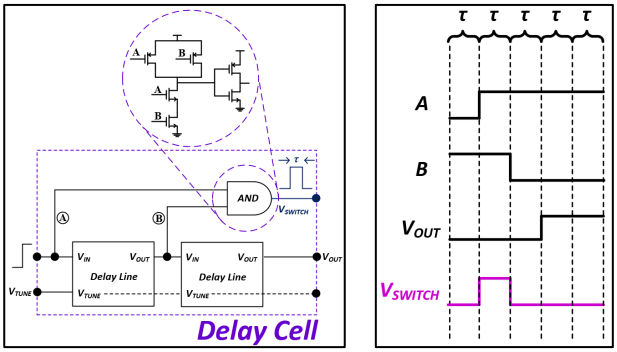

Fig. 2. Schematic of the delay cell implementation and its timing diagram

implementation of the triangular-shaped UWB pulse generator using a pseudo-digital, edge-combination technique along with power transistor scaling improves the sidelobe suppression and essential bandwidth simultaneously. The RLC tank approximating the Gaussian mono-cycle obviates the need of the impedance matching network. In terms of the essential bandwidth, data rate, and the interference rejection, the proposed architecture and its simulation results outperform the previous works [5], [9], [10].

II. PROPOSED UWB PULSE GENERATOR

Fig. 1 shows the proposed pulse generator fundamental with schematic illustration, in which the triangular enveloped pulse is generated by controlling the amount of oscillation amplitude of LC tank through a trans-conductor, G_m, where G_m consists of multiple transistors in pareallel, each having a linearly varying trans-conductance. Each of the individual digital gates in the square wave at the input G_m stage are generated through a cascade of inverter based delay lines (DLs). By tuning the propagation delay through a DL and the oscillation frequency of LC tank, a UWB pulse with the desired triangular shape can be achieved.

The pulse generation scheme described in Fig. 1 can be best explained by analyzing the properties of an LC tank, with the most important being the quality factor, which determines the effective pulse width (and hence, the bandwidth), and the output matching.

Multiple rectangular pulses are generated by cascaded delay cells. Then, Fig. 2 shows the delay cell implementation and its timing diagram to realize the V_{switch}, which is the single rectangular pulse with ON duration, τ. The NMOS devices in the AND gate have been strengthened by two times to support the transition from 11 to 10 or 01.

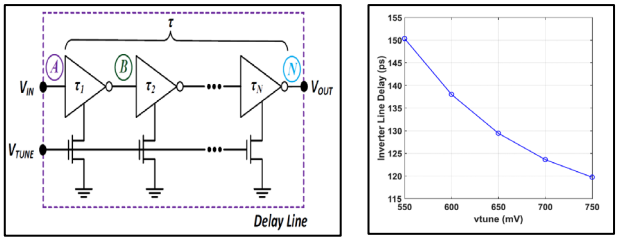

Fig. 3. Schematic of the delay line (left) and simulated timing delay as the function of the tuning voltage

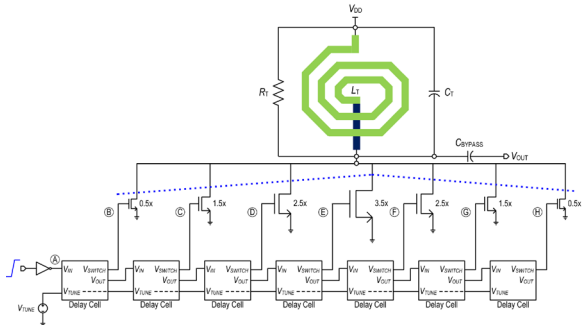

Fig. 4. Full schematic of the proposed UWB pulse generator

Each delay line comprises the cascaded inverter stages with tail NMOS devices as source degeneration components. Its specific circuit diagram and simulated timing delay as the function of the tuning voltage are provided in Fig. 3. Each of these NMOS devices is used to modify the propagation delay of the respective inverter, which further changes the time delay of the DL. After applying a step input at A, the output at N appears after a delay, which is approximately equal to the sum of the individual inverter delays.

Fig. 3 also presents the variation of line delay as a function of tuning voltage (V_{tune}). The increase in tuning voltage reduces the line delay, and desired delay time is 125 ps to place the main lobe of the pulse at the center frequency of 4 GHz for a 3-5 GHz UWB band. The simulation results show that the tuning voltage of around 670 mV places the inverter delay at the desired time and can be further tuned during the measurement.

The full schematic of the proposed UWB pulse generator is illustrated in Fig. 4. To ensure that the output pulse is triangular shaped, the bridging transistors from *B* to *H* are linearly scaled. A linear increase in the size of transistors ensure that for a fixed V_{GS}, the transconductance, G_m, of each transistor increases linearly. Hence, for the transistors from *B* to *E*, the size of transistors increases, while from *F* to *H*, it decreases. The amplitude of the output UWB pulse is proportional to the peak value of the injection current, i_{inj}, the value of which is governed by the size of transistor *E*. The total current is combined at the drain terminals of the transistors and provided to an *RLC* tank with an on-chip inductor. The quality-factor modified resistor presents the output impedance to match the UWB antenna off-chip [11].

III. RESULTS AND DISCUSSIONS

Fig. 5 presents a graphical comparison of power spectral

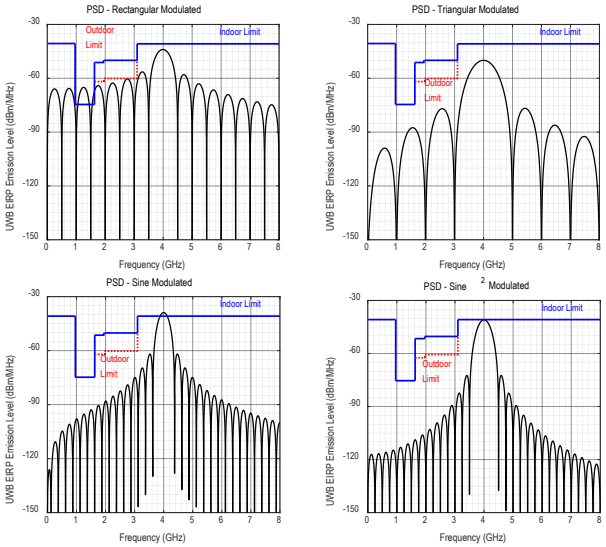

Fig. 5. Power spectrum density (PSD) of various shaping schemes with envelope width fixed at 2 *ns*

TABLE I.
Comparison of various shaping envelopes

Envelopes	Sidelobe Suppression (dB)	-10 dB Bandwidth (MHz)	EBW (MHz)
Rectangular	12.8	735	1000
Triangular	26.6	1114	2000
Sine	23.0	1018	1500
Sine-squared	31.4	1268	2000

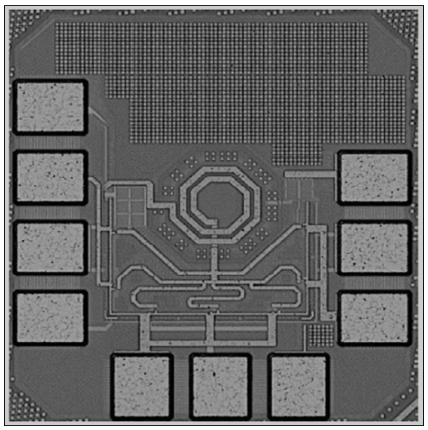

Fig. 6. Chip micrograph of the proposed UWB pulse generator.

densities (PSDs) of various pulse shaping functions. Table I provides a comparison of potential pulse shaping schemes in terms of the sidelobe suppression, the 10 dB bandwidth, and normalized essential bandwidth (EBW). The total width of all the envelopes was normalized to 2 ns to ensure a proper comparison. These results, being based on MATLAB simulations, show that the triangular envelope surpasses the rectangular one in terms of performance. A potential pulse-shaping envelope can be sine-squared, $sin^2(t)$, which provides enhanced performance in comparison to triangular shaping. However, digitally shaping a pulse with a sine-squared envelope shape is relatively tedious as compared to the analog approach, where an analog multiplier can be used to generate the sine-squared envelope. However, such

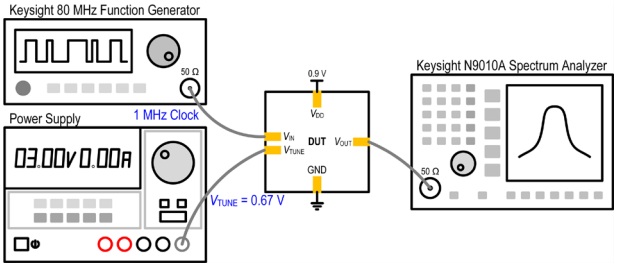

Fig. 7. Measurement setup

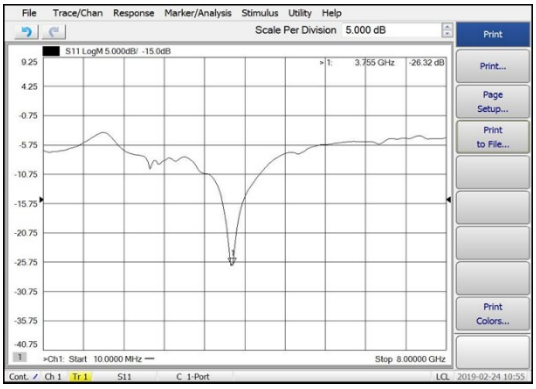

Fig. 8. Output matching performance of the proposed UWB pulse generator

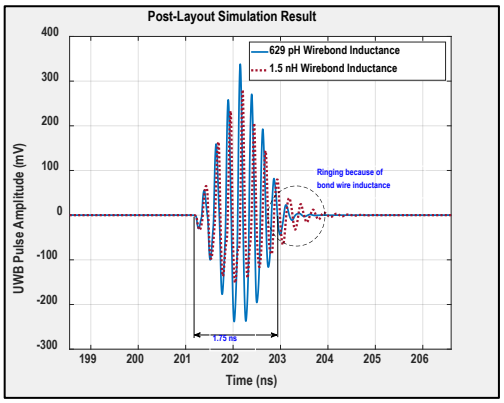

Fig. 9. Output transient waveform of the proposed UWB pulse generator.

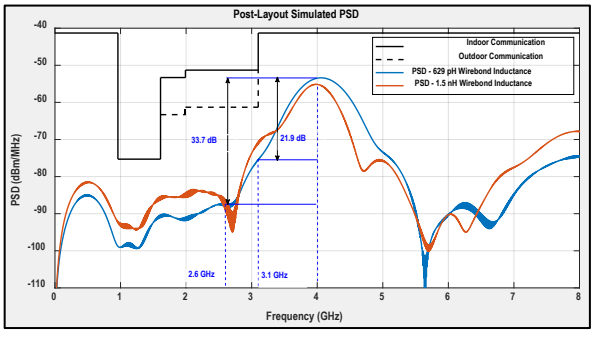

Fig. 10. Power spectrum density (PSD) of the proposed UWB pulse generator

The prototype chip, shown in Fig. 6, has been fabricated in a 65-nm CMOS process. The measurements of the chip were performed at $V_{DD} = 0.9\,V$. Fig. 7 shows the measurement setup to test the performance of the proposed

Table II. Performance Comparison

	V_{pp} (mV)	PW (ns)	BW_{-10dB} (GHz)	f_C (GHz)	SLS (dB)	ECPP (pJ)	η (%)
This Work	580	1.75	1.14	4	>30	34	3.9
[5]	160	3.5	520	3.8	>25	16.8	1.33
[10]	610	2	500	3.8	≈ 14	249	0.75
[12]	400	2	737	3.39	≈ 13	19	4.2
[13]	<100	2	700	4	≈ 14	22.6	0.22

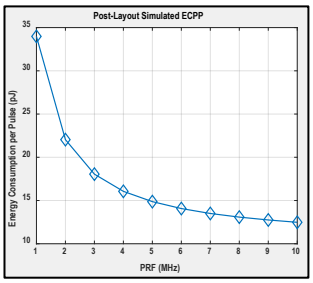

Fig. 11. Energy consumption per pulse vs. pulse repetition frequency (PRF).

UWB pulse generator. The 1 MHz clock is applied from a function generator, while the output spectrum was measured with Keysight N9010A spectrum analyzer. Fig. 8 shows the measured output matching (S_{22}, reflection coefficient) performance of the proposed UWB pulse generator. Due to the embedded matching network, which is composed of an on-chip inductor and additional resistive load, the pulse generator shows a stable and broadband output matching performance around 3-5 GHz UWB frequency band.

Output transient waveform and the PSD of the pulse generator is shown in Fig. 9 and Fig. 10, respectively. The bonding-wire inductance value is assumed to be around 0.6 nH to 1.5 nH and, thus, two extreme values are used for post-layout simulation with minor variations in the output transient waveform. Peak-to-peak pulse amplitude is simulated to be 580 mV with 1.5 nH bond-wire inductor while the PSD is well below the UWB spectrum mask at 1 MHz PRF. A discrepancy can be observed between the post-layout simulated and the calculated PSD of the proposed triangular shaped pulse generator at frequencies above 6 GHz. This difference arises due to higher-order effects, like the effect of wirebond inductance, insufficient on-chip supply decoupling capacitor, and process variations, due to which the pulse shaping deviates from an ideal triangular shaping. The baseline energy consumed by the individual delay cell is 1.7 pJ while the rest of the total energy contribution depends on the size of the bridging power transistor, with the largest being consumed by the middle one. Fig. 11 shows the post-layout simulated dependence of energy consumption per pulse as the PRF increases. The energy consumption is sensitive to lower PRF, but it almost saturates at higher PRFs.

Table II shows the comparison of the proposed UWB pulse generator with the related works. Owing to the triangular shaping scheme, the propose pulse generator provides more than 30 dB of sidelobe suppression (SLS), which is the highest among the related works, and a competitive energy efficiency, η, of 3.9 %. Even though the work in [12] provides the highest η, it has poor sidelobe suppression as compared to this work. Furthermore, the proposed pulse generator has the widest bandwidth as compared to the related works, thanks to the triangular shaping scheme.

IV. CONCLUSION

In this work, we presented a triangular enveloped ultra-wideband pulse generator aimed at IR-UWB applications. A comprehensive analysis has been presented, both describing the characteristics of commonly employed pulse shaping schemes and design considerations for developing the architecture. A pseudo-digital architecture is adopted to generate the UWB pulse with the heart of the circuit being inverter-based cascaded delay cells which generate switching pulses. The pulse center frequency governs the width of each of these pulses. An RLC tank approximates the Gaussian mono-cycle depending on the quality factor of the tank. The amplitude of these mono-cycles is dependent on the current injected into the tank, which has been controlled by the size of the power transistors. Implemented in 65-nm CMOS technology with a 0.9 V power supply, the measurement results show more than 30 dB sidelobe suppression in the DC-2.8 GHz band, while satisfying the FCC spectral mask. The output voltage swing is 580 mV (peak-to-peak) with a 10 dB bandwidth of 1.14 GHz and 34 pJ of energy consumption per pulse. The results show an energy efficiency of 3.9%, which is competitive with the recently published works.

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