A Random and Systematic Jitter Suppressed DLL-Based Clock Generator with Effective Negative Feedback Loop
Seong-Jin An and Young-Shig Choi

P. 01

An Implementation of MIMO PHY Modulator for IEEE 802.11n WLAN System
Minjoon Kim and Jaeseok Kim

P. 07

A 10-bit Single-ended SAR ADC with split dual-capacitive-array for Multi-channel Neural Recording System
Sung-Min Lee and Ju Eon Kim

P. 13

A Battery Management IC using Successive Approximation Register Analog to Digital Converter
Semi Lim, Junseok Park

P. 19

A Random and Systematic Jitter Suppressed DLL-Based Clock Generator with Effective Negative Feedback Loop
Hyeong-Sub Song, Sung-Kyu Kwon, Je-Young Kim, Dong-Jun Oh, Jeong-Chan Lee

P. 25

Design and verification of internal core circuit of FlexRay transceiver in the ADAS
Yui-Hwan Sa and Hyeong-Woo Cha

P. 32

A Current-mode Digital Buck-Boost Converter for LED Driver
Ji-Hoon Park and In-Chul Hwang

P. 38

Single-Inductor Multiple-Output DC-DC Converter with Comparator-Based Feedback Circuit
Jin-Gyu Kang and Changsik Yoo

P. 45