# WR-3.4 Band Reflection-type Phase Shifters

Eun Jung Kim[1] and Sang Geun Jeon[a]
Department of Electrical Engineering, Korea University
E-mail : [1]ejkim96@korea.ac.kr

***Abstract* – This paper presents two WR-3.4 reflection-type phase shifters (RTPS), *i.e.* RTPS1 and RTPS2, using in a 250-nm InP double heterojunction bipolar transistor (DHBT) process. The proposed RTPSs adopt a compact broadside-coupled line coupler as a 90° hybrid coupler. In addition, the average loss variation is reduced by optimizing the impedance of coupled-line coupler and the reflective load. The RTPS1 achieves a 180° phase shift with an average insertion loss of 3.5 to 7.9 dB while maintaining loss variation less than 1.7 dB. The RTPS2 exhibits a full 360° phase shift using a triple-resonance load. The chip size including all probing pads is as small as 372 x 458 $\mu m^2$. The dc power consumption is zero.**

***Keywords*—Phased array system, Reflection-type phase shifter (RTPS), Terahertz band, Triple-resonance load, WR-3.4 band**

## I. INTRODUCTION

The wide bandwidth of the terahertz band (0.3 – 3 THz) is drawing attention to be utilized in the high-speed wireless communication and high-resolution imaging system. Unfortunately, such high-frequency bands suffer from a tight link budget because of high atmospheric absorption and high free-space path loss. As one of the solutions to the high channel loss and tight link budget, a phased array can be adopted. The phased array system enables the electrical beam forming and steering, thereby improving the effective isotropic radiated power (EIRP) in transmitters and signal-to-noise ratio (SNR) in receivers.

A phase shifter is an essential circuit block for a phased array system that controls the phase delay of a multi-path signal coupled in-phase in free space. The phase shifter in a large-scale phased array system should have low dc power consumption and compact size. Furthermore, 360° phase shift range and small insertion loss performance are required. In recent years, several phase shifters with various topologies in WR-3.4 band have been reported [1-8]. Most phase shifters operate in an active type, including the Gilbert cell-based vector modulators and active switches [1-5]. However, due to the significant passive loss and limited device speed at the high frequency of terahertz, the active phase shifters mostly do not provide gain while consuming considerable dc power. On the other hand, the reflection-type phase shifter (RTPS) generally consumes zero dc power and has advantage of adjusting the phase only a few control voltages. However, the RTPS would suffer from poor insertion loss and a limited phase shift range [6-8].

a. Corresponding author; sgjeon@korea.ac.kr

Manuscript Received Jan. 06, 2022, Revised Mar. 15, 2022, Accepted Mar. 25, 2022



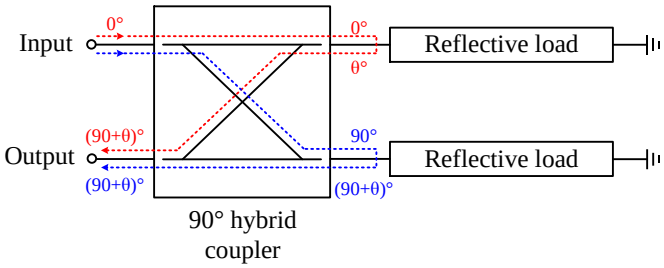


Fig. 1. Operation principle of the RTPS.

This paper presents two compact and wideband RTPSs operating in the WR-3.4 band. By adopting a broadside coupled-line coupler, the chip area is reduced. In addition, the average loss variation is minimized by implementing the reflective load and 90° coupler with the optimum impedance.

This paper is organized as follows. Section II provides a brief introduction of the device technology. A detailed RTPS design is presented in Section III. The simulation results of the RTPSs are provided in Section IV. Lastly, Section V summarizes this paper.

## II. TECHNOLOGY DESCRIPTION

The proposed RTPS is designed with a Teledyne 250-nm InP double heterojunction bipolar transistor (DHBT) technology [9]. A 4x0.25 $\mu m^2$ transistor features a current-gain cutoff frequency ($f_T$) and maximum oscillation frequency ($f_{MAX}$) of > 370 GHz and > 650 GHz, respectively. The technology provides four metal layers (M1–M4) with a top metal thickness of 3 μm. A benzocyclobutene (BCB) dielectric with $\varepsilon_r$ of 2.7 is used for the interlayer material. Also, a metal-insulator-metal (MIM) capacitor with 0.3 $fF/\mu m^2$ and NiCr thin-film resistor with a sheet resistance of 50 Ω are provided. The backside of the InP substrate is thinned to 75 μm and through-wafer vias are provided to suppress the undesirable substrate-propagating modes.

## III. CIRCUIT DESIGN

Fig. 1 shows the basic operation principle of the RTPS. It consists of a 90° hybrid coupler and two identical reflective loads. The 90° hybrid coupler splits the input signal into two signals with equal amplitude and 90° phase difference. The divided input signal is reflected by the impedance mismatch

between the coupler and the load, which causes a phase shift. After the phase shift at the reflective load, the 90° hybrid coupler combines the reflected signals. At the isolation port of the coupler, the reflected signals are combined in-phase, so the isolation port is used as the output port of the RTPS. On the contrary, at the input port, the reflected signals are out-of-phase and canceled out.

The reflective load usually determines the performance of the RTPS, so it is important to optimize the reflective load design. The reflective load is generally implemented using a varactor because its capacitance is easily varied by adjusting a single control voltage.

Two compact and wideband RTPSs operating in the WR-3.4 band are presented in this work. The first RTPS (RTPS1) is designed with a 180° phase shift and low insertion loss and wide bandwidth using a simple reflective load. The second RTPS (RTPS2) employs a triple-resonance load to extend the phase shift range to 360°.

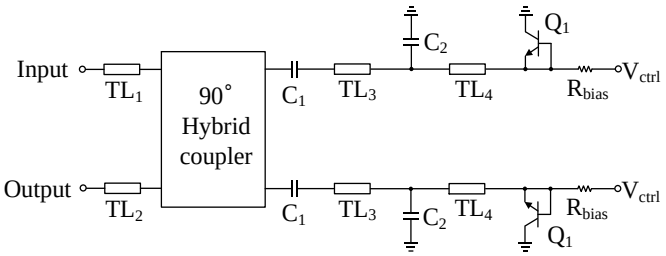


Fig. 2. Schematic of the proposed 180° RTPS (RTPS1).

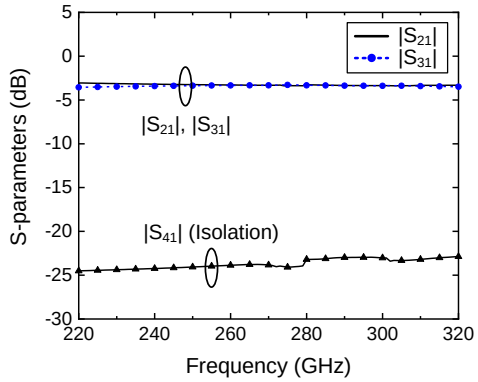


Fig. 3. Simulated magnitude performance of the coupled-line coupler.

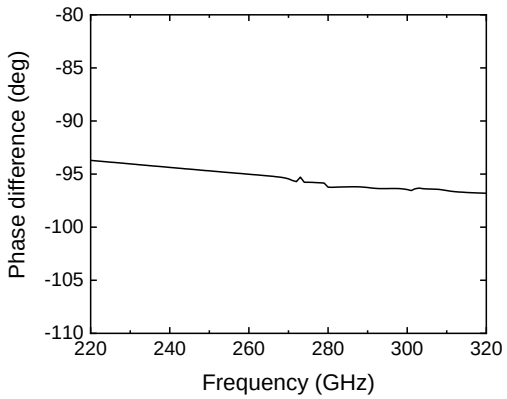


Fig. 4. Simulated phase performance of the coupled-line coupler.

### *A. WR-3.4 180° RTPS (RTPS1)*

Fig. 2 presents a schematic of the proposed 180° RTPS. The 90° hybrid coupler for dividing the input signal and combining the reflected signal is implemented using a coupled-line coupler. The reflective load consists of a varactor ($Q_1$) and an L-section network ($TL_4$ and $C_2$). The varactor $Q_1$ is implemented using a diode-connected transistor with an emitter length of 6$\mu$m. A transmission line ($TL_4$) and a shunt capacitor ($C_2$) are used to extend the phase range to 185°.

To minimize the insertion loss variation over the phase states of the RTPS, the impedance trajectory of the reflective load rotates around the center of the Smith chart. Therefore, a short transmission line ($TL_3$) is used to move the center of the impedance trajectory of the load to 30 Ω. Since the reflective load operates with reference to 30 Ω, the quadrature hybrid coupler is also designed with a 30-Ω port impedance. Instead, quarter-wave transformers ($TL_1$ and $TL_2$) are used at the input and output of the RTPS1 for 50-Ω matching.

The 30-Ω quadrature hybrid coupler is implemented using a coupled-line coupler with two metal layers (M1 and M2) broadside-coupled to each other. In order to optimize the magnitude and phase performance of the coupler, electromagnetic (EM) simulations were carried out using Agilent ADS Momentum. Fig. 3 presents the simulated $|S_{21}|$ and $|S_{31}|$ of the coupler, ranging from -3.5 to -3.0 dB over the frequency from 220 to 320 GHz, with the isolation higher than 23 dB. The phase difference ranges from 93 to 96°, as shown in Fig. 4.

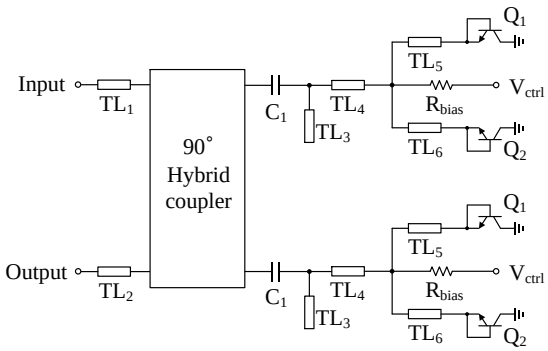


Fig. 5. Schematic of the proposed 360° RTPS (RTPS2).

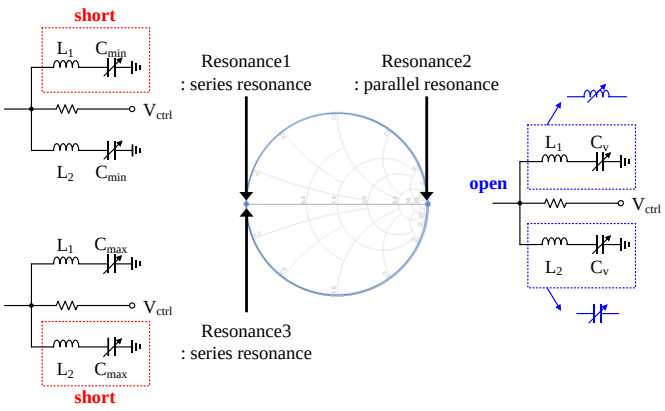


Fig. 6. Impedances of the triple-resonance load.

### *B. WR-3.4 360° RTPS (RTPS2)*

Fig. 5 presents a schematic of the proposed RTPS2. To achieve a full 360° phase shift range, a triple-resonance load is used. It consists of two varactors ($Q_1$ and $Q_2$), two series inductors ($TL_5$ and $TL_6$), and an L-section network ($TL_3$ and $TL_4$).

The impedance of triple-resonance load is depicted in Fig. 6. The capacitance of the varactor ($C_v$) is varied from $C_{min}$ to $C_{max}$ depending on the control voltage. The series inductor ($L_1$ and $L_2$) connected to each varactor resonates with the capacitance of the varactor, therefore extending the phase shift range. The first resonance is a series resonance with $L_1$

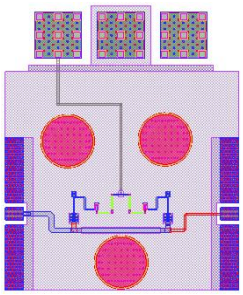

Fig. 7. Layout of the RTPS1.

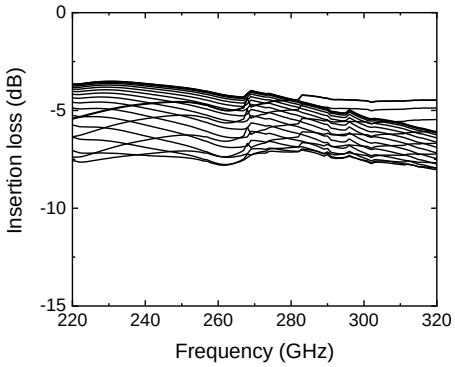


Fig. 8. Simulated insertion loss of the RTPS1.

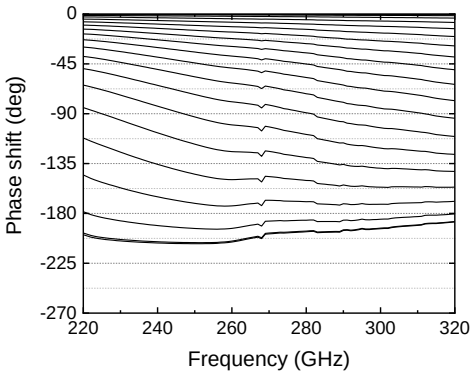


Fig. 9. Simulated phase shift of the RTPS1.

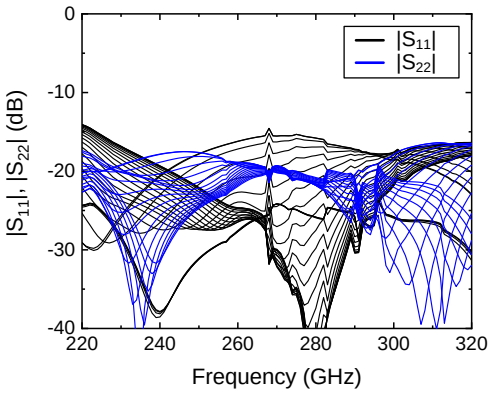


Fig. 10. Simulated input and output matching performance of the RTPS1.

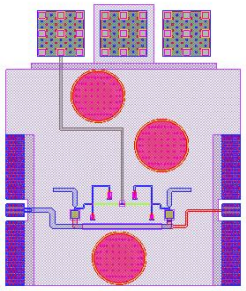

Fig. 11. Layout of the RTPS2.

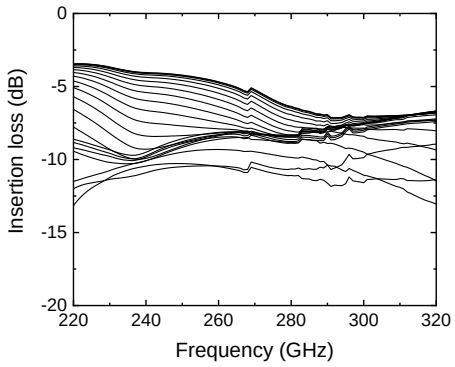


Fig. 12. Simulated insertion loss of the RTPS2.

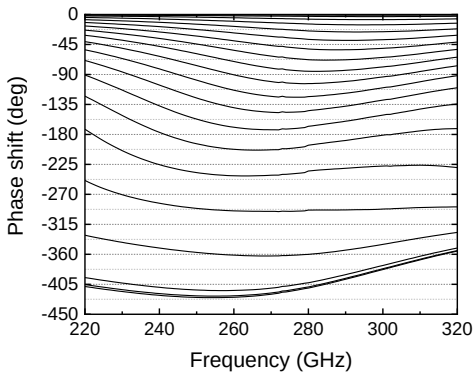


Fig. 13. Simulated phase shift of the RTPS2.

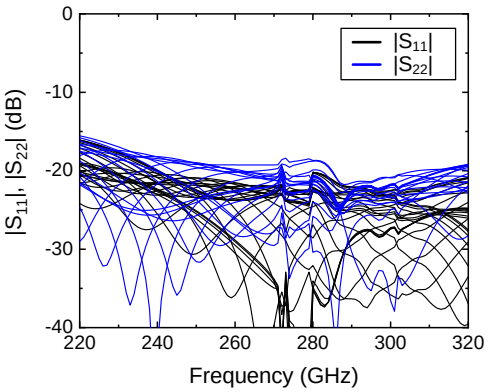


Fig. 14. Simulated input and output matching performance of the RTPS2.

TABLE I. Performance Comparison with other RTPS operating in the WR-3.4 band

| Reference | Technology | Frequency (GHz) | Min. phase shift range (deg) | Average gain (dB) | $P_{dc}$ (mW) | Size ($mm^2$) |
|---|---|---|---|---|---|---|
| [6] | 50-nm GaAs | 245–255 | 145 | -13.6 – -11.5 | 0 | 0.56 |
| [7] | 50-nm GaAs | 218–268 | 205 | -4.6 – -1.6 | 28.4 | 0.56 |
| [8] | 50-nm GaAs | 214–276 | 118 | -7.8 – -7** | 0 | 0.25 |
| **This work* (RTPS1)** | **250-nm InP** | **220–320** | **180** | **-6.5 – -4.8** | **0** | **0.17** |
| **This work* (RTPS2)** | **250-nm InP** | **220–320** | **360** | **-8.3 – -6.4** | **0** | **0.17** |

*Simulation results, **Read from a plot in the article

when $C_v$ is $C_{min}$. In this condition, the resistance of the load impedance at the center frequency becomes minimum and the reactance becomes zero. The second resonance is the parallel resonance that occurs when $C_v$ is between $C_{min}$ and $C_{max}$. As $C_v$ increases after the first series resonance, the $L_1$-$C_v$ branch becomes inductive. On the contrary, $L_2$-$C_v$ branch becomes capacitive. When the impedances of the two resonators become conjugate to each other, they generate a parallel resonance. In this condition, the resistance of the load impedance becomes the maximum whereas the reactance becomes zero. Lastly, when $C_v$ is $C_{min}$, it generates series resonance with $L_2$.

The varactors, $Q_1$ and $Q_2$ are implemented using a diode-connected transistor with an emitter length of 6$\mu$m and 3$\mu$m, respectively. In addition, given that the reference impedance of the 90° hybrid coupler is 30 Ω, an L-section network ($TL_3$ and $TL_4$) is used for impedance matching to 30 Ω. Also, the quarter-wave transformers ($TL_1$ and $TL_2$) are used at the input and output of the RTPS for 50-Ω matching.

## IV. SIMULATION RESULTS

### *A. WR-3.4 180° RTPS (RTPS1)*

The proposed RTPS was designed using a Teledyne 250-nm InP DHBT technology. The layout of the RTPS1 is shown in Fig. 7. The circuit area including RF and DC probing pads is 372 x 458 $\mu m^2$.

Fig. 8 presents a simulated insertion loss of the RTPS1 as the control voltage $V_{ctrl}$ changes between -0.5V and +0.5V. It is found that the insertion loss varies from -7.9 to -3.5 dB over the frequency range of 220 to 320 GHz. In this frequency range, the average insertion loss ranges from -6.5 to -4.8 dB, resulting in a 1.7 dB variation. Fig. 9 depicts the simulated phase shift performance. A continuous phase shift of at least 180° is achieved in the full WR-3.4 band. The input and output return loss are below -10 dB for all phase states, as shown in Fig. 10. The input and output return loss are better than 14.0 and 20.4 dB, respectively.

### *B. WR-3.4 360° RTPS (RTPS2)*

The layout of the RTPS2 is shown in Fig. 11. The circuit area including RF and DC probing pads is 372 x 458 $\mu m^2$.

Fig. 12 shows a simulated insertion loss of the RTPS2 as $V_{ctrl}$ changes between -0.5V and +0.5V. The insertion loss ranges from -10.6 to -5.2 dB at 270 GHz and maintains above -13 dB from 220 to 320 GHz. In this frequency range, the average insertion loss ranges from -8.3 to -6.4 dB, resulting in a 1.9 dB variation. The simulated phase shift over $V_{ctrl}$ is shown in Fig. 13. The proposed RTPS2 can continuously change the phase by at least 360° in the full WR-3.4 band. The input and output port matching are shown in Fig. 14. The return loss is better than 14.3 and 16.4 dB at the input and output, respectively.

In Table I, the proposed RTPSs are compared with the other RTPSs operating in the WR-3.4 band. This work achieves a 180 and 360° phase shift range with comparable insertion loss and wide bandwidth covering the full WR-3.4 band.

## V. CONCLUSION

The WR-3.4 band RTPSs were designed in a 250-nm InP DHBT technology. The RTPS1 exhibits a continuous 180° phase shift with low insertion loss and a wide bandwidth. The average loss variation is minimized by optimizing the impedance of the 90° coupler and the reflective load to 30 Ω. The RTPS1 provides an average insertion loss of 5.3 dB at 270 GHz and a loss variation below 1.7 dB in the WR-3.4 band. The RTPS2 achieves a full 360° phase shift using a triple-resonance reflective load with comparable insertion loss. The average insertion loss of the RTPS2 is 7.5 dB at 270 GHz and a loss variation below 1.9 dB in the WR-3.4 band. Compared to other RTPS in the WR-3.4 band, this work achieves a wide bandwidth and a wide phase shift range with a compact chip size and comparable insertion loss. The RTPSs can be used in the phased array systems in the WR-3.4 band.

## ACKNOWLEDGMENT

This work was supported by Institute of Information & communications Technology Planning & Evaluation (IITP) grant funded by the Korea government (MSIT) (No.2021-0-00260, Research on LEO Inter-Satellite Links). The authors would like to thank the IC Design Education Center (IDEC), Korea for the chip fabrication and EDA tool support.

REFERENCES

[1] M. Elkhouly, S. Glisic, C. Meliani, F. Ellinger, and J. C. Scheytt, "220–250-GHz Phased-Array Circuits in 0.13-$\mu$m SiGe BiCMOS Technology," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 8, pp. 3115-3127, Aug. 2013.

[2] H. G. Yu, K. J. Lee, and M. Kim, "300 GHz vector-sum phase shifter using InP DHBT amplifiers," *IET Electron. Lett.*, vol. 49, no. 4, pp. 263–264, Feb. 2013.

[3] C. Quan, S. Heo, M. Urteaga and M. Kim, "A 275 GHz Active Vector-Sum Phase Shifter," in *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 2, pp. 127-129, Feb. 2015.

[4] Y. Kim, S. Kim, I. Lee, M. Urteaga and S. Jeon, "A 220–320-GHz Vector-Sum Phase Shifter Using Single Gilbert-Cell Structure with Lossy Output Matching," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 1, pp. 256-265, Jan. 2015.

[5] D. Müller, P. Pahl, A. Tessmann, A. Leuther, T. Zwick and I. Kallfass, "A WR3-Band 2-bit Phase Shifter Based on Active SPDT Switches," in *IEEE Microwave and Wireless Components Letters*, vol. 28, no. 9, pp. 810-812, Sept. 2018.

[6] D. Müller *et al*., "A h-band reflective-type phase shifter MMIC for ISM-Band applications," *2014 IEEE MTT-S International Microwave Symposium (IMS2014)*, 2014, pp. 1-4.

[7] D. Muller *et al*., "A WR3-band reflective-type phase shifter MMIC with integrated amplifier for error- and loss compensation," *2017 12th European Microwave Integrated Circuits Conference (EuMIC)*, 2017, pp. 1-4.

[8] D. Müller *et al*., "Bandwidth Optimization Method for Reflective-Type Phase Shifters," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 4, pp. 1754-1763, April 2018.

[9] M. Urteaga et al., "InP HBT Integrated Circuit Technology for Terahertz Frequencies," *2010 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Monterey, CA, USA, 2010, pp. 1-4.

**Eun Jung Kim** received the B.S. degrees in electrical engineering from Chungnam National University, Daejeon, Korea, in 2019, where she is currently working toward the Ph.D. degree in electrical and electronics engineering. Her research interest includes mm-wave and THz circuits.

**Sang Geun Jeon** received the B.S. and M.S. degrees in electrical engineering from Seoul National University, Seoul, South Korea, in 1997 and 1999, respectively, and the M.S. and Ph.D. degrees in electrical engineering from the California Institute of Technology (Caltech), Pasadena, CA, USA, in 2004 and 2006, respectively. From 1999 to 2002, he was a full-time Instructor in electronics engineering with the Korea Air Force Academy, Cheongju, South Korea. From 2006 to 2008, he was a Research Engineer, where he was involved with CMOS phased-array receiver design. Since 2008, he has been with the School of Electrical Engineering, Korea University, Seoul, where he is currently a Professor. His current research interests include integrated circuits and systems at microwave, mm-wave, and terahertz bands for high-speed wireless communications and high-resolution imaging applications.