# Design Techniques of Energy-Efficient Electrical Neural Recording System

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***Abstract*—This paper reviews the design techniques of the electrical neural recording system for energy-efficient operation. To operate neuroprosthetics by decoding action potentials (or neural spikes) and local field potentials *in vivo*, the electrical neural recording system can be used. For extending the system battery lifetime *in vivo* and avoiding tissue damage due to the heat, the neural recording system needs to be energy-efficiently driven while consuming low power and achieving low noise performance. In this paper, three energy-efficient design techniques are reviewed with basic properties of the electrical neural recording system: 1) energy-efficient input structure of the operational transconductance amplifier, 2) neural recording front-end channel using the low supply voltage, and 3) neuronal activity-dependent recording system.**

***Keywords*—AP, LFP, Energy-efficient neural recording system, Low-power design technique, Low-noise design technique, Implantable medical devices, Neuronal activity-dependent system operation, Spike-dependent operation**

## I. INTRODUCTION

Neural activity monitoring is an essential part to drive neuroprosthetics for tetraplegia people and understand neuroscience [1]. Action potentials (APs) and local field potentials (LFPs) are important neuronal information for understanding human intention, behaviors, biological phenomena, etc. In addition to the recording of APs and LFPs, the monitoring of neurotransmitters and calcium ions provides crucial neuronal information for unveiling complex neuronal phenomena [2], [3]. APs and LFPs can be monitored as voltage signals through the microelectrode array [4], [5]. The amplitude of APs ranges from tens of $\mu$V to hundreds of $\mu$V, whereas LFPs change from hundreds of $\mu$V to several mV [2]. Neurotransmitters and calcium ions can be monitored as current signals generated by the electrochemical sensor and photodiode, respectively [3].

To monitor the weak voltage signals of APs and LFPs, the electrical neural recording system needs to process the input voltage signals with appropriate conversion gain and resolution while maintaining low power and low noise performances. Also, when considering the electrical neural recording system operating *in vivo*, the overall power consumption of the recording system needs to be restricted to avoid tissue damage due to the heat and extend the battery lifetime. Therefore, the electrical neural recording system needs to be implemented energy-efficiently by consuming low power and achieving low input-referred noise. For a holistic understanding of the brain by obtaining sufficient neural information, a high density of the neural recording system is required. However, the high-density recording system can induce increased overall power consumption. So each neural recording channel needs to be designed to consume low power while achieving low input-referred noise. In addition, since the high-density recording system needs to be implemented within a limited silicon area, each neural recording channel must be designed to occupy a small design area.

To implement the energy-efficient multichannel neural recording system, three design techniques are reviewed with the basic properties of the electrical neural recording system: 1) energy-efficient input structure of the operational transconductance amplifier [6]–[13], 2) neural recording front-end design using the low supply voltage [14]–[17], and 3) neuronal activity-dependent recording system by scheduling power and controlling data transmission [18]–[22]. The operational transconductance amplifier used in the first amplification stage of the entire recording system determines the overall input noise performance and system power consumption. Therefore, the amplifier of each amplification stage needs to be carefully designed according to the required electrical performance. The straightforward way to reduce the entire power consumption is to lower the supply voltage. However, since the reduced supply voltage affects the dynamic range and transistor operation, the supply voltage needs to be carefully set while ensuring the operation of each transistor and ensuring a sufficient dynamic range. Also, for reducing the power consumption of the entire recording system, the power-consuming blocks, such as the amplifier and communication circuits, can be enabled only when the neural signal is present.

This paper is organized as follows. Basic properties of the neural recording system and energy-efficient design techniques are presented in Section II. Section III concludes this paper with design considerations of the recording system.

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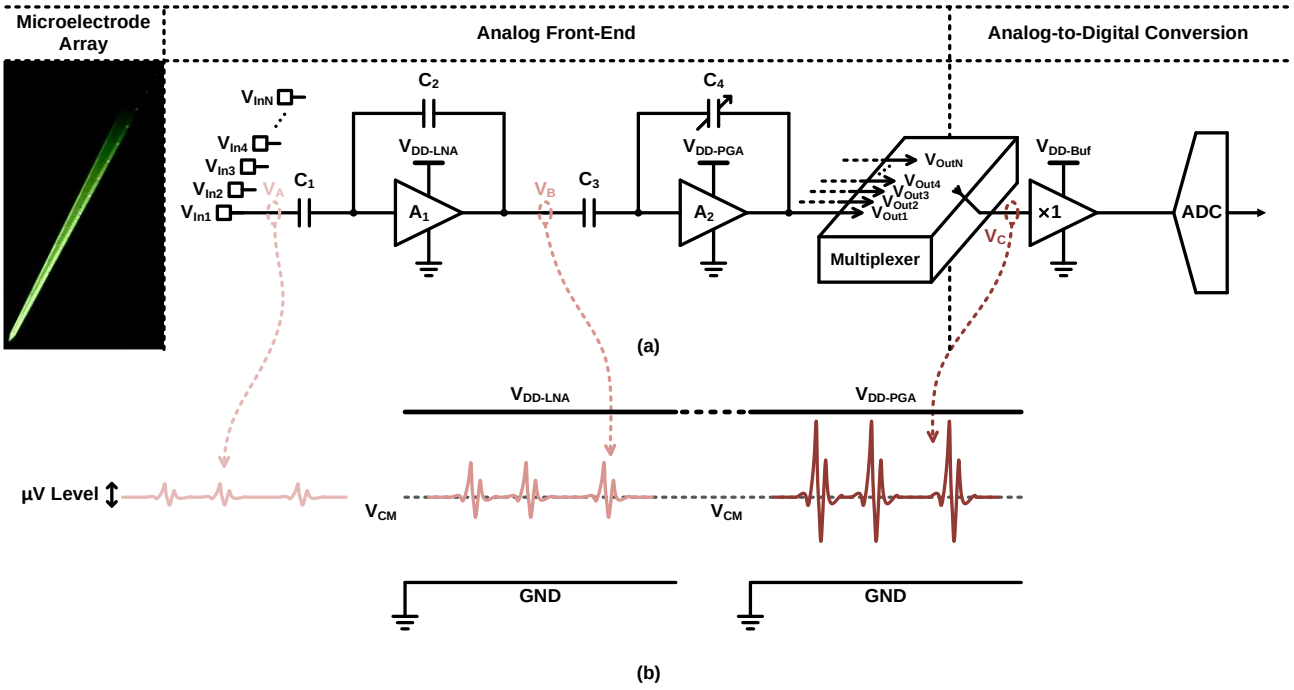


Fig. 1. (a) Neural recording chain from the microelectrode array detecting APs and LFPs to the front-end circuits processing the detected voltage signals. (b) Amplification stage of the neural signals within the supply voltage.

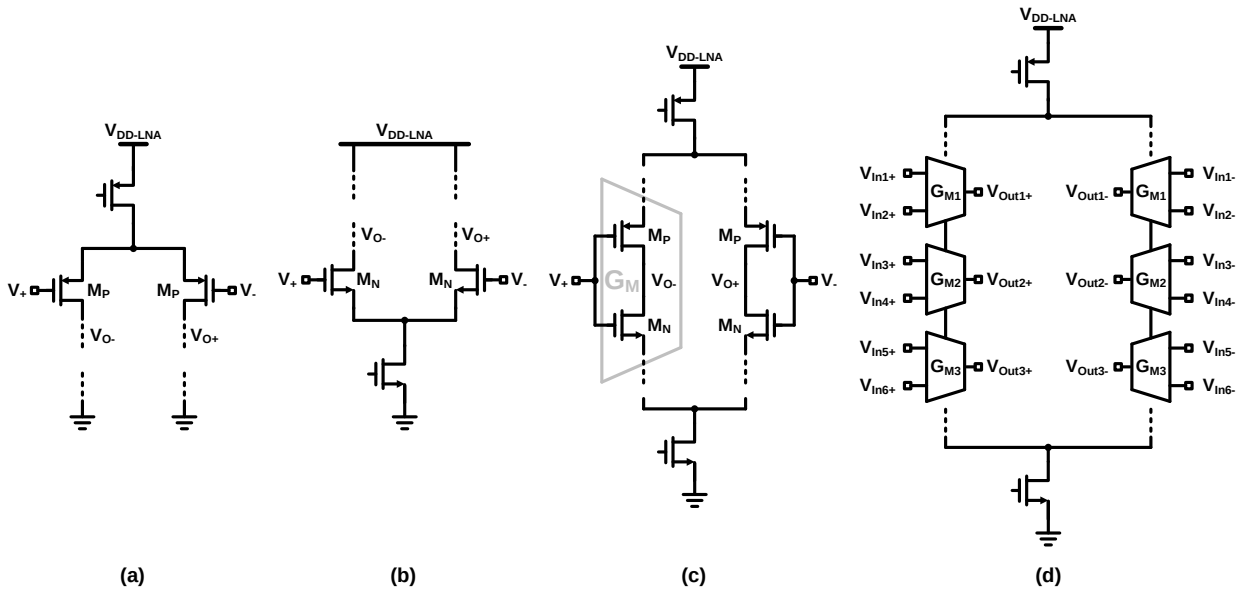


Fig. 2. Differential input stages used in the OTA of the low-noise amplifier: (a) PMOS input pair, (b) NMOS input pair, (c) inverter-based (or current reuse) input pair, and (d) stacked inverter-based input pair.

## II. ENERGY-EFFICIENT DESIGN TECHNIQUES

### *A. Basic Properties of Electrical Neural Recording System*

Since the development of the low-noise amplifier (LNA) employing the capacitively-coupled topology [6], [7], many research teams proposed multichannel electrical neural recording systems based on the design of the capacitively-coupled topology. The capacitive input-based LNA can reliably monitor APs and LFPs with low power and low noise characteristics. Also, thanks to the capacitive input characteristic, the DC electrode offset is efficiently filtered out. Fig. 1(a) shows the entire neural recording chain from the microelectrode array [5] detecting APs and LFPs to the front-end circuits processing the detected neural signals.

For simplifying the description of the front-end circuits, the schematic of the recording system is drawn as a single-ended structure. It is assumed that the DC bias point of the amplifier output is properly set with the half-$V_{DD}$. When implementing the multichannel neural recording system, the number of the analog front-end channels is set equal to the

number of the microelectrode array channels [7], [10]. However, when the number of the microelectrode array channels increases to several hundred or the order of ten thousand, the number of the analog front-end channels cannot be designed as much as the number of the microelectrode array channels due to a limited silicon area. Thus, to overcome the design area issue, the switch matrix can be used to interface between a large number of the microelectrode array channels and a limited number of the front-end channels [23], [24].

The electrical neural signals detected through the microelectrode array are amplified by the analog front-end channel and digitized by the analog-to-digital converter (ADC) as shown in Fig. 1(a). To area-efficiently implement the entire neural recording system during the digitization of neural signals, a single ADC can be shared by multiple analog front-end channels through the multiplexer, as shown in Fig. 1(a) [10], [15], and [24]. Fig. 1(b) shows the amplification stage of the neural signals within the supply voltage. $V_{DD\text{-}LNA}$ and $V_{DD\text{-}PGA}$ are supply voltages used in LNA and programmable gain amplifier (PGA), respectively. The amplitude of detected APs resides at the $\mu$V level, whereas LFPs have the amplitude from the $\mu$V level to the mV level. Typically, the $\mu$V-level neural signals are first amplified by the LNA and further amplified by the PGA for providing enough conversion resolution for the ADC (Fig. 1(b)). Then, the PGA output is digitized by the ADC through the multiplexer and ADC driving buffer (Fig. 1(a)).

In the neural recording chain from the LNA to the ADC, the ADC driving buffer driven by $V_{DD\text{-}Buf}$ is a power-hungry building block. Thus, to implement the energy-efficient multichannel neural recording system, the power consumption of the buffer needs to be saved, and the dual sample-and-hold (S/H) technique can be applied to the ADC for mitigating the power consumption of the buffer [10].

In summary, a vast amount of neural signals must be decoded to expand the understanding of the brain, which means the number of recording channels needs to increase. Therefore, the multichannel neural recording system needs to be energy- and area-efficiently designed by optimizing circuits, such as the analog front-end channel, buffer, and ADC, without performance degradation.

### *B. Energy-Efficient Input Structure of OTA*

In the whole chain of the neural recording system, the LNA is the most sensitive stage to noise and power consumption. The LNA amplifies the weak voltage signals detected from the high-impedance microelectrode array which is directly related to noise contribution. Therefore, the LNA should be designed to minimize the noise generated by the circuit itself. When designing the capacitive input-based LNA, the operational transconductance amplifier (OTA) is used to create an accurate closed-loop gain by providing sufficient open-loop gain. Also, the OTA is a key block that determines the overall input-referred noise and area of the entire recording channel. The OTA input is typically designed as a differential structure to filter out the common-mode noise and implemented to be achieved high transconductance $g_m$. In the LNA design, the $g_m$ of the OTA input stage determines the overall input noise performance and needs to be high for reducing thermal noise contribution [6], [7]. For mitigating the flicker noise contribution from the LNA, the input stage of the OTA is designed with large size. In summary, to lower the thermal noise and flicker noise contributions from the LNA, the operation region of the OTA input stage is pushed into the subthreshold region, thereby achieving high $g_m$, and the OTA input pair is designed with a large size [6], [7].

Fig. 2 shows differential input stages used in the OTA of the LNA. Figs. 2(a) and (b) are input pairs implemented by using PMOS and NMOS, respectively, [6], [7], [18], [22], and [23]. Compared to the designs of Figs. 2(a) and (b), the inverter-based (or current reuse) input pair can boost $g_m$ by about two times while consuming the same bias current as the bias current in the PMOS and NMOS input pairs, as shown in Fig. 2(c) [8]–[11], [15]–[17]. By stacking PMOS and NMOS in a single current branch, the noise efficiency factor (NEF) is improved without an increase in power consumption. Thus, the inverted-based input pair is widely employed for designing the energy-efficient LNA. However, the design area increases by about two times compared to the PMOS (or NMOS) input pair. That is why the inverter-based topology is usually applied to the noise- and power-sensitive stage such as LNA. After amplifying neural signals through the LNA, the PGA further amplifies the LNA output signal. Since the LNA output signal is on the order of mV, the noise performance required by the PGA is more relaxed than the LNA. Thus, to save the design area, the PMOS (or NMOS) input pair is employed for the PGA input stage while consuming a very low bias current.

To further improve the NEF of the LNA, the inverter-based topology can be stacked, whereas the design area increases, as shown in Fig. 2(d) [12], [13]. Also, when applying the stacked inverter-based input pair to the LNA, the bias point of the OTA needs to be carefully set. Compared to the single inverter-based input pair driven by $V_{DD\text{-}LNA}$, the stacked inverter-based input pair can require a higher supply voltage than $V_{DD\text{-}LNA}$, resulting in increased power consumption. Also, if the low supply voltage is used, the gate terminals of the stacked inverter-based input pair should be individually biased for proper DC bias setup, compared to the single inverter-based input pair where PMOS and NMOS gate terminals are tied together and biased [12], [13].

### *C. Front-End Channel using Low Supply Voltage*

The straightforward way to lower the system power consumption is to reduce the supply voltage throughout the whole recording chain (e.g., $V_{DD\text{-}LNA}$, $V_{DD\text{-}PGA}$, and $V_{DD\text{-}Buf}$) [14]–[17]. In the multichannel recording system, multiple LNAs and PGAs share a single ADC for an area-efficient design, meaning that most of the power consumption in the

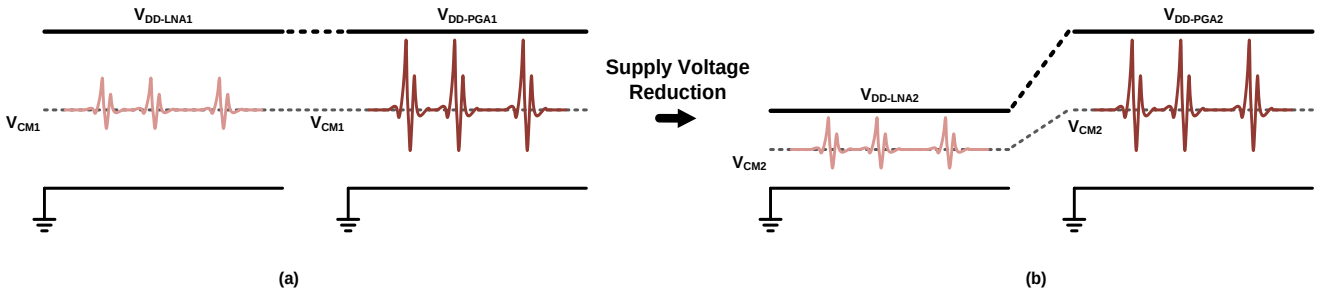


Fig. 3. Amplification stage of the front-end channel using (a) same supply voltages ($V_{DD-LNA1} = V_{DD-PGA1}$) and (b) dual supply voltages ($V_{DD-LNA2} \neq V_{DD-PGA2}$).

entire recording system occurs in the array composed of the LNAs and PGAs.

As shown in Fig. 3(a), when the LNA and PGA are driven by using the same supply voltages ($V_{DD-LNA1} = V_{DD-PGA1}$), the LNA output has sufficient voltage headroom, whereas the PGA output has less voltage headroom because the signal is further amplified than the LNA output. For optimizing the power consumed by each amplification stage, the dual supply voltages, $V_{DD-LNA2}$ and $V_{DD-PGA2}$, can be applied to reduce surplus voltage headroom while keeping the amplifier in the proper operation region, as shown in Fig. 3(b) [15], [16]. For operating the recording system using dual supply voltages, the external low supply voltage can be up-converted to a higher supply voltage through one charge pump and one low-dropout (LDO) regulator [15]. Also, the dual supply voltages can be generated through the buck converter [16]. Then, the low supply voltage is used for the LNAs, and the higher supply voltage is employed for the PGAs. Thus, wasted power is reduced by optimizing the voltage headroom of each amplification stage.

However, when operating the OTA composed of the inverter-based input pair by using a low supply voltage, the overdrive voltage of input circuits may not be set to push the devices into the saturation (or subthreshold) region. To overcome this DC bias setup issue, the individual bias voltages can be applied to the OTA input terminals by placing the decoupling capacitor between PMOS and NMOS of the inverter-based input pair [16], [17]. The recording system driven by using the low supply voltage can reduce the overall power consumption of recording channels, whereas a well-regulated supply voltage is required. Also, the circuits driven under the low supply voltage can be vulnerable to PVT (process, voltage, and temperature) changes, meaning that the recording system can experience unstable operation when implanted *in vivo*. Therefore, sophisticated design techniques are required to ensure reliable system operation.

### *D. Neuronal Activity-Dependent Recording System*

When the neural recording system is designed by incorporating the wireless communication circuits, the digitized neural data through the ADC can be transmitted to the RF transmitter. Throughout the whole recording system, the analog front-end channel array, buffer, and RF transmitter are power-hungry building blocks. However, when conducting the recording experiment *in vivo* (or *in vitro*), the recording system doesn't always monitor meaningful neural signals from the microelectrode array, resulting in significant power consumption. The circuits always perform digital conversion and wireless data transmission, even for meaningless neuronal data, which wastes the overall system power considerably. To overcome this wasted power issue and ensure energy-efficient system operation, the neuronal activity-dependent recording system is developed as shown in Fig. 4 [18]–[22].

Fig. 4 describes the block diagram of the wireless neural recording system incorporating the spike detector and power/data management circuits. The spike detector always senses the neural signals to snatch the spikes. Then, according to the detected neural spikes, the spike detector generates the control signals for delivering power and transmitting neural data. Neural spike detection can be conducted through analog signal processing [18], [19] and digital signals processing [20], [21]. During the spike detection in the analog domain, the amplified neural signal is compared to a manually (or automatically) set threshold through the comparator. When the neural signal exceeds the threshold, the comparator generates enable signal for controlling the power delivery and data transmission. During the spike detection in the digital domain, digitized neural data is stored in the intermediate memory used to calculate the threshold. Then, the detected neural spike is transmitted to the output memory. Through this neuronal activity-dependent system operation, the power consumed for meaningless signals can be saved. Therefore, the overall system power can be considerably reduced, and the battery lifetime also can be prolonged.

## III. CONCLUSION

This paper briefly summarizes the energy-efficient design techniques for the electrical neural recording system. In addition to the energy-efficient design techniques introduced here, various factors need to be considered to ensure the reliable operation of the entire recording system. To process a vast amount of neural signals, the number of neural recording front-end channels must also increase within a limited silicon area [23], [24], meaning that the area of the

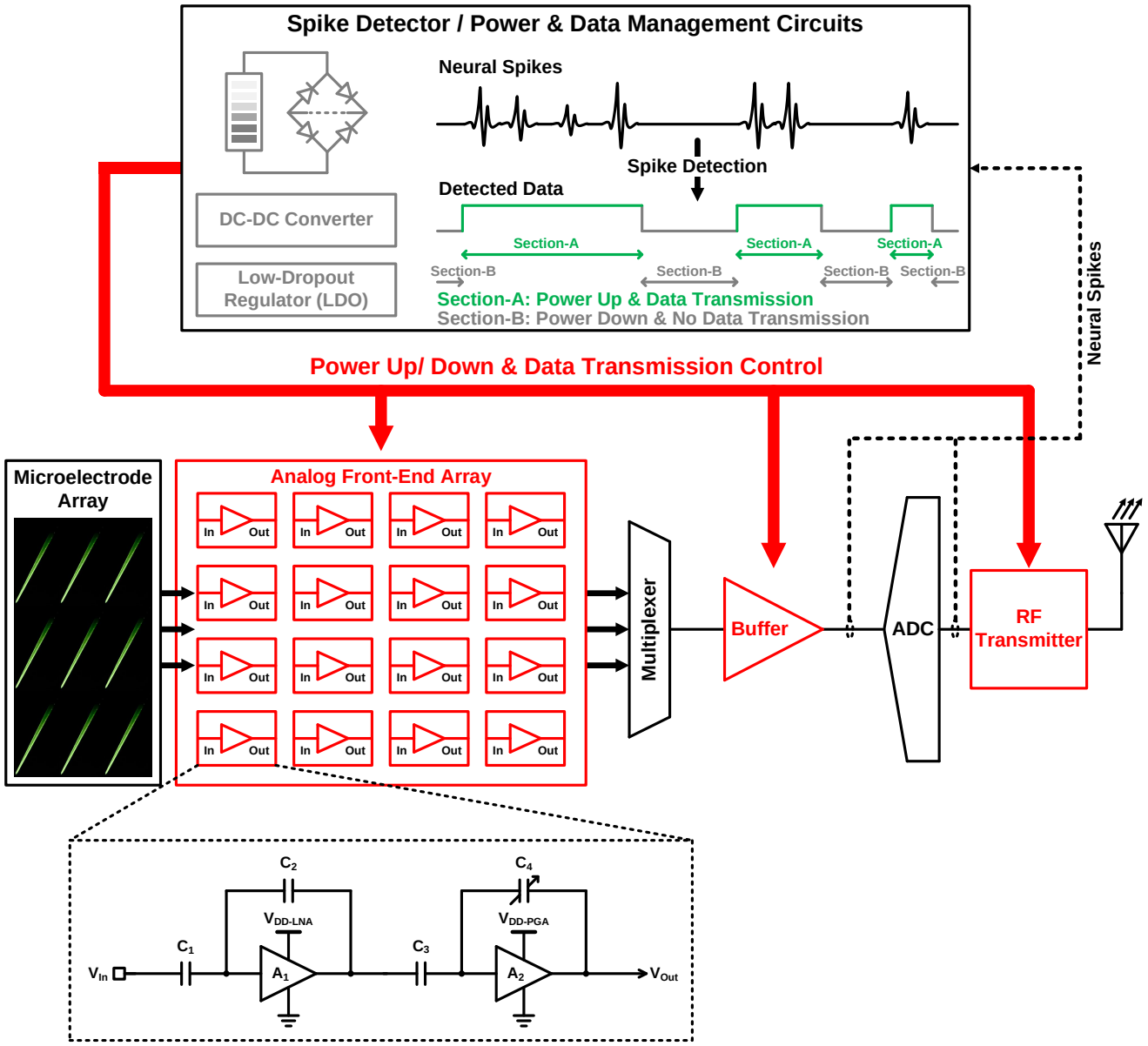


Fig. 4. Neuronal activity-dependent recording system scheduling power and controlling data transmission.

single front-end channel needs to be reduced. After implanting the microelectrode array into the brain, the microelectrode array shows high output impedance (or tissue-electrode impedance), which can cause a loading effect between the electrode output and the input of the front-end channel. To mitigate this loading effect, the input impedance of the front-end channel must be higher than the output impedance of the electrode site through the impedance boosting techniques [25], [26]. In addition, even if electrical stimulation artifacts are coupled to the input of the front-end channel, the front-end channel must process the voltage signal without signal distortion and voltage saturation by widening the system dynamic range [25], [26].

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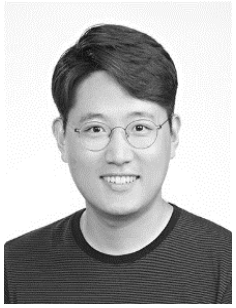

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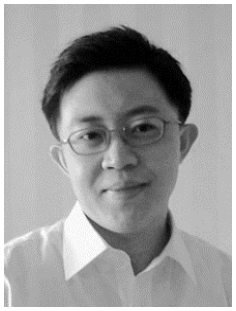

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