Design of a Current-Controlled Oscillator for Wide-Dynamic-Range, Time-Based, Delta-Sigma Modulator

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***Abstract* – This paper presents a design of 15-stage, current-controlled oscillator (CCO) for wide-dynamic-range, time-based, delta-sigma modulator (DSM). The DSM utilizes a time-based quantizer which consists of ring CCO-based integrator and phase extended quantizer. In order to achieve both high loop-gain of the DSM and low-power consumption of the oscillator, the CCO is designed only with inverter delay-cells. In addition, phase extended quantizer is used to add most-significant bit to the DSM output, increasing resolution of the DSM. The designed DSM also utilizes the inherent clocked-averaging property. As a result, the DSM does not need an external dynamic element matching circuit to reduce the effect of the digital-to-analog converter mismatch. The simulation results show that the center frequency and gain of the CCO are near 1.25 MHz and 949 GHz/A under the bias current of 1.2 μA. Through an experiment using the fabricated chip in 65-nm CMOS technology, we confirmed those efficient performances of the designed CCO.**

Keywords—Analog-to-digital converter (ADC), Current-controlled oscillator (CCO), Delta-sigma Modulator (DSM)

I. INTRODUCTION

Time-based, delta-sigma modulators (DSMs) have seen rapid progress in researches during the past decade. Since they leverage more digital-like building blocks instead of classical circuits of DSMs, such as operational transconductance amplifier (OTA) and comparators, they can overcome the performance limitation of the analog circuits in technology scaling trends [1].

Typical time-based, DSMs are composed with time-based quantizer using a ring current-controlled oscillator (CCO) or voltage-controlled oscillator (VCO), analog filter, and feedback digital-to-analog converters (DACs) [1–4]. In these structures, ring CCO acts as a quantizer as well as an integrator due to the relationship between the phase and frequency. Thanks to this property, the CCO-based integrators are not limited by the voltage saturation which occurs in active-RC and G_m-C integrators [1]. In addition, the resolution of the DSMs can be easily enhanced by simply increasing the number of the CCO stages. However, one of the critical issues of the CCO-based integrator is non-linearity. In order to address this problem, recently proposed time-based, DSMs, implemented the CCO-based integrator in the closed-loop as shown in Fig. 1 [5–6]. Since the input current signals of the CCOs become small signal by the subtraction operation of the feedback loop, large distortions in analog-to-digital converters (ADCs) are significantly reduced. Moreover, the XOR phase detector (PD) and dual-CCOs in Fig. 1 provide intrinsic clocked-averaging property, thereby removing external dynamic element matching (DEM) circuits. However, time-based quantizer only using CCOs and XOR PD [see Fig.1 (a)] has limited range of the phase for stable operation, requiring a large number of CCO stage up to 25 [5]. On the contrary, DSM in Fig.1(b) used phase extended quantizer (PEQ) to provide high resolution with the small number of CCO stages [6]. PEQ generates most significant bit (MSB) of the ADC by detecting lead/lag status between the two CCOs. As a result, it achieved wide phase input range of the quantizer and additional resolution

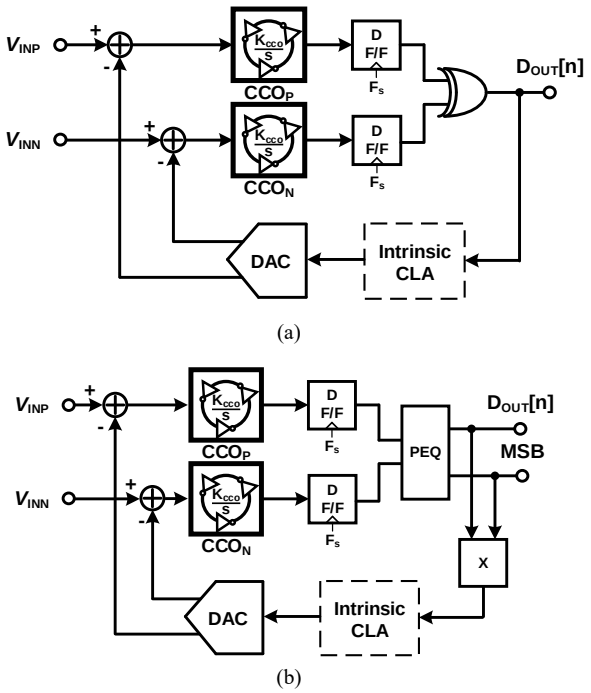

Fig. 1. Block diagram of conventional DSM with CCO-based integrator using (a) XOR PD and (b) phase extended quantizer.

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by only using 15-stage CCOs. However, their target bandwidths are above one megahertz, burdening the decimation filters when they are used for low-frequency applications such as bio-potential acquisition. Especially, the bandwidth requirement of neural recording integrated circuits (ICs) is 10 kHz to record local field potential and action potential. In addition, the dynamic-range must be larger than 70 dB while achieving high noise efficiency.

In this paper, we demonstrate the design of a 15-stage CCO for wide-dynamic-range time-based, DSM. In order to obtain high resolution, PEQ in [6] is used to digitize the analog signal, but the center frequency of the CCOs and sampling rate are significantly reduced for the neural recording application. This paper also explores CCO gain analysis as well as detailed circuit implementation to achieve high loop-gain of the DSM.

II. DESIGN AND MEASUREMENT

Fig. 2 shows the schematic view of the designed time-based quantizer for wide-dynamic-range DSM. The quantizer consists of two 15-stage CCOs, D flip-flops (DFFs), XOR PD, and digital logics to perform lead/lag detection. Input current of the quantizer, I_{INP} and I_{INN}, changes the frequency and phase of CCO_P and CCO_N, and the voltages at each inverter outputs are sampled by DFF. The XOR PD calculates the phase difference between CCO_P and CCO_N which is represented by 15-bit thermometer code, TH[14:0]. The combinational logics in the quantizer generates MSB by extracting the lead/lag status the CCOs. If the phase in the CCO_N leads that of the CCO_P, MSB is 1, otherwise MSB remains at 0.

Examples of the time-based quantization performed by two 3-stage CCOs and XOR PD are shown in Fig. 3. Since the number of inverter delay-cell is odd, transitioning points (TPs), such as 11 or 00 as illustrated in Fig. 3, exists in both CCO_P and CCO_N. The spatial position of the TP moves along the ring CCO with the speed of the oscillation frequency. Therefore, the location of the TP changes by the input current of the CCO. When $I_{INP} - I_{INN} = 0$, TPs of the CCO_P and CCO_N are aligned; as a result, the XOR PD generates the thermometer code of 000. If the input current of each CCOs are different, $I_{INP} - I_{INN} = \Delta I$, the faster frequency of the CCO_P makes the position of the TP of the CCO_P and CCO_N different, resulting the output code of TH[2:0]=001.

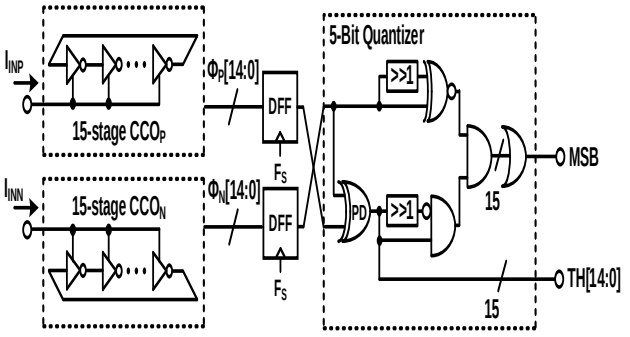


Fig. 2. Schematic view of the designed time-based quantizer using 15-stage CCOs.

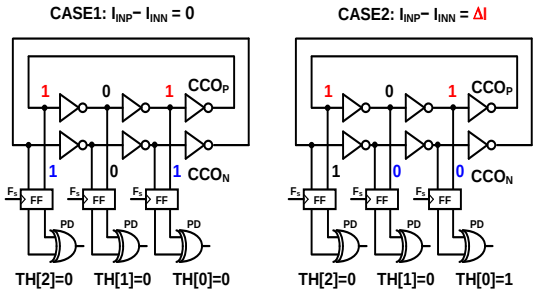


Fig. 3. Examples of the operation of the CCOs and PD.

TABLE I. Target performance of the CCO

Parameters	Specifications
Frequency	1.25 MHz
K_{CCO}	> 500 GHz
Bias current	1.2 μA
Power	< 10 μW

Table I is summarized target performance of the CCO for wide-dynamic-range, time-based, DSM. Since the target bandwidth of the DSM is 10 kHz, the frequency of the CCO is set to be 1.25 MHz where the over-sampling ratio of the DSM is larger than 150. In order to make the signal transfer function of the DSM close to unity and noise transfer function to have a first-order high pass response, the gain of the CCO, K_{CCO}, must be greater than 500 GHz/A. Bias current and power consumption of the CCO should be low enough because the CCO should be applied in the neural recording IC.

To determine the supply voltage of the quantizer and CCO, we simulate propagation delay, and an average power of the single inverter in both 180-nm and 65-nm CMOS process. The length of the inverters is set to be minimum length in each process, and the width of the NMOS are set to be 360 nm for 180-nm process and 130 nm for 65-nm process, in order to make the ratio of the width and length of the NMOS in both processes as two. The ratio between PMOS and NMOS was set to be four, due to their electron mobility difference. Considering a single-ended ring oscillator structure, inverters having a same width and length with a prior stage are loaded in each structure.

Fig. 4 shows the simulation result of the propagation delay of the inverters which were designed in 180-nm and 65-nm process, respectively. For the case of the 180-nm inverter, the propagation delay drastically increases when the supply voltage is lower than 0.8 V. On the contrary, the 65-nm inverter maintains decent delay performance even though it operates under the 0.4 V supply voltage. In addition, average power consumption of each inverters is simulated and it is shown in Fig. 5. The result shows that the 65-nm process consumes more power when the supply voltage is higher than 1.2 V. However, when the supply voltage is lower than 1.2 V, 65-nm process inverter shows better power consumption. Therefore, we define the supply voltage of the CCO-based quantizer as 0.4 V, considering the power and delay performance.

In order to obtain large K_{CCO}, we analyze the gain of the ring CCO. When the ring CCO consists of N-stage inverters and input current of I_{IN}, the oscillation frequency, f_{osc}, of the CCO can be expresses as [7, 8]:

$$f_{osc} = \frac{I_{IN}/N}{1.05N(V_{SW})C_L} = \frac{I_{IN}}{1.05N^2(V_{SW})C_L} \quad (1)$$

where V_{SW} is peak-to-peak output voltage of the inverter, C_L is load capacitor. K_{CCO} can be obtained by differentiating the equation (1).

$$K_{CCO} = \frac{1}{1.05N^2(V_{SW})C_L} \quad (2)$$

From equation (2), K_{CCO} is maximized by reducing V_{SW} and C_L, which are the function of CMOS width and length. Since the bias current of I_{IN} is fixed with 1.2 μA, V_{SW} is determined by the on-resistance (R_{ON}) of the transistors in the inverter delay cell.

Fig. 6 shows the simulation result of the CCOs having different inverter length. The length of the inverters (L) are varied from 60 nm to 2100 nm, and the widths were selected to set V_{SW} around 300 mV. Ideal capacitors are attached to each outputs of the delay cells and the value of the capacitors were adjusted, so that the frequency of the all oscillators can become 1.25 MHz when the input current, I_{IN}, is 1.2 μA. The overall results show that the K_{CCO} at I_{IN} = 1.2 μA increases as L reduces. This is because the shorter L reduces R_{ON} and V_{SW}, thereby enhancing K_{CCO} which is described in equation (2). Using a minimum length provides highest K_{CCO}, but it makes the CCO vulnerable to process variation. For example, if the length of the CMOS is 65 nm, the fabricated length of MOS in each delay cell will more vary than that of the delay cells in the CCO with L=400 nm, because 65 nm is close to photolithography resolution limit. Therefore, we chose L to be 250 nm to make K_{CCO} as high as possible while alleviating the process variation.

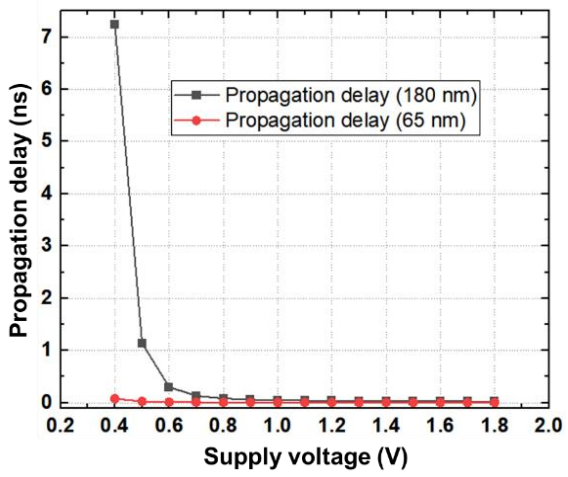


Fig. 4. Comparison of the simulated propagation delay between 180-nm and 65-nm process inverters.

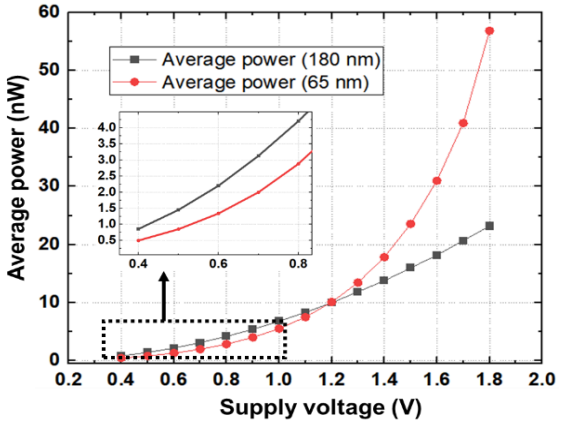


Fig. 5. Comparison of the simulated average power between 180-nm and 65-nm process inverters

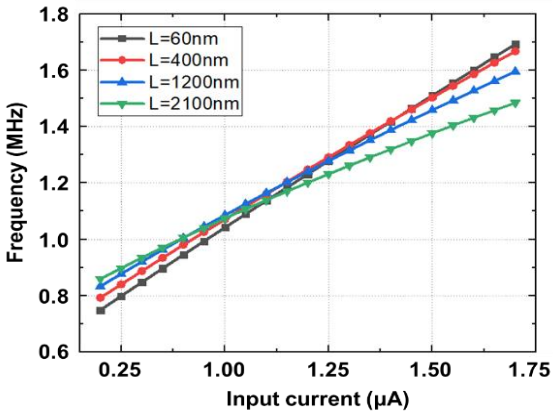


Fig. 6. Simulated transfer curve of the CCO with different inverter length.

The effect of the C_L is also simulated by changing the capacitance from 35 fF to 200 fF, and the results are described in Fig. 7. Fig. 7 indicate that the load capacitor should be minimized to achieve high K_{CCO}.

Fig. 8 is the layout of the designed 15-stage CCO. High threshold voltage devices are used to adjust V_{SW} near 300 mV. The widths of the NMOS and PMOS are chosen to be 10 μm and 40 μm to achieve the target frequency, even though C_L includes the parasitic capacitance due to the output buffer. The area of the 15-stage CCO and the output buffers is 1935 μm^2 which is small enough.

Simulation results of the designed CCO are shown in Fig. 9. The center frequency of the CCO, when I_{IN} = 1.2 μA, is near 1.25 MHz and K_{CCO} is 949 GHz/A. The linear-input-range of the CCO can be estimated as an input-range where the variation of the K_{CCO} is within ±1 %. The simulated linear-input-range is 0.38 μA_{PP}, indicating that the feedback loop is required to use the CCO for neural recording application.

The designed CCO was fabricated in 65-nm CMOS process and measured under the bias condition of I_{IN} = 1.2 μA. Fig. 10 shows that the fabricated CCO operates with the frequency of 1.27 MHz, which is 0.02 MHz faster than the simulation result. The fabricated CCOs was controlled by the G_m-cell, which are composed with PMOS input transistors and current sources, and the CCOs and G_m-cell both shares same power supply because they are cascoded. Since the

fabricated PMOS current source requires larger overdrive voltage than that of the simulation, a voltage across the inverters, V_{SW}, is reduced. As a result, the operating frequency of the CCO is increased according to equation 1.

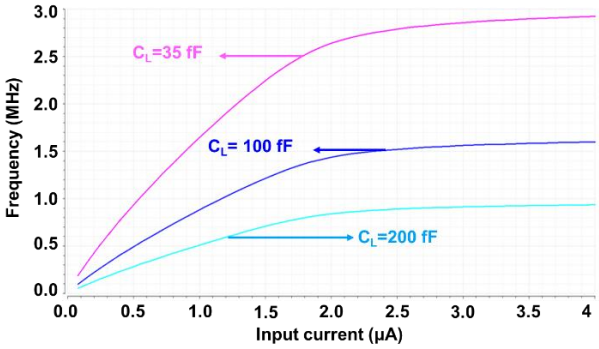


Fig. 7. Simulated transfer curve of the CCO with different load capacitance

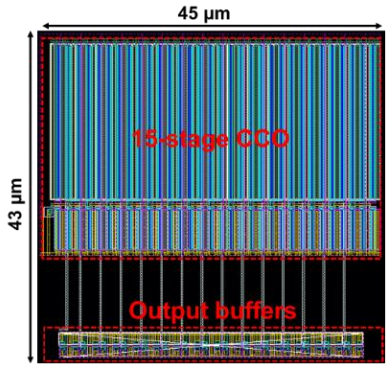
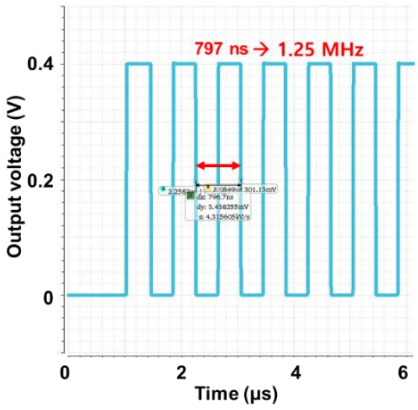
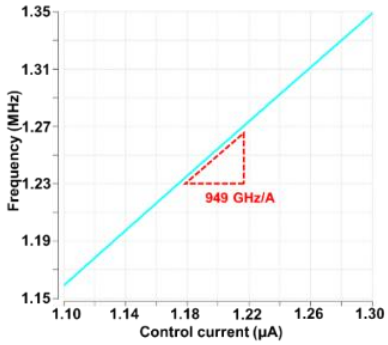


Fig. 8. Layout of the designed 15-stage CCO



(a)



(b)

Fig. 9. Simulated (a) output waveform, and (b) gain of the designed 15-stage CCO.

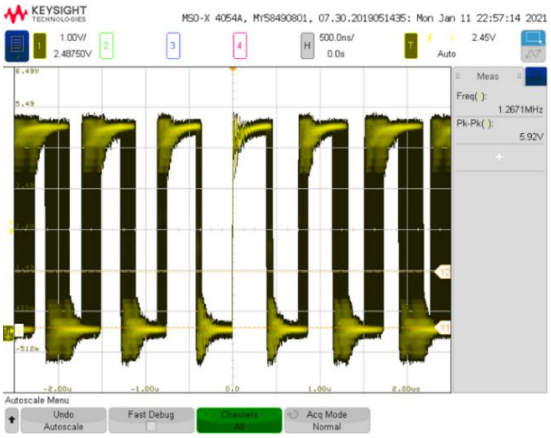


Fig.10. Measured waveform and frequency of the designed CCO

III. CONCLUSIONS

Design of the CCO for wide-dynamic-range, time-based, DSM was demonstrated in 65-nm CMOS technology. Our CCO achieved a high gain of 949 GHz/A at the oscillation frequency of 1.25MHz while consuming small power. The performance of the designed CCO and comparison with the structures having a similar frequency are summarized in Table II. The results suggest that the designed CCO is suitable for the bio-potential acquisition and neural recording applications.

TABLE II. Performance summary and comparison with prior works

Performance	This work	[9]	[10]
Frequency	1.25 MHz	1.28 MHz	500 kHz
Type of OSC	Ring	Ring	Ring
K_{CCO}	949 GHz	N/A	N/A
Supply voltage	0.4 V	0.9 V	1.5 V
Power	570 nW	400 nW	0.4 μW
Process	65-nm CMOS	0.14-μm CMOS	0.35-μm CMOS
Application	ADC	RFID	RFID

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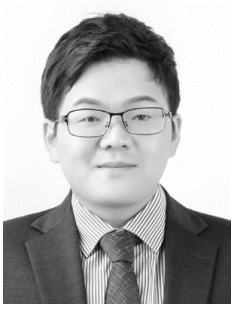

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