Ultra-Low Power Quadrature LO-Generator

Yu Hwan Shin[1], Young Hyun Lim, Sun Eui Park, Ju Yeop Kim, Joo Eun Bang, and Jae Hyouk Choi[a]
Department of Electrical Engineering, Korea Advanced Institute of Science and Technology
E-mail: [1]yuhwan.shin@kaist.ac.kr

***Abstract* – This work presents an ultra-low power quadrature local oscillation (LO) generator for mobile transceivers using a low-dropout (LDO) regulator and low noise voltage-controlled oscillator (VCO). Using a loop-gain stabilizer in LDO, the gain of the error amplifier can be constant in a wide range of load current or reference voltage. The LDO achieves high PSR and fast transient-response. Since the proposed LDO is based on the gate-pole dominant, it can be integrated on-chip. For low phase noise, NMOS-type LC-VCO is used. To reduce phase noise, a tail inductor was added. The LDO using a loop-gain stabilizer shows a fast response of 138 ns and a high PSR of −70 dB at 10 kHz to 1 MHz offset frequency, regulating output at 1.0 V with a 1.1 V supply voltage. The VCO shows a frequency range of 7.675 GHz to 12.301 GHz with a power consumption of 10 mW to 12 mW at a regulated supply of 1.0 V.**

***Keywords*— LC-VCO, LO-generator, Loop-gain stabilizer, Low-Dropout (LDO) regulator, Parallel amplifier**

I. INTRODUCTION

Systems on chip (SoCs) are trends in recent integrated circuits. Multiple functional circuit blocks have multi-power domains in mobile SoC. Especially, the local oscillation (LO) generator is a core cell to support different network standards. LO-signals must satisfy the phase noise requirement with enough frequency range to cover all the network standards safely [1]. Recently, low phase noise signal generation with a tightly limited power budget is required.

In a single chip, the appropriate voltage must be applied to each of the functional circuits from one battery [2] – [3]. Figure 1 shows the most solution in SoC. Most solutions tend to use multiple DC-DC converters to lower the DC voltage level with high power efficiency; after that, each low-dropout (LDO) regulator individually and precisely scales down the voltage. For ultra-low-power consumption, 1.1 V supply voltage was applied, and 0.1 V drop-out voltage is targeted. In this ultra-low-power application, LDO shows high PSRR with the wide reference voltage range for analog circuit application and high PSRR with the wide load current range under the same drop-out voltage for digital circuit application.

a. Corresponding author; jaehyouk@kaist.ac.kr

Manuscript Received Oct. 13, 2021, Accepted Nov. 11, 2021

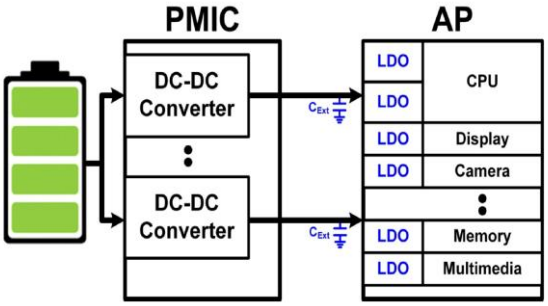

Fig. 1. Multi-power domain in mobile SoC and demands on LDO for Analog/RF/Digital circuit blocks.

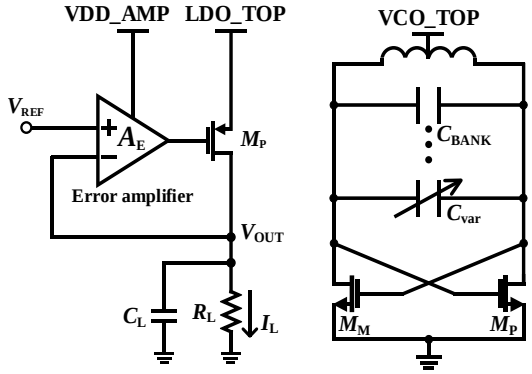

Fig. 2. Architecture of LO-Generator using LDO and VCO.

For signal generators, voltage-controlled oscillator (VCO) is used. As a tradeoff with the area, LC-VCO is mainly used because of its better noise performance than Ring-VCO. With controlling cap-bank and varactor, it could achieve a sufficiently wide frequency tuning range.

The rest of this paper is organized as follows. Section II presents the implementation of the proposed LO-generator using the LC-VCO and the LDO. Section III shows the results and discussion. Section IV provides conclusions.

II. PROPOSED LO-GENERATOR USING LC-VCO AND LDO

A. Overall architecture of the LC-VCO for wide tuning range

As a core element of a signal generator, oscillators that generate AC signals are divided into two mains. Ring oscillator and LC oscillator. Since the ring VCO occupies a much smaller area, it is better in terms of integration and has a broader range for frequency tuning. However, compared to the LC VCO, the noise specification is not good. LC VCO

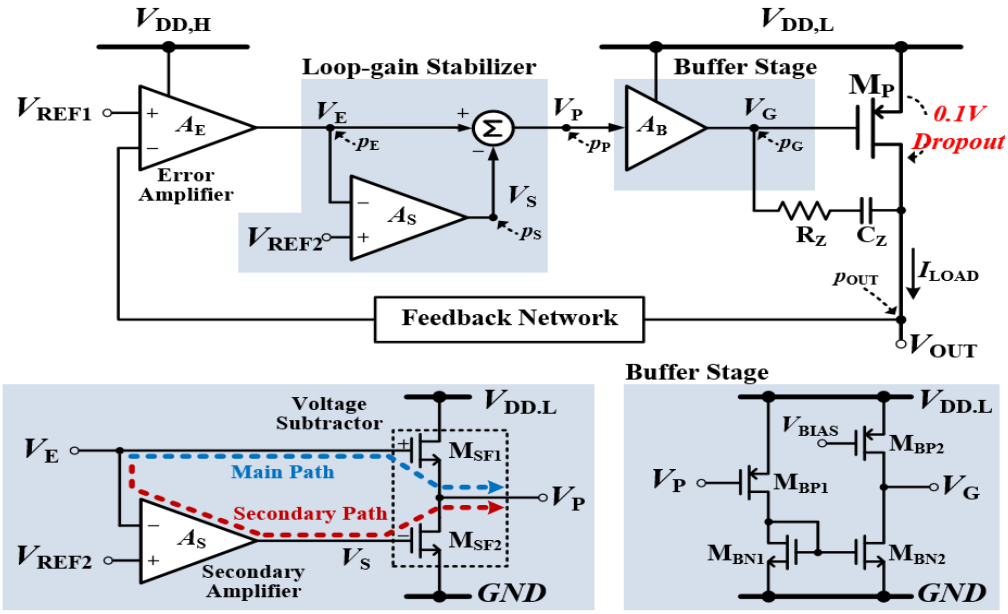

Fig. 3. Overall architecture of the LDO using a Loop-Gain Stabilizer.

has advantages in terms of noise but has disadvantages in terms of tuning range and area [4]. In this paper, we implemented low phase-noise and sufficiently wide-range LC-VCO. Figure 2 shows the architecture of the LO-generator using LDO and VCO.

For a low-phase signal generator, NMOS-type LC-VCO is adopted. The target frequency is 7.4 GHz to 10.98 GHz, which is not that low, so the size of VCO is not extremely large. For wide tuning range, cap-bank and varactor consist of 8 bits and 2 bits, respectively. Each cap-bank was binary-weighted. The LC-VCO was implemented to cover target frequency in all PVT corners. A tail inductor was added to minimize phase noise.

Dividers with even numbers could generate quadrature signals for wide-range applications. With the VCO, implementing dividers can achieve various frequency range quadrature signals.

B. Overall architecture of the LDO using a Loop-Gain Stabilizer

The LDO using a loop-gain stabilizer consists of error amplifier, loop-gain stabilizer, buffer stage, pass-transistor, and output load [5]. The overall mechanism of the LDO is the same as a conventional LDO. To achieve load current and reference voltage robust performance, the loop-gain stabilizer is used as above. Figure 3 shows the overall architecture of the LDO using a loop-gain stabilizer. At the error amplifier output node, loop-gain stabilizer and buffer stage are implemented. In this LDO, to achieve ultra-low drop-out, PMOS is used for pass transistors.

With the loop-gain stabilizer, the error amplifier has the effect of broadening the bandwidth and higher gain. Therefore, the LDO could achieve higher PSR and fast transient- response. It is to make the error amplifier's performance better by trade-off with the power. In the loop-gain stabilizer, the error amplifier's output signal is

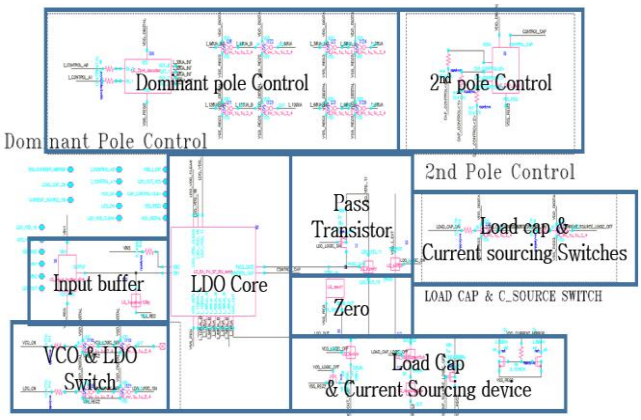

Fig. 4. Overall Schematic of LDO for LC-VCO loads.

strengthened at node V_p by adding the secondary amplifier's amplifying signal. The voltage at the node V_E is robust to variations in load current, $I_{LOAD,}$ or reference voltage, V_{REF1} since the DC-gain of the loop-gain stabilizer is high. Therefore, the gain of the error amplifier can be constant in a wide range of I_{LOAD} or V_{REF1}, which stabilizes the loop gain of the LDO over the whole operating range. The loop-gain with a high gain and a wide bandwidth of the LDO achieves high PSR and fast transient response of the LDO; thus, "High PSR and fast transient-response with a wide range of I_{LOAD} or V_{REF1}" will be available. For biasing, the buffer stage transfers the V_p signal to the output node with desirable dc bias.

Figure 4 shows the overall schematic of the LDO. In addition to the LDO using a loop-gain stabilizer, the schematic consists of a dominant pole control, a 2nd pole control, an input buffer, a switch of VCO and LDO, a load cap, and current sourcing switches. By controlling the capacitor and bias current of the amplifier, the dominant pole's location could be controlled at gate-dominant LDO.

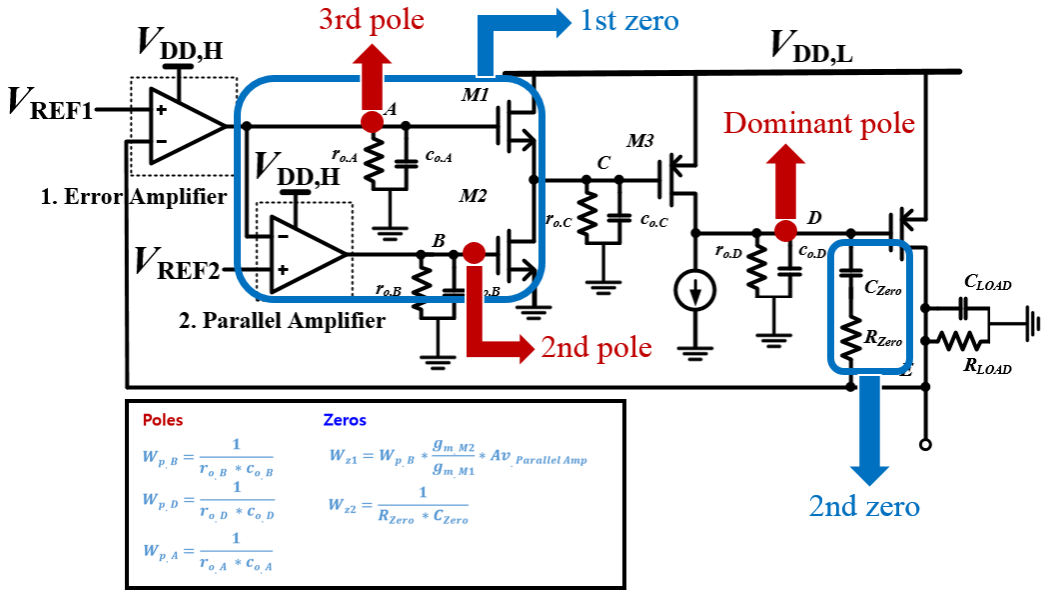

Fig. 5. Poles and Zeros analysis of LDO using a loop-gain stabilizer.

VCO&LDO switch can change the load block from ideal cap to implemented analog and digital circuit blocks (e.g., VCO, digital synthesized block).

C. Analysis of the LDO using a Loop-Gain Stabilizer

For high gain and bandwidth, two-stage error amplifiers were adopted. For small power consumption and size, a parallel amplifier, which uses V_{REF2} as an input, was designed by using a conventional one-stage structure. For high PSR of the amplifier, PMOS input pair was selected in a parallel amplifier. With PMOS pass-gate, type-B error amplifier shows high PSR bandwidth [6]. With loop-gain stabilizer, the LDO could achieve high gain with wide bandwidth.

Figure 5 shows the poles and zeros analysis of the LDO. Using a loop-gain stabilizer, there are three poles and two zeros in a feedback loop. The dominant pole is in the gate of pass-transistor. And 2nd, 3rd pole is each located in the gate of voltage subtractor. The first zero is in the loop-gain stabilizer path, and the 2nd zero is in the output node to gate of the pass-transistor path. By using an additional error amplifier, we could achieve high gain and sufficiently high bandwidth.

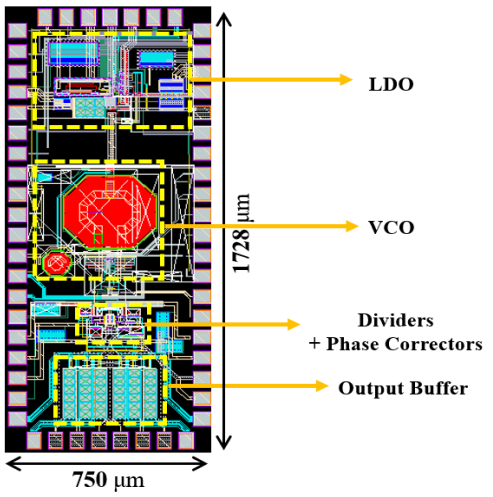

Fig. 6. Layout of the proposed LO-generator with other load blocks.

III. RESULTS AND DISCUSSION

Figure 6 shows the layout of the LO-generator with other blocks. The VCO and LDO are core cells in LO-generator. Fabricated in 40-nm CMOS technology, VCO and LDO used an active area of 0.32 mm^2. For measurement, LO generated signal can be selectively extracted direct or through the divider. Transferred signal pass-through output test buffers and DC-blocking metal-oxide-metal (MOM) capacitors. The output buffer consists of cascaded inverters, where their sizes increased gradually to drive 50-ohm load impedance.

Figure 7 shows the measured spectrum of LO-signals of divide-by-12 and inversely calculated VCO frequency range. It covers high frequency, and wide frequency tuning ranges. Therefore, by dividing 12 the signals, the max and min frequency of LO-signal are expressed in Fig. 7. It covers 7.056 GHz to 11.4 GHz, which is sufficiently high as the target range. By using divider, it could generate quadrature signal for each the even number divider.

Table I shows the phase noise at each PVT corner for each offset frequency. It shows low phase noise as the VCO was LC-based. For all PVT corners, the target frequency range is achieved.

Figures 8 and 9 show the measured gain, bandwidth, and PSRR of LDO using a loop-gain stabilizer. In Fig. 8, the input voltage level was swept at the input range of 0.8 V to 1.4 V. The measured picture is the case of 1.0 V as input voltage. Parallel amp's dc gain was higher than 25.1 dB, and the bandwidth was higher than 1.2 MHz. To use in ultra-low power consumption LDO, the power consumption of parallel

amp was only 18 uW. Regardless of the process and temperature variation, the performance was almost similar. In the case of the general amplifier, it could achieve a high gain (> 54.5 dB) and a wide bandwidth (> 19.58 MHz) at an input voltage of 0.85 V. This specification was achieved in power consumption of 1.08 mW. Compared to power consumption, it was found that the performance of the parallel amplifier was better.

In Fig. 9, for realistic conditions, *LC* VCO was used as a load of LDO. When the LDO top voltage is 0.95 V, the amp power supply is 1.8 V, VCO top voltage is 0.85 V, and VCO current is 20mA, the PSR in frequency domain was shown as Fig. 9. The voltage drop was only 0.1 V. Depending on the process and temperature, even in the worst case, the performance was -60 dB before 1 MHz. After 1 MHz, it shows a good performance of less than −40 dB, regardless of process and temperature.

In Fig. 10, for realistic conditions, *LC* VCO was used as a load of LDO. It shows the output noise of LDO, which is critical to VCO. When the LDO top voltage is 1.1 V, and the VCO top voltage is 0.85 V, the PSR in the frequency domain was shown as Fig. 10. Regardless of process and temperature, the output noise was lower than -149.8 V/$\sqrt{\text{Hz}}$ at 1 kHz offset and -167 V/$\sqrt{\text{Hz}}$ at 100 kHz offset.

Table II shows the summary of specifications of LDO and prior arts. Performance metrics are categorized with drop voltage, PSR, droop voltage, settling time, FOM, and regulation. It consumes more power than other prior arts. However, PSR and other performances are relatively better than the prior art. Especially, PSR and settling time is much better than prior art due to the loop-gain stabilizer.

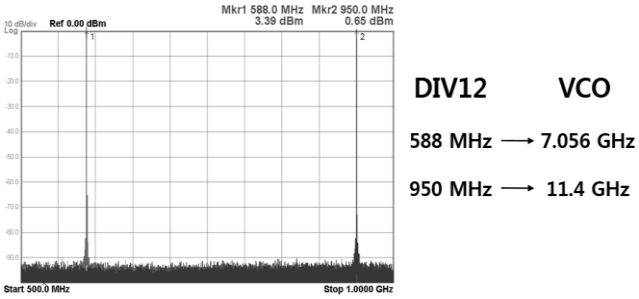

Fig. 7. Measured Spectrum of the LO-signal of divide-by-12 and inversely calculated VCO frequency range.

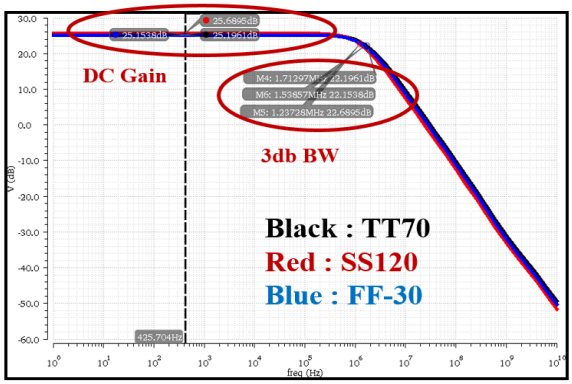

Fig. 8. Measured Parallel amp's gain & bandwidth, AC Simulation when input voltage is 1.0 V.

IV. CONCLUSION

The proposed ultra-low power quadrature LO-generator was implemented by using LC-VCO, LDO with a loop-gain stabilizer, and divider. In LDO, to increase the amplifier's gain and bandwidth, a parallel amplifier was proposed. Due to the loop-gain stabilizer, high gain and bandwidth with extremely small power consumption were achieved. The PSR was under -60 dB before 1 MHz, the settling time was 138 ns at 100 ns edge, and the droop was 1.18 ms at the same condition. With low noise and high PSR LDO, LC-VCO achieved the performance with low phase-noise and more than 40% tuning range at any PVT corner. Implementing dividers with various even numbers can generate quadrature signals with various frequency ranges. This LO-generator was fabricated in a 40-nm CMOS process. The proposed LO-generator is a good candidate for the mobile SoC.

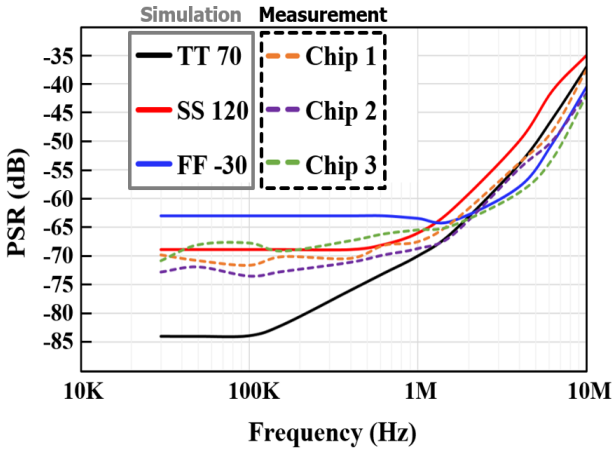

Fig. 9. Measured PSRR when VCO TOP voltage is 0.85 V.

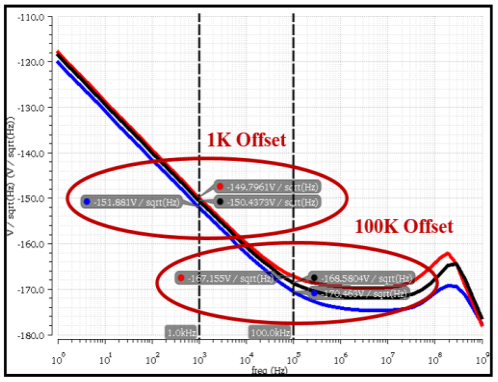

Fig. 10. Measured Output Noise when VCO TOP voltage is 0.85 V.

ACKNOWLEDGEMENT

This work was supported by the 'DGIST R&D Program of the Ministry of Science and ICT(21-IJRP-01)', National R&D Program through the National Research Foundation of Korea(NRF) funded by the Ministry of Science and ICT(2020M3H2A1078045)), and the chip fabrication was supported by the IC Design Education Center.

TABLE I. Simulated phase noise of LC-VCO at three extreme PVT variations and various frequencies

	Frequency	100K	400K	1M	10M	20M	45M
SS	6.9549GHz	-98.58	-111.3	-119.4	-139.5	-145.6	-152.6
SS	11.678GHz	-94.54	-108.2	-116.6	-137.1	-143.5	-151.6
TT	7.6748GHz	-100.9	-113.6	-121.8	-141.9	-147.9	-154.8
TT	12.301GHz	-93.88	-107.9	-116.5	-137	-143.3	-151.1
FF	8.5997GHz	-103	-115.8	-124	-144.1	-150.1	-157.1
FF	13.034GHz	-92.87	-107.7	-116.6	-137.5	-143.7	-151.2

* The unit of phase noise is dBc/Hz.

TABLE II. The desired specifications and simulation results of LDO

	FFRC	PSR Enhancer	Wide Loading Range	Low Power Fast	FVF with DSMFC	Full-Spectrum PSRR	**Proposed LDO**
Paper	JSSC 2010	JSSC 2014	TCAS2 2012	JSSC 2010	TCAS1 2014	TCAS1 2015	
	OFF CHIP	ON-CHIP	ON-CHIP	OFF CHIP	ON-CHIP	ON-CHIP	**ON-CHIP**
Load Cap (F)	4 u	100 p	20 p	1 u	10 p - 10 n	N/A	**10 p – 100 p**
CMOS Technology	0.13 um	0.18 um	0.13 um	90 nm	65 nm	65 nm	**40 nm**
V_{IN} (V)	>1.15	1.8	1.15 – 1.4	1	1.2	1.15	**1.1**
P_Q (W)	57.5u	99 u	51.8 u	9.3 u	28.44 u	103.5 u	**1.27 m**
Output Noise @100kHz (uV/$\sqrt{\text{Hz}}$)	N/A	0.27	N/A	N/A	N/A	N/A	**0.0044**
V_{DROP} (V)	> 0.15	0.2	0.2	0.1	0.2	0.15	**0.1**
V_{OUT} (V)	1	1.6	0.95 – 1.2	0.9	1	1	**1**
$I_{MIN} - I_{MAX}$ (A)	0 – 50 m	0 – 50 m	50 uA – 50 m	0 – 50 m	0 – 50 m	0 – 10 m	**300 u – 50 m**
PSR (10KHz) (dB)	60	62	70	55	52	20	**75**
PSR (1MHz) (dB)	67	70	40	45	N/A	20	**70**
PSR (10MHz) (dB)	56	37	15	35	N/A	20	**41**
ΔV_{OUT} @T.Edge (V)	15 m @10ns	120 m @100ns	56 m @200ns	10 m @10ns	40 m @100ns	82 m @200ps	**1.18 m @100ns**
Settling time @T.Edge (s)	N/A	6 u	400 n	N/A	N/A	N/A	**138 n @100ns**
FOM* (s)	N/A	0.26 p	0.017 p	N/A	N/A	5.74 p	**0.012 p**
Load regulation @T.Edge (mV / mA)	0.048 @100ns	0.14 @100ns	0.056	0.082	0.034	1.1	**0.00037 @100ns**
Line regulation @T.Edge (mV / V)	26	75 @100ns	8.1	14	8.89	37.1	**0.266 @100ns**

* FOM = $T_R \frac{I_Q}{I_{MAX}} = \frac{C \times \Delta V_{OUT}}{I_{MAX}} \times \frac{I_Q}{I_{MAX}}$, Where I_Q is quiescent current which is P_Q/V_{IN} (Max).

REFERENCES

[1] H. Yoon et al., "A 0.56–2.92 GHz Wideband and Low Phase Noise Quadrature LO-Generator Using a Single LC-VCO for 2G–4G Multistandard Cellular Transceivers," in *IEEE Journal of Solid-State Circuits*, vol. 51, no. 3, 2016, pp. 614-625.

[2] X. Wang and P. P. Mercier, "A Dynamically High-Impedance Charge-Pump-Based LDO With Digital-LDO-Like Properties Achieving a Sub-4-fs FoM," in *IEEE Journal of Solid-State Circuits*, vol. 55, no. 3, pp. 719-730.

[3] P. Liu, S. Huang, Q. Duan, Q. Zhu and Z. Meng, "A Low-Quiescent Current Off-Chip Capacitor-less LDO Regulator with UGCC Compensation," *2019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, 2019, pp. 1-3.

[4] Razavi, *RF Microelectronics*. Englewood Cliffs, NJ: Prentice-Hall, 1998.

[5] Y. Lim et al., "An External Capacitor-Less Ultralow-Dropout Regulator Using a Loop-Gain Stabilizing Technique for High Power-Supply Rejection Over a Wide Range of Load Current," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no.11, 2017, pp. 3006-3018.

[6] V. Gupta, G. A. Rincon-Mora and P. Raha, "Analysis and design of monolithic, high PSR, linear regulators for SoC applications," *IEEE International SOC Conference, 2004. Proceedings.*, 2004, pp. 311-315.

Yu Hwan Shin was born in Geoje, South Korea, in 1999. He received the B.S. degree in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2021. He is currently pursuing the M.S. degree with the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea.

His research interests include CMOS analog/mixed integrated circuit (IC) designs, especially high-speed clock/frequency generation systems.

Young Hyun Lim (Member, IEEE) was born in Gyeongju, South Korea, in 1992. He received the B.S. degree in electrical engineering from the Ulsan National Institute of Science and Technology (UNIST), Ulsan, South Korea, in 2015, where he is currently pursuing the combined M.S./Ph.D. degree.

He was an Intern with Qualcomm, Inc., San Diego, CA, USA, where he was involved in designing the phase-locked loops (PLLs) in the upcoming TRXs. His research interests include low-power and high-performance analog, mixed-signal, and RF integrated circuits for emerging wireless/wired standards. Mr. Lim was a recipient of the IEEE Student Research Preview (SRP) Award for the outstanding poster at ISSCC in 2019, the Korean Government Scholarship (GPF), and the Honorable Mention and the Bronze Prize at the 24th and 25th Samsung Human-Tech Paper Awards in 2018 and 2019, respectively.

Sun Eui Park (Student Member, IEEE) was born in Seoul, South Korea, in 1994. She received the B.S. and M.S. degrees in electrical engineering from the Ulsan National Institute of Science and Technology (UNIST), Ulsan, Korea, in 2017 and 2020, respectively. She is currently pursuing the Ph.D. degree with the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea.

Her research interests include analog, mixed-signal IC designs, especially low-power and low-jitter clock generation circuits.

Ju Yeop Kim (Student Member, IEEE) was born in Changwon, South Korea, in 1994. He received the B.S. and M.S. degrees in electrical engineering from the Ulsan National Institute of Science and Technology (UNIST), Ulsan, Korea, in 2017 and 2020, respectively. He is currently pursuing the Ph.D. degree with the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea.

His current research interests include CMOS analog/mixed IC designs, especially millimeter-wave clock/frequency generation systems.

Joo Eun Bang (S'18) was born in Busan, South Korea, in 1995. She received the B.S. and M.S. degrees in electrical engineering from the Ulsan National Institute of Science and Technology (UNIST), Ulsan, South Korea, in 2018 and 2020, respectively. She is currently pursuing the Ph.D. degree with the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea.

Her current research interests include low-power and high-performance analog, mixed-signal, and RF integrated circuits for emerging wireless/wired standards.

Jae Hyouk Choi (Senior Member, IEEE) was born in Seoul, South Korea, in 1980. He received the B.S. degree (*summa cum laude*) in electrical engineering from Seoul National University, Seoul, in 2003 and the M.S. and Ph.D. degrees in electrical and computer engineering from the Georgia Institute of Technology, Atlanta, GA, USA, in 2008 and 2010, respectively.

From 2010 to 2011, he was with Qualcomm, Inc., San Diego, CA, USA, where he was involved in designing multi-standard cellular transceivers. In 2012, he joined the Ulsan National Institute of Science and Technology (UNIST), Ulsan, South Korea, as a Faculty Member. Since 2019, he has been an Associate Professor with the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea. His research interests include low-power and high-performance analog, mixed-signal, and RF integrated circuits for emerging wireless/wired standards.

Dr. Choi has been a TPC Member of the IEEE International Solid-State Circuits Conference (ISSCC) since 2017 and the IEEE European Solid-State Circuits Conference (ESSCIRC) since 2016. He was the Country Representative of South Korea for the ISSCC Far-East Region in 2018. He has been a Distinguished Lecturer (DL) of the Solid-State Circuits Society (SSCS) since 2020.