A Fully Integrated Fine-Grained Dual-Output Switched-Capacitor DC-DC Converter for Low-Power Applications

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Abstract **- This paper presents a fully integrated fine-grained dual-output switched-capacitor DC-DC converter that satisfies the requirements of low-power applications. In order to generate a large number of VCRs for dual-output, the converter is partially modified from an algorithmic voltage-feed-in (AVFI) topology, which adds one more output terminal to the original topology. In addition, since the presented converter scheme separates a converter into two individual converters and generates independent VCRs for each converter, a larger number of VCRs can be obtained than that of AVFI converters when not using partitioning techniques. A test chip was fabricated using 0.18 µm standard CMOS process. The measured result shows conversion efficiencies higher than 86.3 % over a range of output voltages from 0.3V to 3.0V for a 3.3V input. In this voltage range, 39 VCRs are distributed for 10 power cells.**

Keywords**—Algorithmic Voltage-feed-in, DC-DC Converter, Dual outputs, On-chip converter, Switched-capacitor DC-DC converter**

I. INTRODUCTION

In recent low-power applications such as mobile, portable, or IoT devices, most of the functional circuit blocks are usually integrated together on a single chip [1]-[3]. In order to power these blocks with high efficiency, it may be better that the power conversion circuits are also integrated with other circuit blocks, because a lot of energy (e.g. IR drops) may be lost when delivering power on the circuit board. Even in a low-power system, losses during power conversion may account for a very large proportion of the overall power of the system, which will be a problem in terms of the power budget.

Since the size of systems is typically very compact, if the power circuit contains large components such as passives they can become a bottleneck in terms of commercial value and user-friendliness. Furthermore, the use of many off-chip components on the circuit board will increase the bill-of-materials cost [4], so it is necessary to reduce the use of them.

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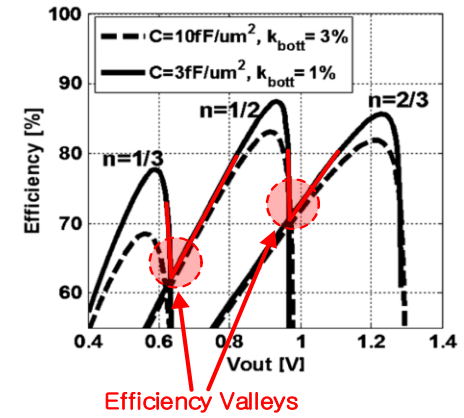

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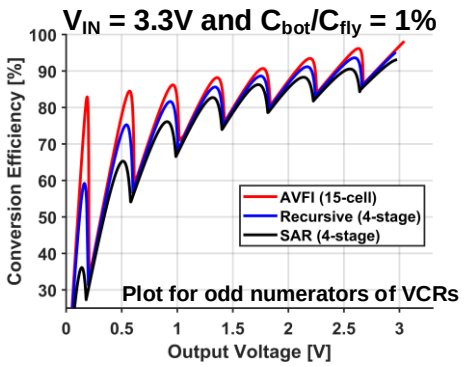


(b)

Fig. 1. Conversion efficiencies versus output voltage with (a) three available topologies [5] and (b) algorithmic VCR configurations (simulated results for [6], [7], and [8]).

The excellent dynamic performance required by the recent low-power high-speed systems also encourages on-chip integration [9]. Because these systems require just-in-time power conversion through fast feedback between inputs and outputs, the regulation speed limitation due to the large trace capacitance on the circuit board can adversely affect system performance and power efficiency. In summary, power conversion circuits have been highly integrated in low power applications.

As a fully integrated power conversion circuit, a low-dropout (LDO) regulator and a switched-capacitor (SC) converter can be considered. LDO regulators are easily distributed across a chip and individually power each load in a multiple supply domain thanks to the high on-chip

integration capability, thereby reducing IR-drop [10]. LDO regulators are very suitable for systems requiring dynamic voltage scaling (DVS) because they show fast response and excellent linearity. However, the conversion efficiency decreases severely when generating lower output voltages using LDO regulators. In other words, LDO regulators can maintain high efficiency only in a narrow voltage range.

SC converters, like LDO regulators, regulate output voltages very rapidly and can be highly integrated. On the other hand, SC converters can be used for a wider voltage range compared with LDO regulators because the conversion efficiency is not significantly reduced for low input voltages. However, SC converters require a large number of voltage-conversion-ratios (VCR) for fine voltage regulation, but only generate a limited number of voltage levels due to their discontinuous topologies for VCR configurations. This drawback of SC converters leads to an efficiency valley between the optimum output voltages corresponding to two adjacent VCRs [5] [see Fig. 1 (a)].

In order to reduce the depth of these efficiency valleys, the method of increasing the number of VCRs by simply combining several discontinuous topologies has been popularly used. However, this method causes the following two considerable problems [11]. With a large number of topologies, each topology often adds additional transistors, resulting in additional series resistances in the adjacent topologies. In addition, a rapid topology switching between different topologies may result in control overhead, which in turn causes a large power loss.

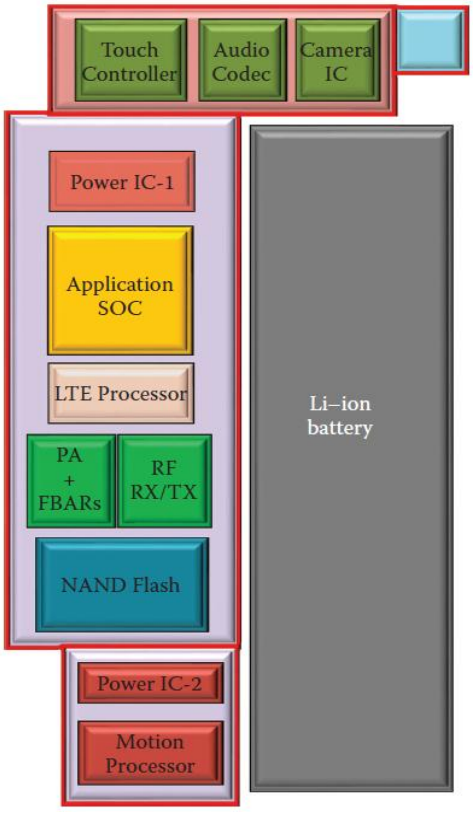


Fig. 2. Typical smartphone teardown showing different voltage domains [12].

Hence, to increase the number of VCRs, many-ratio SC converters have been devised [13], [6]; these studies were followed by [7],[8],[14] with negligible efficiency degradation in return for increased ratio programmability. Similar to applying the cell-based methodology in implementing digital integrated circuits, these converters are designed to generate desired VCRs by synthesizing several unit power cells. For the number of unit cells used, the SAR (the first algorithmic SC converter) [6] and recursive (improved version of SAR, with higher output conductance than that of SAR) [7] converters generate binary weighted VCRs and the algorithmic voltage-feed-in (AVFI) (with lower bottom-plate loss that that of other converters) converter [8] generates rational VCR. Thus, they easily generate a large number of VCRs with high programmability, which in turn allows the converters not only to generate fine-grained output voltages but also to overcome the efficiency drops that occur when converter configurations are changed [see Fig. 1 (b)].

Meanwhile, in recent low-power applications, since various circuit blocks are integrated together on a single chip as shown in Fig. 2, the demand for power conversion circuits that is capable of supplying power to multiple voltage domains is increasing. Therefore, this paper presents a dual-output power conversion circuit based on a many-ratio SC converter.

Section II describes the structure of the presented converter. Section III shows the measurement setup and results. Finally, Section IV concludes this paper.

II. FINE-GRAINED DUAL-OUTPUT SWITCHED-CAPACITOR DC-DC CONVERTER

A. Algorithmic voltage-feed-in (AVFI) topology

The converter presented in this paper is based on the AVFI converter among the introduced many-ratio SC converters. AVFI can have an arbitrary rational ratio (both step-down and step-up) according to the framework as shown in Fig. 3. AVFI offers fine-grained VCRs with good output conductance, and its switching loss is further optimized by selectively using the Dickson and series-parallel configurations and reducing the bottom-plate voltage swing of each flying capacitor. As a result, the conversion efficiency gets better than SAR and recursive converters [see Fig.1 (b)]

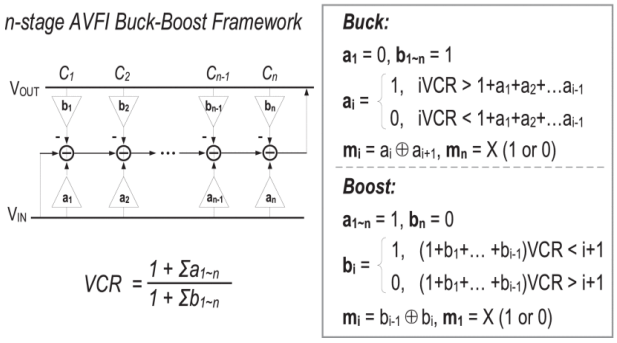


Fig. 3. AVFI topology for the rational buck-boost conversion [8].

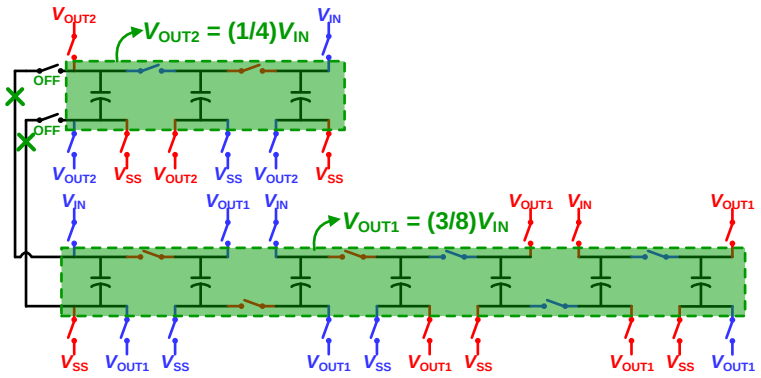


Fig. 4. An example of the dual-output SC converter with many rational ratios by arbitrarily separating cascaded power cells into two individual converters (VCR_1 = 1/4 and VCR_2 = 3/8).

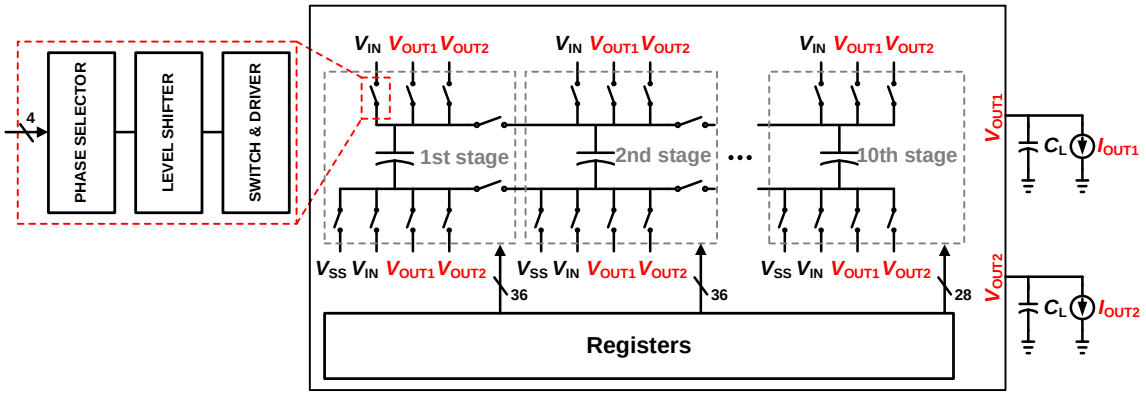


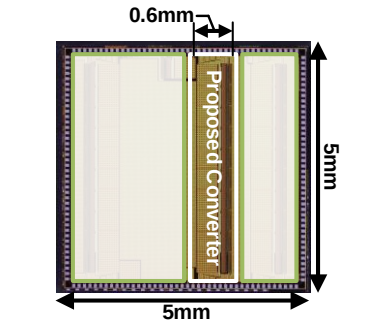
Fig. 5. Overall circuit diagram of the presented dual-output SC converter.

In addition, all power cells in an AVFI converter have the output terminal in step-down mode (input terminal in step-up mode), while SAR and recursive have it at only the final power cell. This makes it easy to modify the topology and allows the converter to support dual-output. That is, it is possible to support dual-output while retaining the advantages of AVFI converter (high power conversion efficiency and rational VCRs) through simple modification.

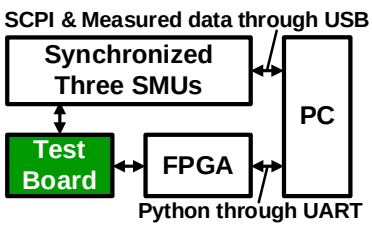
B. Implementation of dual-output SC DC-DC converter

Just as inductive converters generate multiple-output with a single inductor [15], SC converters can have multiple-output using switching operations with multiple phases. However, as shown in Fig. 4, if each power cell has two output terminals (V_{OUT1} and V_{OUT2}) and connections between the power cells are arbitrarily reconfigured, two output voltages with different VCRs can be obtained from a SC converter without using multiple-phase. In other words, cascaded power cells (using cell connection switches at either top- or bottom-plate of flying capacitors) are separated into two individual converters, and each converter has an independent rational ratio according to the AVFI's configuration algorithm. Through this separation, a large number of VCRs can be obtained at dual-output, and full power cell utilization also can be achieved without any complicated partitioning techniques.

As shown in Figure 3, the maximum denominator (in step-down mode) of the VCR is one greater than the number of power cells, thus if an AVFI converter consisting of n power cells is divided into two individual converters with x and y



(a)



(b)

Fig. 6. (a) Chip micrograph and (b) measurement setup

TABLE I. Performance summary and comparison of the dual-output SC converter

Dual-Output SC Converters	**This Work**	**[9] *JSSC*, 2015**	**[10] *Access*, 2018**	**[5] *TCAS-I*, 2018**	**[11] *TVLSI*, 2019**
Process	0.18 µm	0.35 µm	0.18 µm	65 nm	0.13 µm
Number of VCRs (Pairs)	39	4 (2)	8 (4)	2	2
V_{IN} [V]	3.3	1-1.8	1	1.05-1.4	1.5
V_{OUT} [V]	0.3-3.0	2, 3	(1.49, 0.47), (1.91, 0.98) (1.97, 1.97), (2.85, 1.88)	0.55, 1	0.44, 0.88
I_{OUT} [mA]	0.1-1	12 (Ext. cap)	0.04, 0.06, 0.08, 0.1	0.35, 0.01	12
Efficiency [%]	> 86.3	< 90	< 85.26	< 78	< 78

power cells, two VCRs with the maximum denominators (in step-down mode) of x+1 and y+1 can be obtained. Therefore, it is possible to generate a larger number of VCRs than the number of VCRs that AVFI can have using the presented converter when performing full power cell utilization without applying partitioning techniques.

III. MEASUREMENT AND RESULTS

To verify the performance of the presented SC converter, a test circuit including ten power cells was designed (see Fig. 5). This circuit contains a dual-output SC converter with 10 SC power stages and registers. A flying capacitor within each SC power stage is an on-chip MIM capacitor with 2.5 nF. Each reconfigurable switch consists of a phase selector, level shifter (converting 1.8V to 3.3V), and power switch (I/O transistor) with a gate driver. The registers were used to store data for the phase selector to configure VCRs of the converter. (The phase selector set by the data provides control to turn each switch on or off at the desired phase.) In addition, in order to experiment with the designed test circuit, a chip was fabricated using a 0.18 µm CMOS process, occupying an area of 0.6 mm × 5 mm [see Fig. 6 (a)].

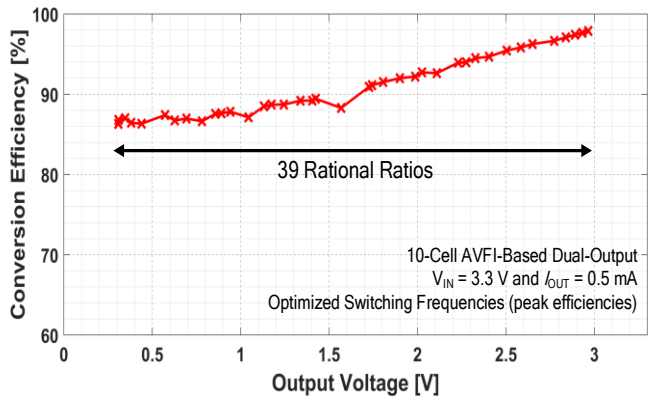


Fig. 7. Measured conversion efficiencies of the presented dual-output SC converter

Because the test chip is measured under a very large number of VCRs, switching frequencies, and load conditions, manual measurement for all test conditions may bring a large time cost. Hence, the test chip was measured by configuring an automated measurement environment as shown in Figure 6 (b). The switch configuration parameters corresponding to the desired VCRs are calculated using the Python program on the PC. These parameters are converted into electrical signals by the FPGA and transmitted to the test chip via UART. Additionally, in order to perform repeated measurements for several parameter combinations, the measurement instruments were completely automated using standard commands for programmable instruments (SCPI).

The presented dual-output SC converter with ten power cells shows the conversion efficiencies over the output voltages from 0.3V to 3.0V for a 3.3V input voltage and two 0.5mA load currents (see Fig. 7). The measured efficiencies are the results of operating the converter at the optimum switching frequencies. Since the measurements were performed for 39 rational ratios, high efficiency is maintained (higher than 86.3% for all VCRs) with negligible efficiency valleys.

For the key specifications of dual-output SC converters, this work and the previously proposed works are compared in Table I. It can be seen that there is little reduction in conversion efficiency over a very wide output voltage range, and the number of VCRs is much larger than other converters.

IV. CONCLUSION

This paper presents a fully integrated SC DC-DC converter with dual outputs. By adding an output terminal to AVFI SC converter, the presented converter supports dual-output with many VCRs. In addition, using the scheme of separating a converter into two individual converters, the converter can have more rational VCRs compared with the original AVFI converter when partitioning techniques are not applied. A test chip fabricated using 0.18 µm CMOS process shows not only high conversion efficiencies over a wide output voltage range but also a much larger number of VCRs than the previously presented dual-output SC converters.

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His research interests include energy-efficient power management integrated circuits.

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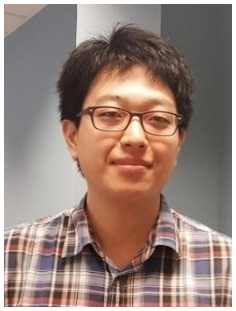

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