Electrical Neural Recording System for Use in the Brain and the Peripheral Nerve

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***Abstract* – This paper presents the electrical neural recording system for monitoring neural spikes in the brain and the peripheral nerve. The implemented recording system is composed of the flexible electrode array, the recording front-end integrated circuit (IC), the ground sheet, and the flexible cable. The recording front-end IC amplifies weak neural spikes residing in about 1 kHz bandwidth. Amplified neural spikes are then digitized through the successive-approximation-register analog-to-digital converter (SAR ADC) with a 10-bit resolution. The system operation is first verified using the artificial neural spike generator. Then, the system is applied to the *in vivo* experiment using the rat. The presented electrical neural recording system successfully monitors neural spikes in the brain and the peripheral nerve while consuming only a few μW power per channel. The recording front-end IC is fabricated using a 1-poly 6-metal (1P6M) 180-nm standard CMOS technology.**

***Keywords*—Brain-machine interface, Double-high-pass filter, Electrical neural recording, Narrow-band buffer, Neural interface, Implantable medical device(IMD)**

I. INTRODUCTION

The implantable neural recording system is an essential building block for implementing neuroprosthetics. The recording system is widely applied to applications such as the prosthetic arm and the *in vitro* platform [1], [2]. Also, for sophisticate system operation of neuroprosthetics, the recording system can be used in conjunction with the electrical stimulation system such as the deep brain stimulator, cochlear implant, retinal prosthesis, etc. [3].

The neural recording system needs to satisfy key features for reliable neural activity monitoring *in vivo*. For monitoring weak neural signals and preventing tissue heating, the recording front-end integrated circuit (IC) needs to operate with low noise and low power performances. The area of the front-end IC needs to be reduced for minimizing the size of an implantable module. When implanting the recording module into the body, the space in which the module can be placed *in vivo* is considerably limited.

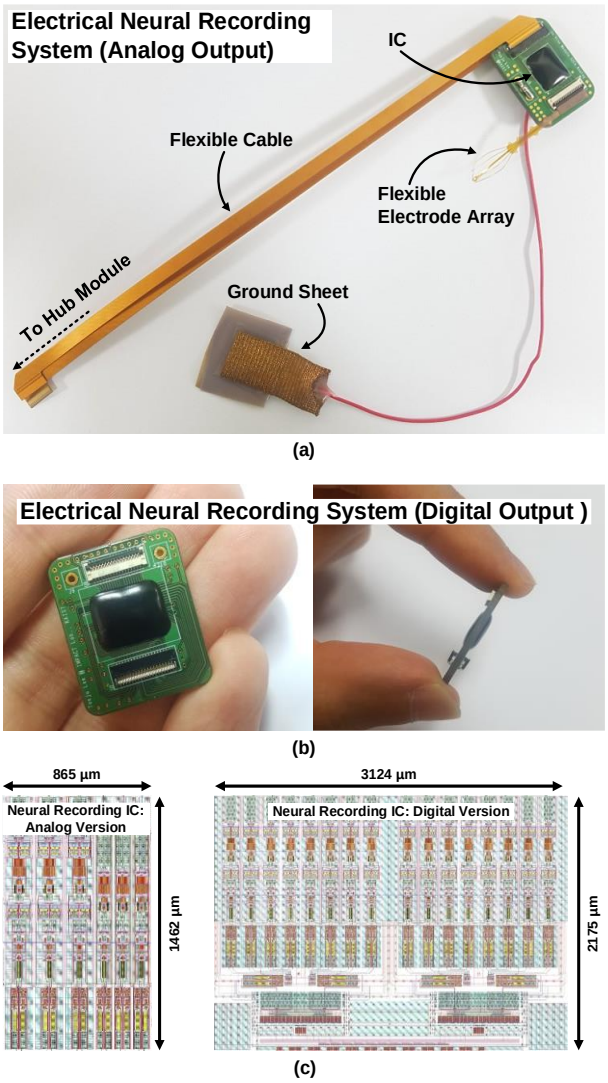

Fig. 1. Implantable electrical neural recording systems (a) without the ADC and (b) with the ADC, (c) layout of neural recording ICs used in the analog output version and the digital output version [4].

Therefore, in order to conduct stable implantation without the damage to surrounding tissues, the size of the recording module should be minimized as much as possible. Also, for ensuring the signal integrity of recorded neural signals, the electrode array and the recording module have to be properly shielded from electrical artifacts such as digital clock and power line interferences.

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This paper presents the electrical neural recording system with extended contents including system description and experiment results [4]. This paper is organized as follows. Section II describes two versions of implemented neural recording systems. Section III presents experiment results using the artificial neural spike generator and *in vivo* measurement results. Finally, Section IV concludes this work with the comparison of the prior neural recording systems.

II. SYSTEM ARCHITECTURE

Fig. 1 shows electrical neural recording systems for use in the brain and the peripheral nerve [4]. The Fig. 1(a) shows the analog version of the neural recording system which only amplifies neural signals without analog-to-digital conversion. The size of the printed circuit board (PCB) module is 25 mm by 17 mm. Fig. 1(b) shows the digital version of the recording system with 10-bit resolution for analog-to-digital conversion. The PCB module size of the digital version is 26 mm by 22 mm.

When the recording system is used for monitoring peripheral nerve signals, each recording system is composed of the flexible electrode array, the front-end PCB module, the flexible cable, and the ground sheet as shown in Fig. 1(a). The flexible electrode array is inserted into the target nerve. Then, the ground sheet surrounds the target nerve and the flexible electrode array for ensuing the signal integrity. After detecting neural signals through the flexible electrode array, processed neural data by the recording module is collected to the hub module through the flexible cable. When monitoring neural signals by using the digital version of the recording system, for ensuring the signal integrity of recorded neural signals, the weak analog signal lines on the flexible cable should be properly protected from the digital clock and power line interferences. The details of protection techniques are presented in [4].

The neural activity monitoring in the brain is similar to the recording of peripheral nerve signals, but the used electrode array can be different. When recording brain signals, rigid types of probes such as Utah array and Michigan array can be used [5], [6].

A. Neural Recording Front-End IC: Analog Version

Fig. 2 shows the block diagram of the neural recording front-end IC used for the analog version [4]. The IC is composed of six analog front-ends (AFEs). The weak neural signal is amplified through two stage amplifiers. The AFE is designed as the capacitively-coupled structure for filtering out the DC electrode offset.

The first stage amplifier has the 40 dB voltage gain and the second stage amplifier controls the voltage gain from 15 dB to 27 dB. When the AFE monitors wideband neural signals of action potentials (APs) and local field potentials (LFPs), the high-pass cutoff frequency is set to sub-1 Hz and the low-pass cutoff frequency is set to 10 kHz. Then, the high-pass cutoff frequency can be controlled from sub-1 Hz to 500 Hz for monitoring only neural spikes (or APs). The IC operates using two supply voltages. The AFE is driven by using the 1 V supply voltage and the 1.8 V supply voltage is used to operate the bias block.

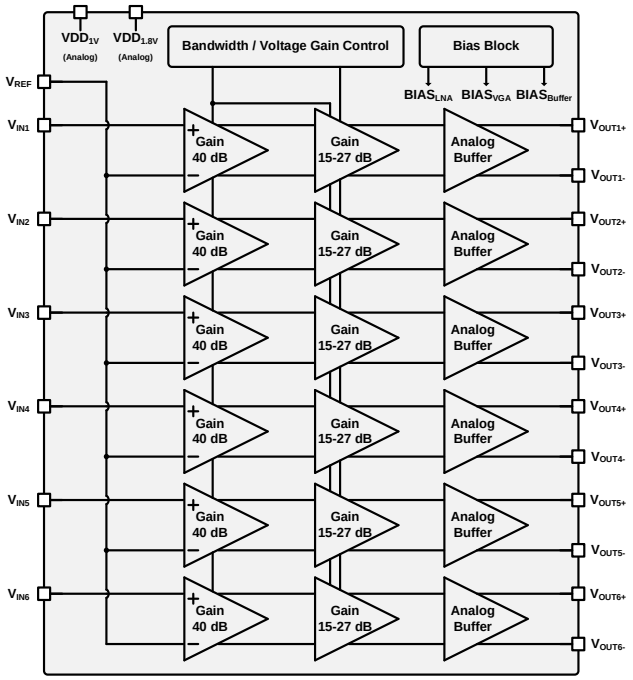

Fig. 2. Neural recording front-end IC without the ADC.

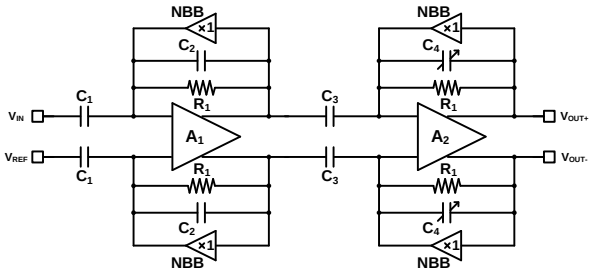

Fig. 3. Analog front-end using narrow-band buffers.

Fig. 3 shows the schematic of the AFE. For ensuring accurate and reliable control of the high-pass cutoff frequency, the double-high-pass-filter structure is employed by placing the narrow-band buffers (NBBs) to the feedback paths of each amplifiers [7].

When NBBs are deactivated, the AFE monitors wideband neural signals from sub-1 Hz to 10 kHz. The high-pass cutoff frequency having sub-1 Hz is formed by the pseudoresistor R_1 and feedback capacitors C_2 and C_4. When the NBBs are activated for filtering out low-frequency signals, the low-frequency band of the AFE is suppressed as much as the bandwidth of the NBB. The NBB is applied to the first and second amplification stages, thus the second-order high-pass characteristic is achieved and the high-pass cutoff frequency is reliably controlled without the influence of the pseudoresistor [7]. The pseudoresistor is only involved in achieving a sufficiently low high-pass cutoff frequency. The control of the high-pass cutoff frequency to a higher frequency is reliably set by NBBs.

The operational transconductance amplifiers (OTAs) of A_1 and A_2 are designed based on [8]. For improving the current-noise efficiency in the input stage of A_1, the PMOS and NMOS are used as the input stage [9]. Thus, the input transconductance g_m is doubled while maintaining the power consumption.

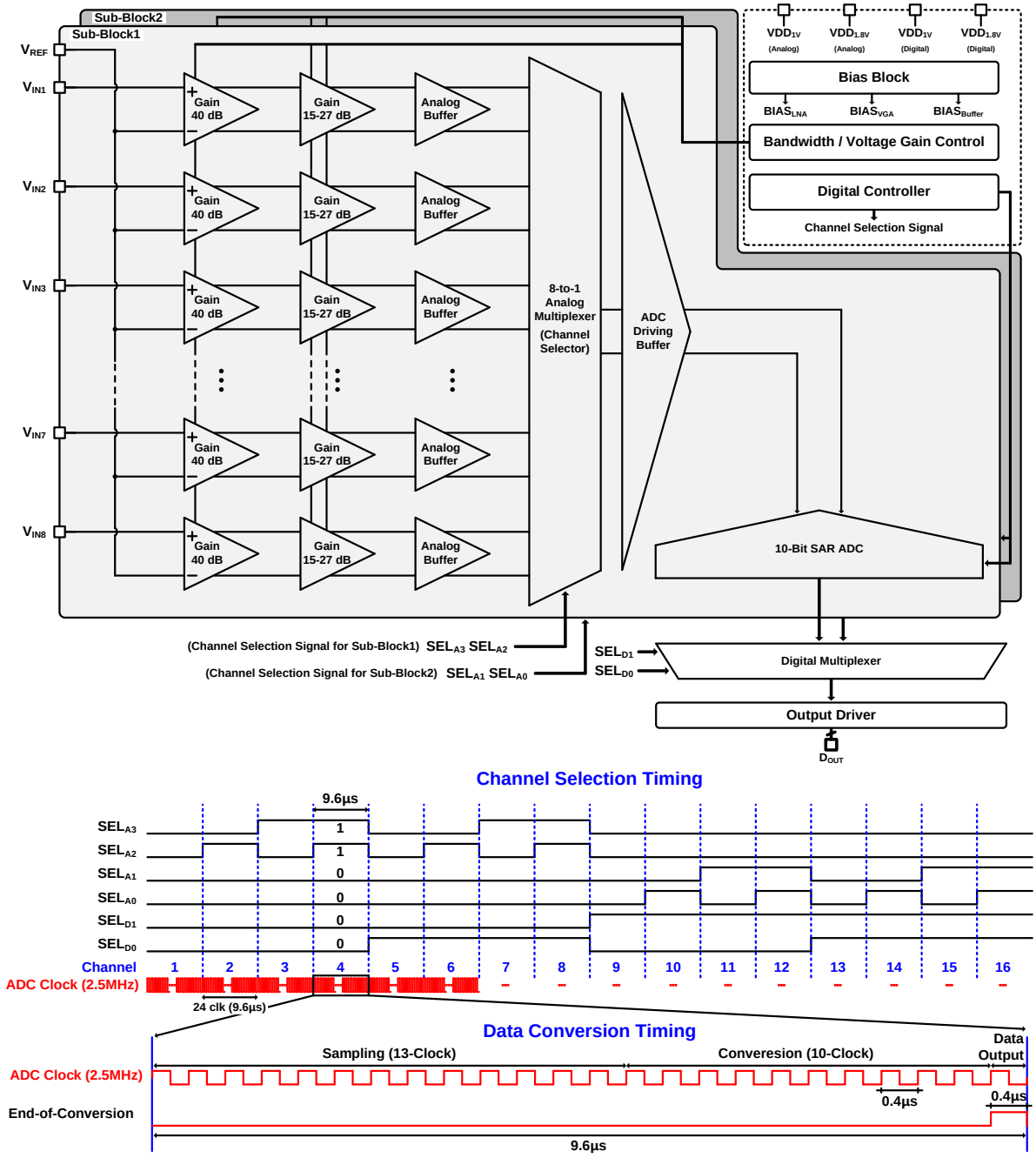

Fig. 4. Neural recording front-end IC with the ADC (top) and the timing diagram (bottom).

B. Neural Recording Front-End IC: Digital Version

Fig. 4(top) shows the block diagram of the 16-channel neural recording front-end IC including the analog-to-digital converter (ADC) [4]. The IC is composed of two sub-blocks. Each sub-block consists of eight AFEs, the channel selector, the ADC driving buffer, and the 10-bit successive-approximation-register (SAR) ADC. The AFE structure is the same as the analog version IC.

Channel selection signals of $SEL_{A0,1,2,3}$ and $SEL_{D0,1}$ control channel conversion sequence as shown in Fig. 4(bottom). The bias block generates bias voltages for the AFE. The bandwidth and the voltage gain are controlled like the analog version IC. The digital controller generates clock patterns for operating the 10-bit SAR ADC, as well as channel selection signals. The digital version IC operates using four supply voltages ($VDD_{1V,1.8V}$ for analog circuits and $VDD_{1V,1.8V}$ for digital circuits). The SAR ADC is designed by employing the dual sample-and-hold (S/H) technique [9], thus current consumption by the ADC driving buffer is relieved. Also, for energy-efficient ADC operation, the time-based comparator is employed [10].

Thanks to dual S/H operation, the sampling time is extended while maintaining the sampling frequency. After digitization of neural signals, the data is transferred to the hub module through the flexible cable as shown in Fig. 1(a). The output driver shown in Fig. 4 reliably transmits digital bits to the hub module using the 1.8 V supply voltage.

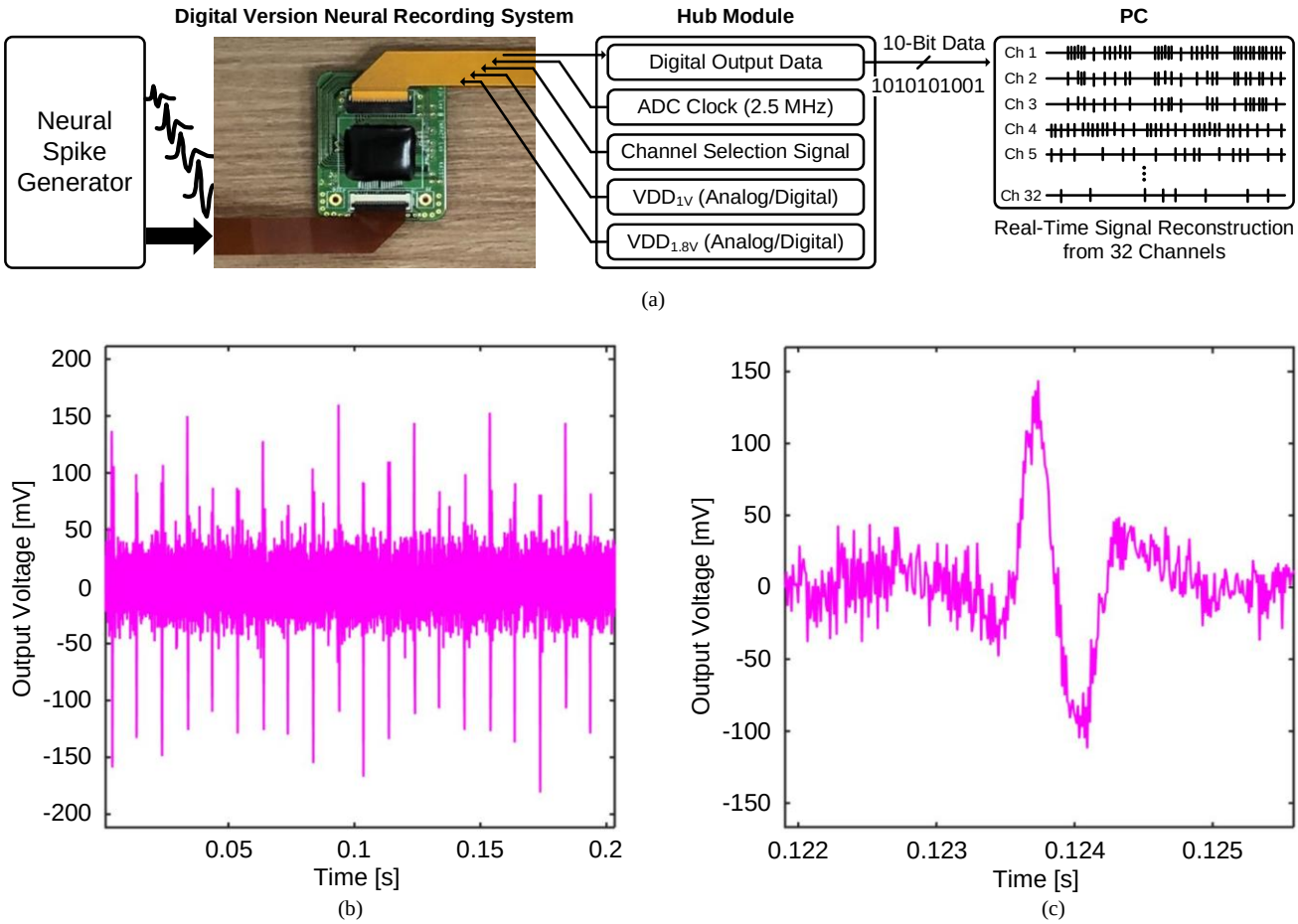

Fig. 5. (a) Benchtop test setup using the digital version neural recording system and the artificial neural spike generator (Blackrock Microsystems, signal simulator [11]), (b) measured neural spikes, and (c) the single-unit spiking (also known as action potential) when applying the artificial neural spike generator to the input of the digital version neural recording system.

III. MEASUREMENT RESULTS

A. Benchtop Test

Fig. 5 shows measurement results of the benchtop test using the digital version neural recording system presented in Fig. 1(b), the artificial neural spike generator (Blackrock Microsystems, signal simulator [11]), and the hub module. Before conducting *in vivo* experiments, the benchtop test is conducted using the artificial neural spike generator to verify the operation of the recording system and figure out electrical issues.

The artificial neural spike generator produces electrical neural signals having the frequency of about 1 kHz, and the amplitude of generated signals is from tens of μV to hundreds of μV [11]. The digitized neural data is collected to the hub module through the flexible cable as shown in Fig. 5(a). Figs. 5(b) and (c) present reconstructed neural spikes from the 32-channel digital version neural recording system when artificial neural spikes are applied to the input of the recording system.

The neural recording systems (analog and digital versions) are implemented by wire-bonding two ICs on the both sides of the PCB. Thus, the 32-channel digital version neural recording system is implemented using two 16-channel digital version ICs as shown in Figs. 1(b) and (c).

B. In Vivo Experiments

After completing the benchtop test using the artificial neural spike generator, *in vivo* experiments are conducted from the brain and the peripheral nerve using the rat as shown in Figs. 6 and 7. All the animal experimental procedures using a rat were approved by the Korea Institute of Science and Technology (KIST), and conducted in accordance with the ethical standards stated in the Animal Care and Use Guidelines of the KIST.

Fig. 6 shows measured neural signals using the rat. The electrode array is implanted into the thalamus of the brain using the anesthetized rat. Then, spontaneous neural spikes are successfully recorded as shown in Fig. 6(a). Figs. 6(b) and (c) show enlarged neural spikes.

Fig. 7(a) shows the *in vivo* experiment setup in the right sciatic nerve. Unlike spontaneous neural activity in the thalamus of the brain, the sciatic nerve does not produce spontaneous neural signals in the anesthetized state of the right hind leg is stimulated by brushing [4]. Then, neural spikes are recorded. Fig. 7(b) shows evoked neural spikes by brushing, as well as stimulation artifacts. In this *in vivo* experiments, neural spikes are evoked after approximately 100 ms according to the stimulation. The duration of the rat.

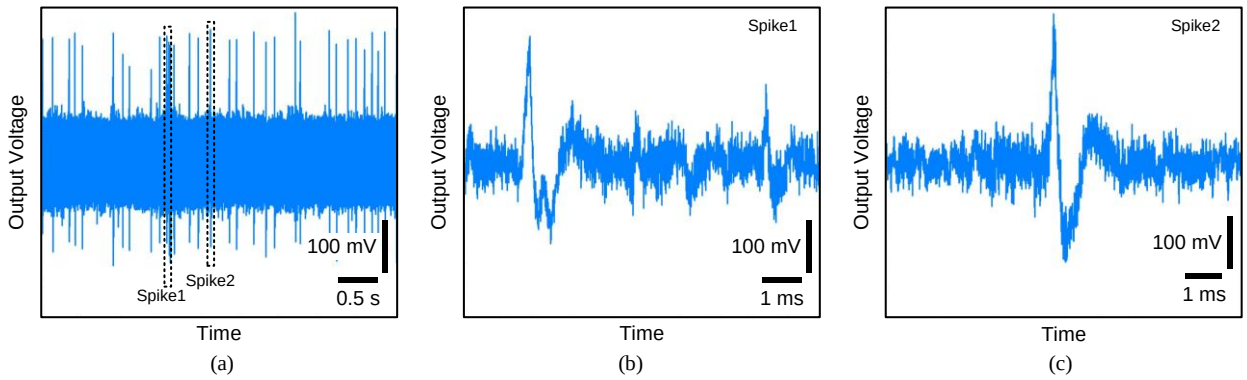

Fig. 6. (a) Measured neural signals from the rat brain, (b) enlarged neural spikes, and (c) the single-unit spiking (also known as action potential).

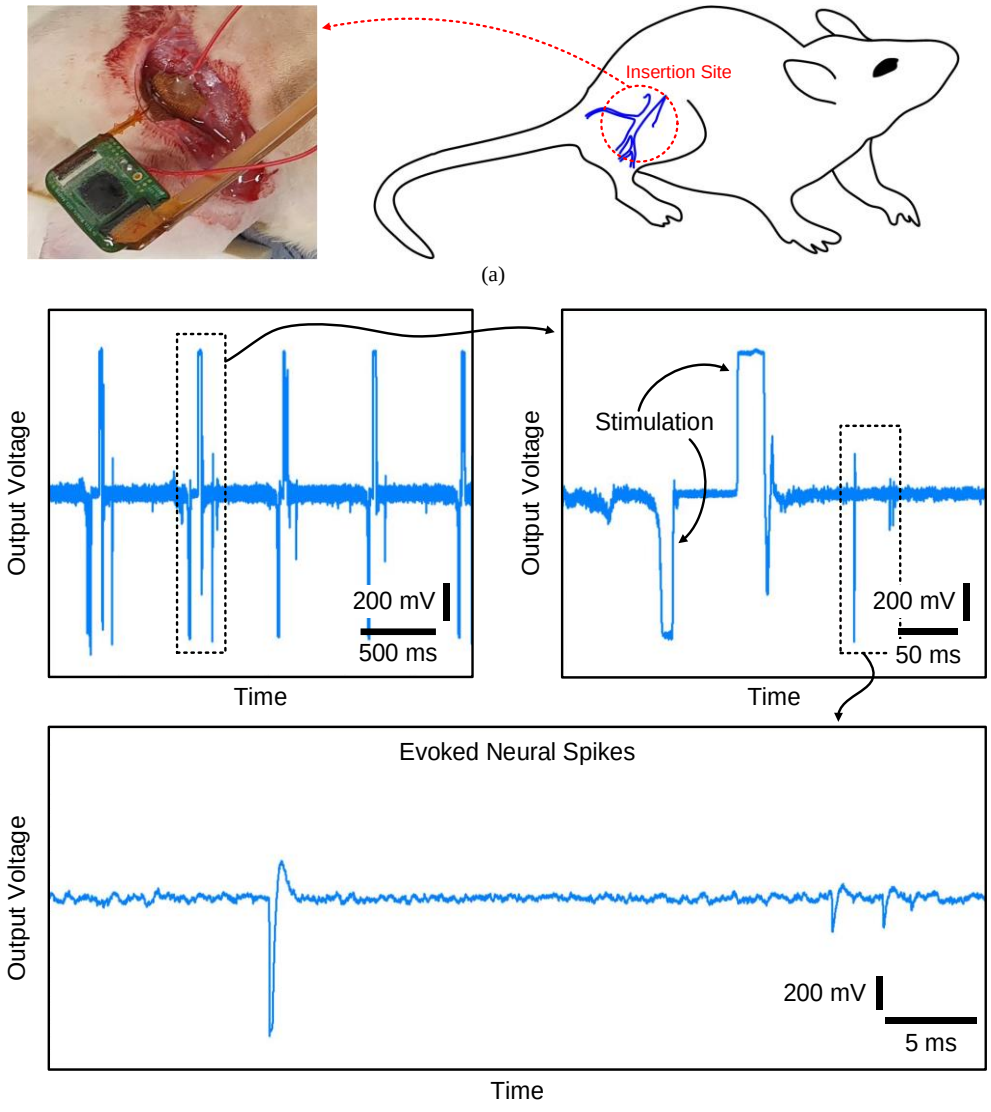

Fig. 7. (a) *In vivo* experiment setup for monitoring peripheral nerve signals in the right sciatic nerve [4], (b) measured stimulation artifacts due to brushing and evoked neural spikes.

Thus, for inducing neural signals in the sciatic nerve, the anodic and cathodic phases is about 25 ms, and the brushing of the right hind leg is manually conducted by every 500 ms.

When monitoring neural signals from the peripheral nerve, the flexible electrode array is inserted into the cross section of the sciatic nerve. Then, the ground sheet shown in Fig. 1(a) surrounds the electrode insertion site and the nerve to protect from external noise sources. The ground sheet is connected to the IC ground, and the all grounds used in the recording system are integrated into one.

TABLE I. PERFORMANCE SUMMARY COMPARED TO PRIOR WORKS

Design	This Work	RHD2000 Series (Intan Technologies)	MaxOne (MaxWell Biosystems)	Neuralink IC
Number of Channels	32	32	1024	1536, 3072
Channel Power	[a]3 μW	[b]250 μW	-	[b]5.2 μW
Input-Referred Noise	<4 μV_{rms}	2.4 μV_{rms}	2.4 μV_{rms}	5.9 μV_{rms}
A/D Resolution	10-bit	16-bit	10-bit	10-bit
Channel Sampling Rate	25 kS/s	30 kS/s	20 kS/s	19.3 kS/s
Voltage Gain	55 dB - 57 dB	45.7 dB	up to 78 dB	42.9 dB - 59.4 dB
Bandwidth	0.2 Hz - 10 kHz (Wideband Mode) 500 Hz - 10 kHz (High-Pass Mode)	0.1 Hz - 500 Hz (High-Pass Cutoff Freq.) 100 Hz - 20 kHz (Low-Pass Cutoff Freq.)	-	-

a: ADC power consumption is included; b: only analog amplifier is considered

IV. CONCLUSION

In this paper, we describe the two types of neural recording systems for use in the brain and the peripheral nerve, fabricated using a 1P6M 180-nm standard CMOS technology. The functionality of the recording modules is verified through the benchtop test using the artificial neural spike generator. Also, the implemented recording modules successfully conduct *in vivo* experiments from the brain and the peripheral nerve. The NBB applied to the AFE can reliably adjust the high-pass cutoff frequency while avoiding the influence of the pseudoresistor, thus the accurate recording bandwidth can be achieved according to the target signals. Table I provides the performance summary compared to the prior neural recording systems of RHD2000 Series [12], MaxOne [13], and Neuralink IC [14].

Although the channel performances such as power consumption, input-referred noise, and ADC resolution are comparable to the prior works, the neural recording module presented in this paper has a limited number of channels compared to the prior works. For fully understanding the whole brain consisting of tens of billions of neurons, the number of recording channels must be dramatically increased compared to the current number of channels within a limited silicon area.

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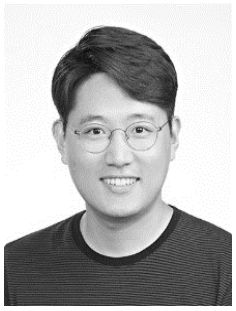

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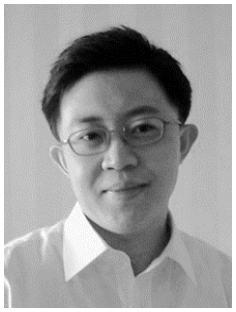
From 2014 to 2016, he was with the DGIST, where he was involved in developing neural recording ICs and brain rehabilitation systems. From 2017 to 2020, he was with the KAIST, where he developed multichannel electrical neural recording ICs and led the development of multimodal neural recording ICs monitoring APs/LFPs/Calcium ions for conducting the cell-type-specific study in complex neural networks. He also developed the implantable electrical neural recording module for use in peripheral nerves and was involved in various *in vivo* experiments using the customized neural probe and neural activity readout IC. He is currently a Postdoctoral Researcher at the IMPACT Lab, KAIST. His current research interests include neural interfaces focusing on the monitoring of multiple neural signals.



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He joined Samsung Electronics, Giheung, South Korea, as a Senior Engineer, in 2003, where he worked on multi-mode multi-band RF transceiver SoCs for GSM/GPRS/EDGE/WCDMA standards. From 2006 to 2013, he was with the Institute of Microelectronics (IME), Agency for Science, Technology and Research (A*STAR), Singapore. He worked as a Senior Research Engineer, from 2006 to 2007, a Member of Technical Staff, from 2008 to 2011, a Senior Scientist, in 2012, and a Deputy Director, in 2013. From 2011 to 2013, he led the Integrated Circuits and Systems Laboratory, IME, as a Department Head. In IME, he led various projects developing low-power 3D accelerometer ASICs for high-end medical motion sensing applications, readout ASICs for nanowire biosensor arrays detecting DNA/RNA and protein biomarkers for point-of-care diagnostics, ultra-low-power sensor node SoCs for continuous real-time wireless health monitoring, and wireless implantable sensor ASICs for medical devices, as well as low-power radio SoCs and MEMS interface/control SoCs for consumer electronics and industrial applications. He was also a Program Director of NeuroDevices Program under A*STAR Science and Engineering Research Council (SERC), from 2011 to 2013, and an Adjunct Assistant Professor with the Department of Electrical and Computer Engineering, National University of Singapore (NUS), from 2010 to 2013. From 2014 to 2015, he was an Associate Professor with the Department of Information and Communication Engineering, Daegu Gyeongbuk Institute of Science and Technology (DGIST), South Korea. Since 2016, he has been an Associate Professor with the School of Electrical Engineering, KAIST. He is the author of five book chapters and has more than 290 peer-reviewed international conference and journal publications in the areas of sensor interface IC, wireless IC, biomedical microsystem, 3D IC, device modeling and nanoelectronics. He also has more than 50 patents issued or filed. His main research interests include advanced IC platform development, including smart sensor interface ICs and ultra-low-power wireless communication ICs, as well as microsystem integration leveraging the advanced IC platform for emerging applications, such as intelligent miniature biomedical devices, ubiquitous wireless sensor nodes, and future mobile devices. He has served on the Technical Program Committee and Organizing Committee for various international conferences, symposiums, and workshops, including the IEEE International Solid-State Circuits Conference (ISSCC), the IEEE Asian Solid-State Circuits Conference (A-SSCC), and the IEEE Symposium on VLSI Circuits (SOVC). He is currently working as a Distinguished Lecturer of the IEEE Circuits and Systems Society.