A 2.4 GHz Fractional-N Sub-Sampling PLL with a Hybrid Type Phase-Interpolator

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***Abstract* - This paper presents a 2.4 GHz sub-sampling fractional-N PLL (SSPLL) with a hybrid type phase-interpolator (HPI). The usage of the HPI alleviates the demanding specification of digital-to-time converter (DTC). The proposed HPI structure is composed of a capacitive and tournament phase-interpolator (PI). This structure generates multi-phases with lower power consumption due to the capacitive PI part which do not consume the static power. On the other hand, the capacitive PI is affected by mismatches and parasitic when fine resolution is generated. In order to achieve accuracy with lower power consumption, MSB part is divided by capacitive PI and LSB part is divided by the tournament PI. The proposed SSPLL with the HPI is implemented by 65 nm CMOS process. It achieves 162 fs jitter, -247.3 dB figure-of-merit (FoM), and -47 dBc fractional spurs with a gain calibration circuit which is based on a least-mean-square (LMS) algorithm.**

Keywords - Digital-to-Time Converter(DTC), Fractional-N, Least-Mean Square(LMS), Phase-interpolator, Phase Locked Loop (PLL), Sub-sampling

I. INTRODUCTION

In recent years, the wireless applications have been increased. A low power transceiver architecture is shown in Fig. 1. In the receiver path a frequency synthesizer as a local oscillator (LO) is used in down conversion mixer. The received radio frequency (RF) signals are first amplified by a low noise amplifier (LNA) before down-converted to the intermediate frequency. The down conversion is operated in the mixer for both in-phase and quadrature signals. Then the signals are low-passed and amplified by the low-pass filter and programmable gain amplifier. Entirely, the signals after amplification is fed into an analog-to-digital converter (ADC) before they are processed by the digital baseband. For the transmitter, the direct up-conversion topology has the advantage of no need for mixing and low-pass filtering while its disadvantage is that the side lobes cannot be further suppressed, which are still tolerable. Above all, the frequency synthesizer is a key block in both the transmitter path and receiver path. The phase locked loop (PLL) is typically used

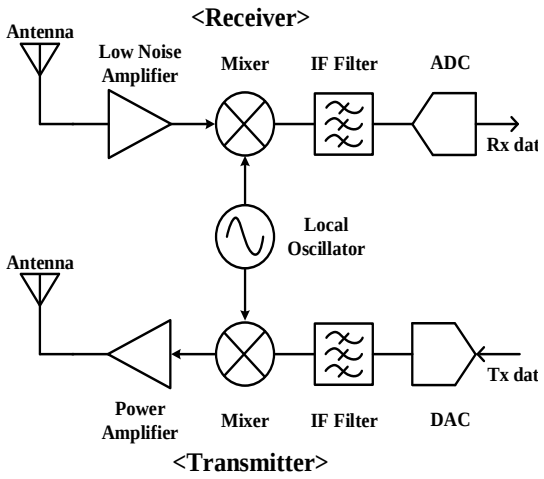

Fig. 1. Block diagram of the transceiver

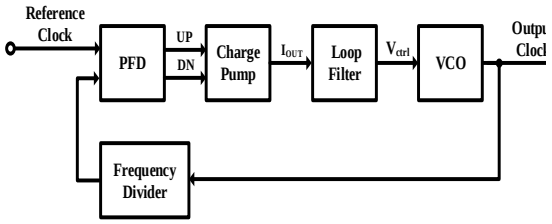

Fig. 2. Block diagram of the phase locked loop (PLL)

in the wireless communication system to generate the LO. The wireless communication industry is growing rapidly and the demands increase for smaller, less expensive, better performing and less power consuming circuits. The most common PLL used in today wireless communication systems is the fractional-N PLL.

The block diagram of the conventional PLL is implemented by the charge pump PLL architecture is shown in Fig. 2. The conventional PLL is consist of a phase frequency detector (PFD), charge pump (CP), loop filter (LF), voltage-controlled oscillator (VCO), and frequency divider (FD). The PFD compares the phase and frequency of the divided clock and reference clock. The CP converts the phase information which was generated from the PFD to analog control

$$f_{out}=f_{Ref}\times N \quad (1)$$

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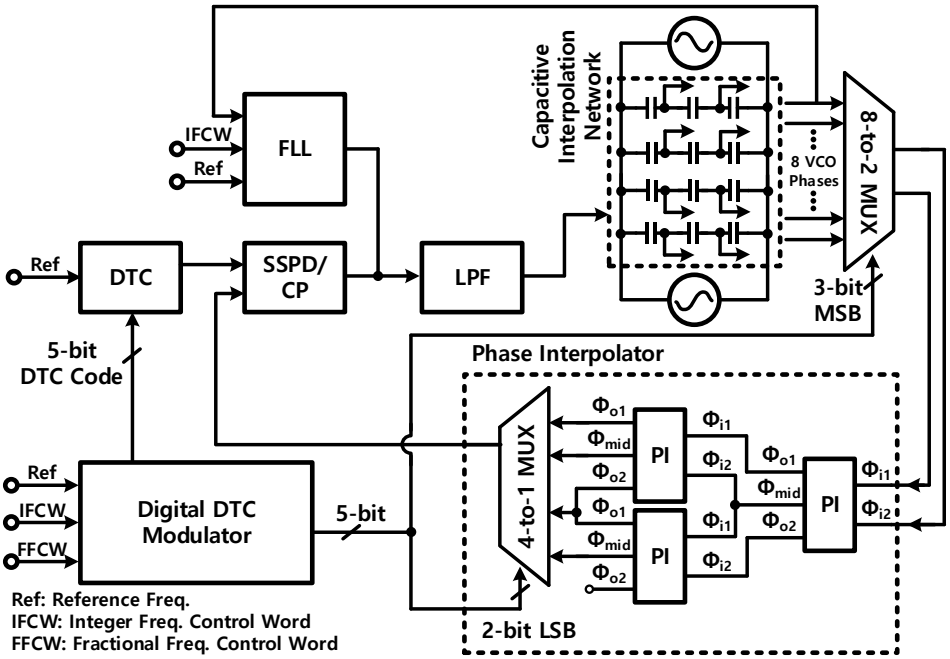


Fig. 3. Block diagram of the proposed fractional-N SSPLL

voltage for the VCO. The applied analog control voltage determines the output frequency of the PLL. The output frequency of the PLL is determined by the reference clock frequency and division ratio N as follow (1).

The conventional PLL has been widely used in the transceivers. But the conventional PLL has drawbacks of the in-band phase noise. Due to the existence of the divide-by-N in the feedback path, the PFD/CP and divider noise (in power) is multiplied by N^2 when it is transferred to the conventional PLL output. So, the in-band phase noise of the conventional PLL is limited by the divide-by-N. Thus, it is difficult to design the low jitter PLL. To overcome this challenge, a fractional- N sub sampling PLL (SSPLL) based on a hybrid phase interpolator (PI) and digital-to-time converter (DTC) is proposed. In the proposed architecture, by employing a hybrid PI, the requirements imposed of DTC can be reduced compared with conventional factional-N PLL. Thus, the low intrinsic jitter and low power consumption fractional -N operation can be obtained. Unlike the conventional PLL, the charge pump PLL architecture, a sub-sampling PLL architecture can work without using a divider. Thus, the divider noise and power dissipation can be eliminated. In additional, the PD/CP of the sub-sampling PLL noise is not multiplied by N^2 in contrast to the conventional PLL. As a result, the in-band phase noise is greatly improved which lead to the PLL design with very low jitter as well as low power [1].

This paper is organized as follows. Section II introduces the proposed SSPLL and circuit implementation. Section III describes the simulation results of the SSPLL using Spectre. Finally, the conclusion is given in Section IV.

II. PROPOSED SSPLL AND CIRCUIT IMPLEMENTATION

A fractional-N sub-sampling PLL (SSPLL) includes a DTC, SSPD/CP, LPF, hybrid phase-interpolator (HPI), digital DTC modulator, and frequency locking loop (FLL) as shown in Fig. 3. A sub-sampling loop (SSL) contains the DTC, SSPD/CP, and VCO. The HPI includes the capacitive PI and active PI. Because of the HPI, this structure can enhance the linearity of the DTC.

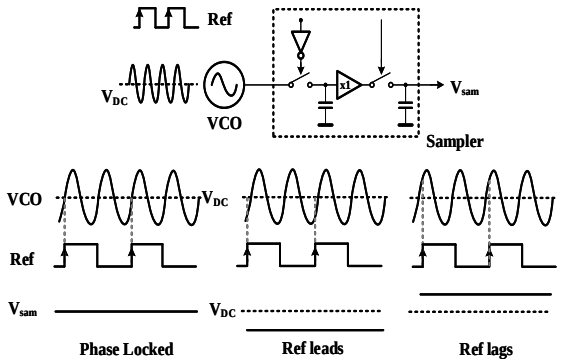


Fig. 4. Sampling based PD conceptual diagram and its timing diagram

A. Sub-sampling phase detector (SSPD) and charge pump (CP)

Fig. 4 shows a conceptual diagram and timing diagram of the sampling-based PD [1]. The VCO output, a sine wave with amplitude AVCO and DC voltage V_{DC}, is sampled by a reference clock Ref. When the phases of the VCO and Ref are aligned and their frequency ratio N is an integer, the sampled voltage V_{sam} has a constant value equal to V_{DC}. When there is phase error between the VCO and Ref, V_{sam} will be deviated from V_{DC}. As a result, the SSPD works like the PFD of the conventional PLL.

The SSPD noise is can be calculated as

$$L_{\text{in-band,SSPD}} = \frac{kT}{C_{sam} \times A_{VCO}^2 \times f_{Ref}} \text{[dBc/Hz]} \qquad (2)$$

where k is the Boltzmann constant, T is the absolute temperature, C_{sam} is the sampling capacitor value, A_{VCO} is the swing of the VCO, and f_{Ref} is the frequency of the Ref. In (2), the SSPD noise is certainly not multiplied by N^2. Because of that, the overall noise can be improved. For example, the above parameters assume the values f_{Ref} = 40 MHz, A_{VCO} = 0.4 V, and C_{sam} = 10 fF. It brings $L_{in\text{-}band,SSPD}$ to be -131.9 dBc/Hz. The Fig. 5 is the block diagram of the SSPD/CP implemented by the differential type [1]. The differential type has many advantages. First, we can alleviate charge injection and charge sharing issues and help to reject supply noise. Second, the additional reference voltage V_{DC} is not needed. The pulser generates a pulse width to reduce the SSPD/CP gain. Because of integrating the capacitor area of the LF. The CP in Fig. 5 is similar to the conventional CP. However, a key difference is that the current source amplitude of this CP is controlled by the SSPD while the current source switch-on time of the conventional CP is controlled by the PFD. So, this CP has a robustness of the current matching compared with the conventional CP.

B. Digital-to-time converter (DTC)

The integer-N SSPLL has recently re-introduced in [1-2]. To enable the fractional mode in SSPLL, it needs the DTC. The DTC is used to control the exact instant of sampling, such that it always rises or fall on the expected zero crossing of the VCO, even for non-integer ratios between the VCO frequency and the reference clock. Fig. 6 shows the DTC architecture. It is implemented by delay cell and capacitors. The exact instant of sampling is controlled by the delay code which is from a DTC modulator. The delay code sets the time constant of the DTC modulating the number of the capacitors. The DTC can cover over a single VCO period. There are some key issues using the real DTC for implementing the fractional mode. The first limit is the DTC resolution. So, the DTC limits the performance of in-band noise. It is calculated as

$$L_{in\text{-}band,DTC}=10.\log_{10}\left[\left(\frac{2\pi\times LSB}{\sqrt{12}\times T_{VCO}}\right)^2\times\frac{1}{f_{Ref}}\right][dBc/Hz] \quad (3)$$

where LSB is the resolution of the DTC, and TVCO is the period of the VCO. In (3), the DTC's resolution affects the performance of the in-band noise. By using the fine resolution of DTC, we can ignore the effect of DTC's noise. For example, the above parameters assume the values f_{Ref} = 40 MHz, T_{VCO} = 416 ps (or f_{VCO} = 2.4 GHz), and LSB = 5 ps. It brings $L_{in\text{-}band,DTC}$ to be -162.6 dBc/Hz. That performance is similar to a crystal oscillator which is the Ref. As a result, we can ignore the in-band noise of DTC when we use the fine resolution of the DTC. The second key issue is the linearity of the DTC. The INL performance in the DTC leads to the spurious tone of SSPLL output. So, this SSPLL includes an additional calibrator which improves the linearity of the DTC to suppress spurious tones.

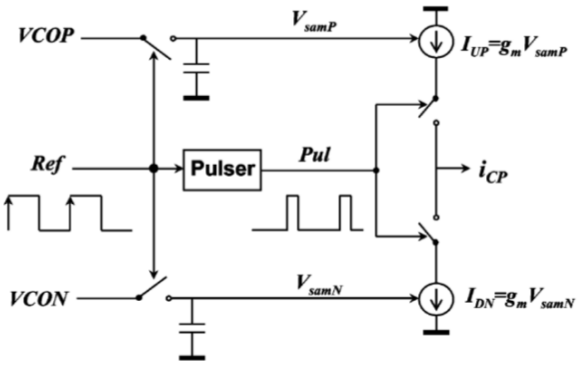


Fig. 5. Block diagram of the SSPD/CP

C. Digital DTC modulator

The fractional-N SSPLL needs the DTC which is controlled by the digital DTC modulator [4]. As shown in Fig. 7, the digital computation of the necessary phase adjustment which means the fractional division ratio is calculated by the first sigma-delta modulator (SDM) and phase accumulator. To scale the output of the accumulated phase error to a digital tuning code, it needs to multiply the output of the accumulator in Fig. 7 by a factor $T_{Ref}/(LSB_{DTC}.N_{frac})$. And then the gain correction factor is multiplied by the digital tuning code for calibrating the linearity of the DTC using a sign-sign least-mean-square (LMS) algorithm. The LMS algorithm is verified by MATLAB and implemented by logic gates to improve spurious tones [5]. Finally, the second SDM is to shape the quantization noise beyond the bandwidth of the SSPLL. Owing to the fact that the stream of the SDM is quite accurate on average, the average frequency of the SSPLL is also accurate, with no visible modulation. The generated code, e.g. the DTC code, from the DTC modulator is applied to the DTC for the implementation to the fractional-N SSPLL. The SDMs are implemented by a MASH type which provides better randomization of the generated code and helps to reduce spurious tones than a single type.

D. Frequency locking loop

The SSL in the SSPLL has a narrow detection range of the PD due to sinusoidal characteristics. Moreover, SSL cannot distinguish between $N.f_{Ref}$ and other harmonics of f_{Ref} and thus the SSPLL may false to lock and unwanted division ratio [1]. Therefore, SSPLL needs the FLL to guarantee to correct lock to wanted division ratio. Fig. 8 shows the block diagram of the FLL [1]. The FLL includes the tri-state PFD with a dead-zone (DZ), the conventional CP, and fractional divider which involves the SDM. The tri-state PFD with the DZ is shown in Fig. 9(a). The PFD with the DZ has the conventional tri-state PFD and two D-type flip flops which re-sample the generated UP and DN pulses. The two added D-

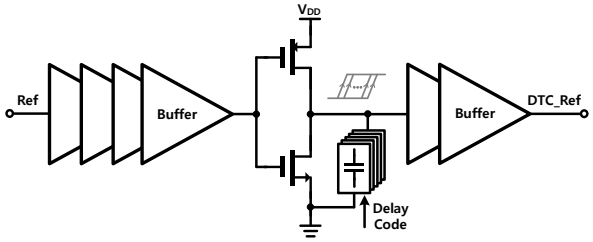


Fig. 6. DTC architecture

type flip flops are trigged by the falling edges, which are $T_{Ref}/2$ delayed from the rising edges if the clock duty cycle is 50%. In this way, any UP and DN pulses with width smaller than $T_{Ref}/2$ will be "filtered" out, creating a timing DZ of $\pm T_{Ref}/2$. Fig. 9(b) shows an example timing diagram when Ref lags. The FLL action is as follows. The overall action of the FLL without the DZ is the same as the conventional fractional-N PLL which is implemented by the charge pump type. When f_{VCO} is even far from $N \bullet f_{Ref}$, the phase/frequency error between VCO and Ref is large and activates the FLL. The FLL has a larger gain than the SSL, controls and brings down $|f_{VCO} - N \bullet f_{Ref}|$. When it is close to locking state, the phase/frequency error between VCO and Ref is small and activates SSL. The FLL has no influence on the SSL and do not degenerate the PLL output noise performance. In order to realize the aforementioned functions, the bias current for the CP of the FLL should be large enough. So, the FLL dominates the loop control outside the DZ. After locking is completed, the FLL is disable to save power and does not affect the SSPLL output noise performance.

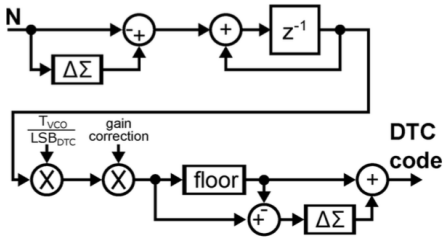


Fig. 7. Digital DTC modulator including quantization, gain correction, and quantization noise shaping

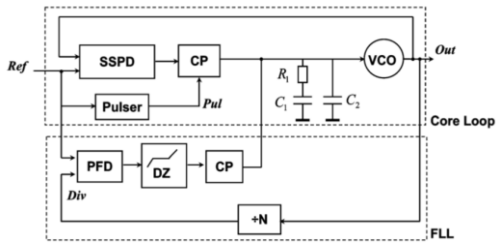


Fig. 8. Block diagram of the FLL

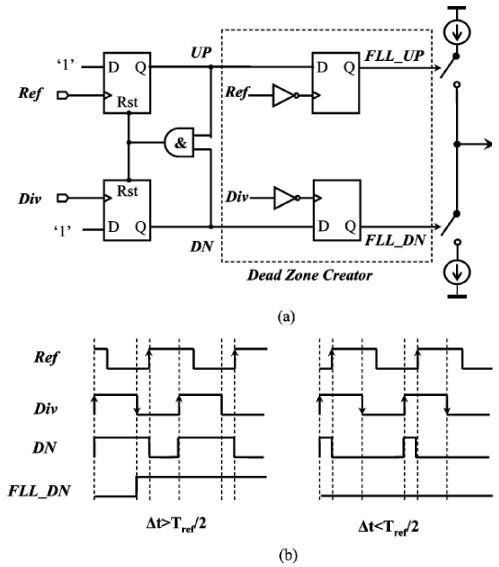


Fig. 9. Tri-state PFD/CP with the dead zone (a) schematic, (b) example timing diagram when Ref lags

E. Quadrature voltage-controlled oscillator (QVCO)

A quadrature voltage-controlled oscillator generates a quadrature signal using a capacitor-coupling technique. This architecture contains two standard LC-voltage controlled oscillators (LC-VCOs) and coupling capacitors as shown in Fig. 10. This capacitor-coupled QVCO (CC-QVCO) biased with sinusoidal current. The CC-QVCO adopts two novel technique: 1) using capacitor to couple two LC-tank cores for quadrature generation and 2) employing sinusoidal currents through these coupling capacitors to bias the oscillator [6]. The CC-QVCO removes the undesirable effects caused by the coupling transistors in the parallel-QVCO (P-QVCO), increases the oscillation amplitude, and reduces phase noise contributed by cross-coupled transistors. Compared to the P-QVCO, the CC-QVCO can achieve a theoretical 3 dB phase noise improvement, as verified by simulations [6].

F. Capacitive phase-interpolator (PI)

The multi-phase clock signal is need to implement the fractional mode PLL using the sub-sampling technique. Fig. 11 shows the circuit schematic of a capacitive phase-interpolator (PI) [7]. It generates half-quadrature output signals from quadrature excitations (I+, I-, Q+, and Q-). This technique generates multi-phase using a capacitance ratio between C_1 and C_2. According to [9], the capacitance ratio capacitance ratio between C_1 and C_2 is specified by

$$C_1 \cong 1.4 \times C_2 \quad (4)$$

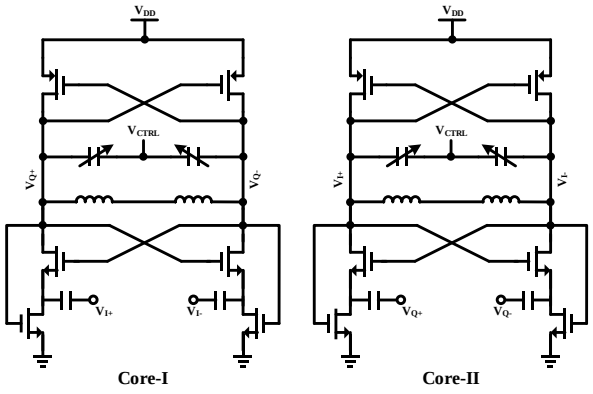


Fig. 10. Schematic of the QVCO using the capacitor-coupling technique

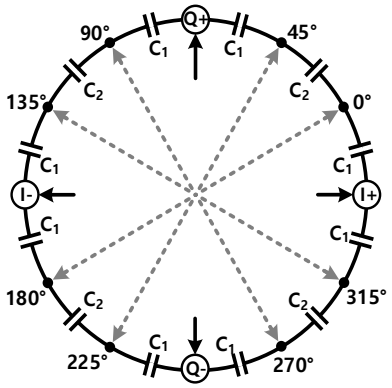


Fig. 11. Schematic of the capacitive PI

This structure is important the capacitance ratio than the absolute values of the capacitances. Considering the excellent matching property of the on-chip components, accurate half-quadrature output phases can be generated by the capacitive PI even in the presence of process and temperature variations [7]. The generated multiple output phases from the capacitive PI can be selected by a multiplexer to choose the wanted phases.

IV. SIMULATION RESULTS

The total area is 1.08 mm^2 with pads. The top layout includes the SSL, FLL, LF, QVCO, PI, and digital which means the digital DTC modulator as shown in Fig. 12. The proposed fractional-N SSPLL is implemented in a 65nm CMOS process. A 1.0 V supply powers the chip. The SSPLL is able to tune from 2.2 to 2.6 GHz. The phase domain simulation is performed by Spectre simulator, and then the time domain simulation is also performed by CPPSIM simulator using the result of Spectre. The simulation result of CPPSIM is shown in Fig. 13. The phase noise at 1 MHz offset of the proposed SSPLL is -118 dBc/Hz in the fractional mode. The loop bandwidth is set to around 1.4 MHz where the in-band noise floor intersects the VCO phase noise for minimal SSPLL total noise. The simulated rms jitter in fractional mode is 162 fs in the integration range of 10 kHz to 20 MHz with a power consumption of 7 mW. The figure of merit (FoM) is calculated as -247.3 dB. The SSPLL output spectrum is shown in Fig. 14. Before the LMS calibration in Fig. 14(a), the reference spur is -50 dBc and the fractional spur is -39 dBc. After the LMS calibration in Fig. 14(b), the reference and fractional spur are greatly reduced. As a result, the reference spur has reduced by 23 dB to -73 dBc and the closest fractional spur has reduced by 8 dB to -47 dBc. The performance of the proposed fraction-N SSPLL is compared against other works and a more detailed comparisons is given in Table II.

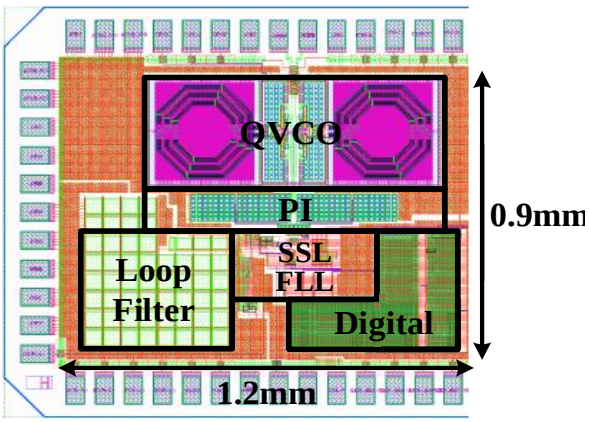


Fig. 12. Top layout of the proposed fractional-N SSPLL

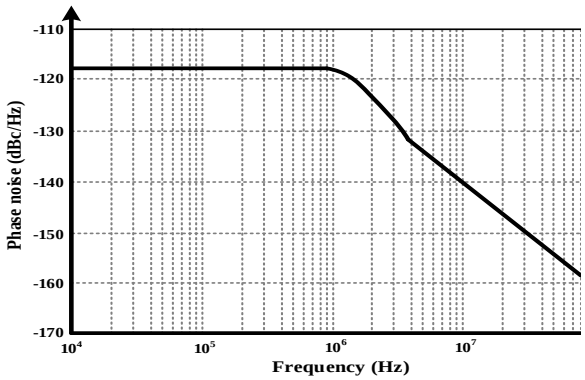
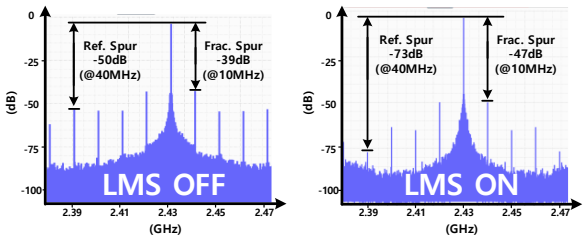


Fig. 13. Simulated PLL output phase noise using CPPSIM

V. CONCLUSION

A fractional-N sub-sampling PLL (SSPLL) based on a hybrid phase-interpolator (PI) and digital-to-time converter (DTC) is reported. The proposed architecture reduces tight requirements imposed on the DTC used in the conventional fractional-N PLL by employing a hybrid PI. The hybrid PI includes the capacitive and active PI. It has lower power consumption than pipelined PI because of reducing the number of unit PIs. Also, it has lower sensitivity to parasitic components and mismatches than the capacitive PI. This enables efficient architecture of the multi-phase generators required for the fractional-N operation with low intrinsic jitter and low power consumption. The proposed fractional-N SSPLL is implemented in 65nm CMOS process and achieves an integrated jitter of 162 fs and the FoM of -247.3 dB at 2.43



(a) (b)

Fig. 14. Reference and fractional spur (a) before LMS calibration, (b) after LMS calibration

TABLE I. Performance summary of fractional-N PLLs

Parameters	Performance
Technology(nm)	180
Ref. (MHz)	40
Output frequency (GHz)	2.2~2.6
In-band PN (dBc/Hz)	-120
Integrated rms Jitter (fs)	162*
Ref. Spur (dBc)	-73
Power(mW)	7
No. of out. Phases	32
FoM(dB)	-247.3

$$\text{FoM}=20\log\left(\frac{\sigma_t}{1s}\right)+10\log\left(\frac{P}{1mW}\right),$$

* measured in fractional mode

GHz in fractional mode with a power consumption of 7 mW. This SSPLL design achieves a reference spur and fractional spur of -73 and -47 dBc with an LMS calibration, respectively. The proposed hybrid PI can be employed to not only the fractional-N SSPLL, but also other applications which need accurate multi-phases.

ACKNOWLEDGMENT

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