A 32-Channel Low-Power Neural Recording System for Continuous ECoG Signal Monitoring and Detection

Jung Woo Jang[1], Yu Ri Kim, Chae Eun Lee and Yoon-Kyu Song[a]
Department of Nano Science and Technology, Graduate School of Convergence Science and Technology,
Seoul National University
E-mail: [1]jungwoojang@snu.ac.kr,

***Abstract* - In this study, a 32-channel low-power neural recording system was developed to analyze neural activity. Neural activity recording systems play an important role in neurosciences as well as the development of neuroprosthetic devices to treat neurological diseases and assist in recovery from disabilities. For example, monitoring neural signals allows prediction of the behaviors of paralyzed patients or explanation for the causality between behavior and neural activity. A conventional recording system with an integrated circuit has several limitations in terms of noise and power consumption. Herein, we propose a 32-channel low-power fully implantable neural signal recording system; a low-noise amplifier, a lowpass filter, an analog multiplexer, and a shift register were designed for the system. The experimental results highlight the low noise and adequate frequency response of the system. Further, in the experiments, ECG signals with magnitudes of up to 100 µV could be detected clearly. For the 32-channel neural recording system, a low supply voltage of only 1.2 V is needed, and the total power consumption is 60 µW, with a total gain of 58 dB and input referred noise of 3 µVrms. The bandwidth of the system is 2–300 Hz for measuring target ECoG signals. The system was designed with a standard 0.18 µm CMOS technology to measure neural signals while maintaining very low power consumption.**

***Keywords*—Brain–Machine Interface, Low-Noise Amplifier, Implantable Recording System**

I. INTRODUCTION

Brain−machine interface (BMI) refers to the technology where an external system and the human nervous system can communicate bidirectionally to help rehabilitate patients with impaired brain functions [1]. BMI can also be used for diagnosing mental illnesses, rehabilitating the elderly or disabled, and life-support systems. Moreover, it includes functions that can partially replace or supplement the activities of persons with impairments [1-4] .

Recording neuronal activity is essential in BMI research and includes an invasive method to implant electrodes on the surface of the brain; for example, electrocorticography (ECoG), intracranial electroencephalography (iEEG), local field potential (LFP) or non-invasive methods such as electroencephalography (EEG) require such implants to record brain activity [5]. As shown in Fig. 1, ECoG uses electrodes to record neural activity from the surface of the cerebral cortex.

Practically speaking, the development of invasive BMI is required to enable paralyzed patients to control external devices or to compensate for the damaged vision of visually impaired people. The invasive recording method is a technique that utilizes a surgically implanted microelectrode array in the gray matter to measure signals with high signal-to-noise ratio and spatial resolution. However, the surgical insertion of the microelectrode array poses risks that can induce neurological damage and infection due to the electrode and electronic devices.

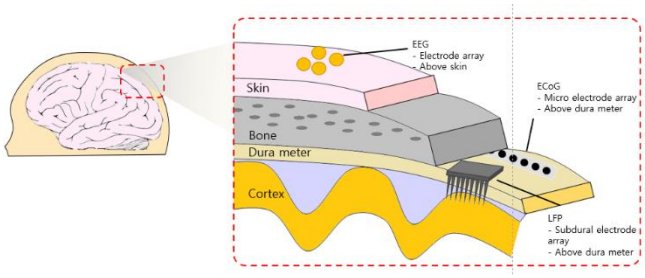


Fig. 1. Different types of brain signal measurements

Conventional recording systems have several limitations owing to their excess noise levels and high-power consumption. Over the past few decades, the need for developing appropriate approaches to design BMI circuit systems has gradually increased. For clinical or pre-clinical applications, ultralow power consumption is desired. As the integrated chips are located very close to the cells in pre-clinical or clinical studies, the power consumption should be reduced to prevent cellular damage. Currently, power scheduling methods are commonly used, which supply power only when necessary through a switching network. An alternative method is to integrate an analog-to-digital converter (ADC) in each channel, which can increase sampling time and reduce power but increase the chip size.

In Section II, the schematic design and block diagram are explained. In Section III, the experimental data and analysis results are discussed. Finally, the summary and conclusion are presented in Section IV.

a. Corresponding author; yksong@snu.ac.kr

Manuscript Received Feb. 15, 2021, Revised Mar. 29, 2021, Accepted Mar. 30, 2021

This is an Open Access article distributed under the terms of the Creative Commons Attribution Non-Commercial License (http://creativecommons.org/licenses/bync/3.0) which permits unrestricted non-commercial use, distribution, and reproduction in any medium, provided the original work is properly cited.

II. DESIGN METHODOLOGY

The low-noise amplifier (LNA) is the main block of the design consisting of a front end that amplifies the brain signals and filters undesired signals. The electrocorticography ranges from 0.1–300 Hz and must be detected clearly. However, in the proposed scheme, the amplifier was designed to have a bandwidth of 2–300 Hz to remove low-frequency noise. As the noise level of the neural recording system is determined by the LNA, it is the most important block in the entire system (Fig. 2). The designed 32-channel low-power neural recording system comprises a neural amplifier, an analog multiplexer (MUX), a shift register, and an additional amplifier system. The complete system has a size of 5mm×1mm.

In early research, the lower cutoff frequency was determined by a reverse-biased diode or a transistor operating in the subthreshold region. However, a pseudoresistor is highly influenced by not only the process parameters but also the nonlinear characteristics according to the drain–source voltage. We designed a pseudoresistor using a PMOS transistor in which a constant voltage was applied to the gate to always maintain a constant resistance value. Fig. 3 shows the capacitive feedback structure widely used in neural signal measurement circuits [6]; the advantage of this structure is that it can remove noise in the low-frequency band, such as flicker noise, by the pole generated by the pseudoresistor and the feedback capacitor. In addition, it has the advantage of being able to cutoff the offset voltage by the large input capacitor.

Existing lowpass filters (LPFs) using resistor and capacitor components need large resistors and capacitors, which renders the filter inefficient in terms of chip space. In the proposed system, an active LPF is designed to determine the cutoff frequency using an operational transconductance amplifier (OTA). To design a small transconductance value, there is a limit to simply increasing the length of the input MOSFET. However, we were able to lower the output transconductance to the nano siemens level by placing the MOSFET in series and parallel. The active LPF consisting of the OTA and capacitor comprises the schematic of the proposed LNA.

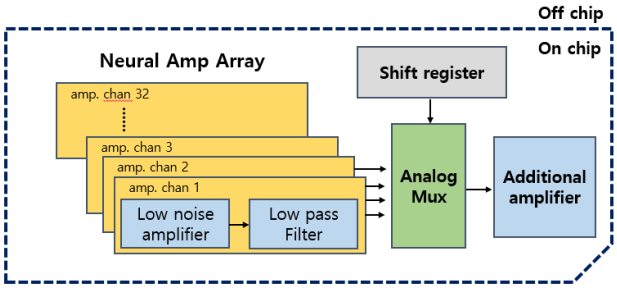


Fig. 2. Block diagram of the 32-channel low-power neural recording system.

A. Neural Signal Detection Module

Each neural signal detection module in the proposed design includes an LNA, an LPF, a buffer, and an analog switch [7]. In a previous former work, we used current-reuse input pairs to reduce the input referred noise and a telescopic arrangement to achieve higher gain [8]; this topology is suitable for driving capacitive loads and minimizing noise as each transistor is designed to operate in the weak, moderate, or strong inversion region. A common-mode feedback circuit is designed to stabilize the output common-mode voltage via adjustment of the common-mode output currents. However, after Monte Carlo simulations, we found some problems where the output DC voltage was observed near the ground or VDD rather than at half VDD as originally designed. This is because most of the current-reuse architecture consists of an inverter structure that receives the input voltage from an NMOS and a PMOS at the same time. In the inverter structure, since the output changes rapidly to VDD or GND according to the voltage level of the input terminal, an auxiliary circuit is essential to maintain a constant output common-mode voltage. On the other hand, the general-type fully differential amplifier renders the output common-mode voltage regulation relatively simple. Therefore, to stabilize the output DC voltage, we selected a cascode structure, as shown in Fig. 4.

In order to minimize the noise of front amplifier, we designed the width of the transistor at the input stage to be 200um. In addition, the input stage was operated in the strong weak inversion region, and M1 and M2, which provide bias current, were operated in the saturation region, and the biasing transistor were designed to operate in moderate inversion region. The common mode feedback circuit (CMFB), which regulates the output voltage, consumes 1/5 of the total power of the main amplifier. Pseudo-resistor was used for calculating the common mode of the output stage. The input capacitance of the designed low noise amplifier is 4pF and the layout size is 100um×300um.

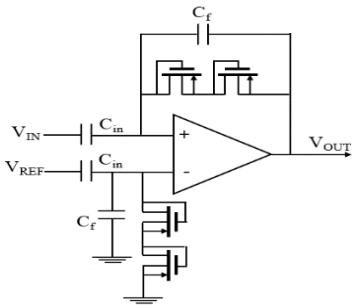


Fig. 3. Schematic of capacitive-feedback neural amplifier

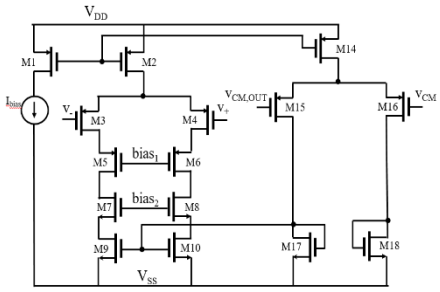


Fig. 4. Schematic of low-noise amplifier

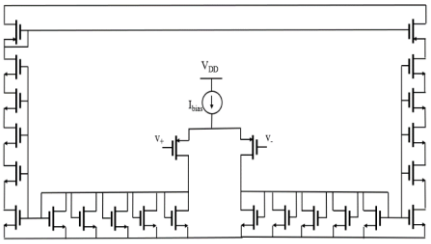


Fig. 5. Schematic of OTA for lowpass filter

B. Analog MUX and Shift Register

In this study, the target neural signal is the ECoG, whose frequency range is below 300 Hz. Since the target signal range is in a very low frequency band, a sequential multiplexing method is used. We designed the analog multiplexer by sequentially applying the enable signal to the analog switch, the final output terminal of the neural signal detection module, and through the 32-bit shift register. The shift register was directly synthesized using the Synopsys digital circuit design tool and simulated in Cadence AMS, which can help simulate analog–digital mixed designs. The designed shift register had a size of 120 µm × 80 µm and consumed 20 µW of power.

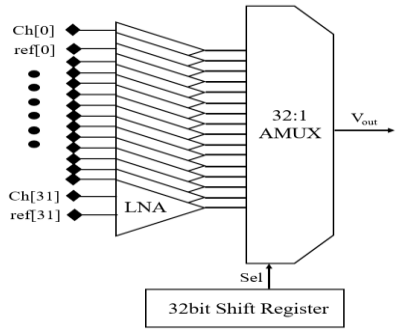


Fig. 6. Simplified schematic of the analog multiplexer.

C. Additional Amplifier

The additional amplifier was designed with the same capacitive feedback structure as the LNA. The gain of the additional amplifier was 18 dB, and the capacitance at the input stage was 1.2 pF. The total layout size was 60 µm × 100 µm.

III. RESULTS AND DISCUSSIONS

A. Noise Power Spectral Density

We measured the input referred noise of the LNA. As shown in Fig. 7, the low-frequency noise (flicker noise) is dominant below 10 Hz and thermal noise is dominant at higher frequencies. The output signal waveform was measured using an oscilloscope, and the results were extracted to calculate the input referred noise in MATLAB. The measured total noise level was approximately 3 µVrms, which was almost identical to the simulated value.

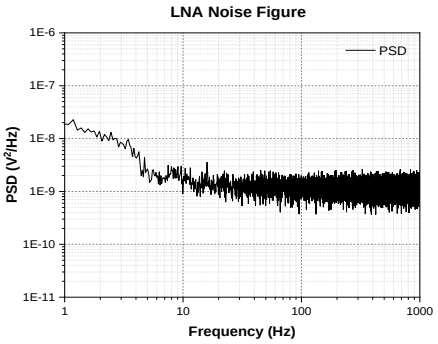


Fig. 7. Measured power spectral density of LNA.

B. Frequency Response

For frequency response of the integrated circuit, the overall bode plot of the designed analog front end is shown in Fig 8. As frequency range of target neural signal ECoG is below 300Hz, LPF was needed for cut off high frequency band. The total gain of the analog front end is about 58dB which is the result of adding low noise amplifiers and additional amplifiers.

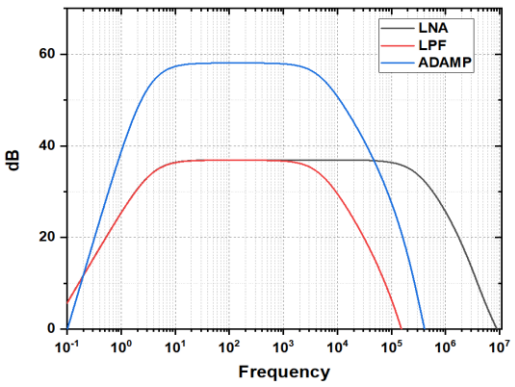


Fig. 8. AC response of Analog Front End

C. ECG signal measurement

Based on the designed integrated circuit in this paper, a customized test board was fabricated. The experiment setup is shown in Fig. 9. The signal line and ground line are located several centimeters apart in the same petri dish filled with Phosphate-buffered saline (PBS). A virtual ECG signal was applied to the saline solution at 2Hz by connecting electrodes to the fabricated board with an omnetics connector as shown in Fig. 9. We locate electrode on the surface of saline solution and measure ECG signal using Logic Pro 16 (Saleae, Inc). ECG signal measurement result is shown in Fig. 10. The result shows that the ECG signal is measured clearly with an amplitude of 180uV. We performed 2Hz~300Hz band pass filtering and supply noise filtering by post processing the measured data through MATLAB. We confirmed that up to an amplitude of 100uV was detected well. Also, as shown in Fig.11, there was no other noise except for low frequency (flicker noise) in the power spectral density graph.

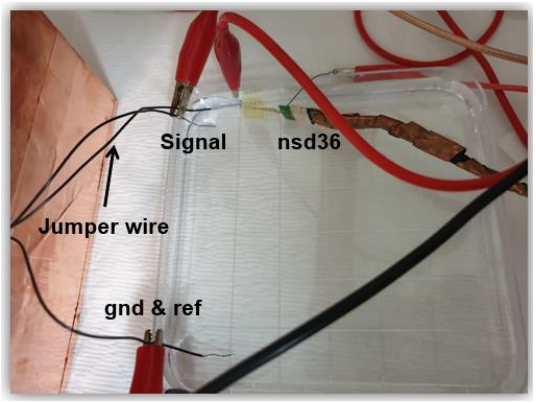


Fig. 9. Test setup for recording virtual ECG signal in PBS solution.

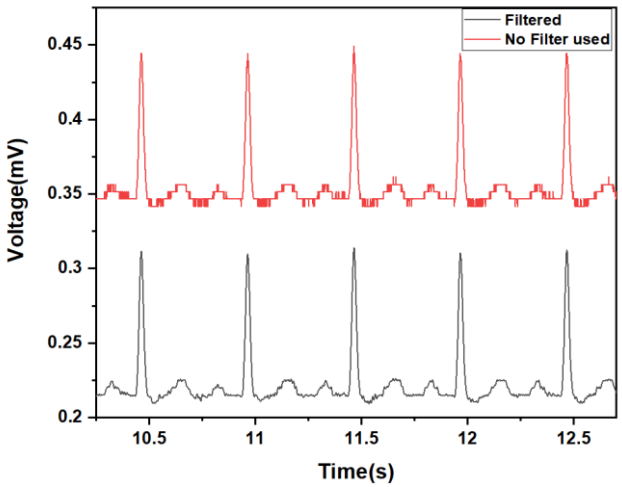


Fig. 10. Transient response of analog front-end when applying virtual 180uVpp ECG signal in PBS solution.

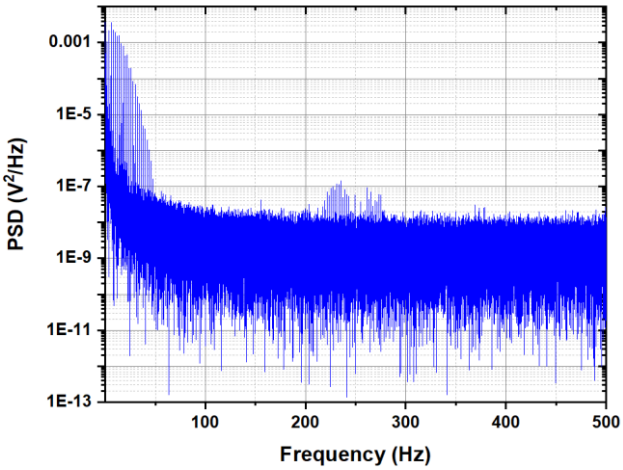


Fig. 11. Power spectral density of the low noise amplifier when measuring ECG signal in PBS solution.

IV. CONCLUSION

This paper proposes a 32ch channel neural recording system. It was designed as an interactive device between computer and brain for various neuroscientific studies. The high-resolution recording AFE, which applied LNA and LPF, supports signal acquisition near micro-volts. Through post-processing and analysis, it works as an effective tool in an extracellular recording. We designed 32ch LNA, LPF, Analog MUX, and shift register with low power consumption and low noise. Power spectral density and bode plot of the whole system shows better noise and gain characteristic. ECG measurement in the PBS environment exhibits that small ECG signals up to 100uV are well measured without disturbing noise.

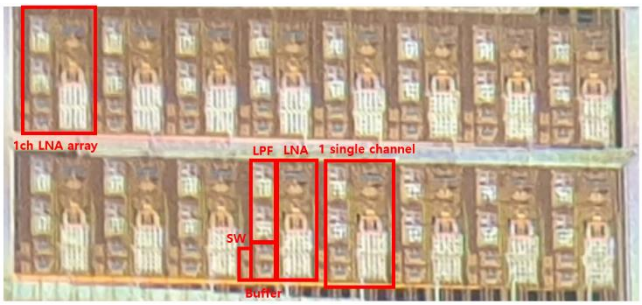


Fig. 12. The photograph of a neural signal detection module array

Fig. 12 shows a photograph of the designed 16 channel neural signal detection module array. The one neural signal detection module consists of a low noise amplifier, LPF, buffer and analog switch, and the total size is 190um×330um. 32 channel system consists of two 16 channel arrays.

As shown in Table 1. 32ch wireless neural recording system specification is summarized. For the 32ch neural recording system, only 1.2V supply voltage is needed with a total power consumption of 60uW. The total gain is 58dB with input referred noise of 3uVrms. Bandwidth is 2~300Hz for targeting the ECoG signal. Compared to systems manufactured by other groups for ECoG measurement, the noise is higher than other group, but it has advantages in terms of power consumption and size when compared per channel.

TABLE I. Comparison with other groups designed ECoG recording system

	[9]	[10]	This work
Number of channels	1	100	**32**
Supply voltage	1.2V	-	**1.2V**
Chip Area	-	25.38mm^2	**5mm^2**
Total Power Consumption	15uW	7.2mW (total) 4.5uW (LNA)	**60uW**
Total Gain	76.34dB	59.2dB	**58dB**
Bandwidth	25.4Hz ~ 25.6kHz	0.05Hz~240Hz	**2Hz ~ 300Hz**
Input referred noise	1.2uVrms	1.7uVrms	**3uVrms**

The designed wired system proved that it could detect a 100uVpp virtual neural signal in PBS solution. The designed system will be applied to an animal model to conduct a real neural signal measurement. In addition, we will proceed with

research focusing on the development of a multi-channel neural recording wireless system capable of implantation.

ACKNOWLEDGMENT

The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC) in Korea

REFERENCES

[1] M. Mollazadeh., E. Greenwald., N. Thakor., M. Schieber., and G. Cauwenberghs., "Wireless Micro ECoG Recording in Primates during Reach to Grasp Movements," in *2011 IEEE Biomedical Circuits and System Conference (BioCAS)*, pp. 237-240, 2011.

[2] G. Charvet. *et al.*, "WIMAGINE, 64-channel ECoG recording implant for human application," in *IEEE Engineering* in *Medicine and Biology Society Conference 2013*, vol. 23, no. 1, pp. 10-21, 2013.

[3] C. S. Mestais, G. Charvet, F. Sauter-Starace, M. Foerster, D. Ratel, and A. L. Benabid, "WIMAGINE: wireless 64-channel ECoG recording implant for long term clinical applications," *IEEE Trans. Neural Syst. Rehabil Eng*, vol. 23, no. 1, pp. 10-21, Jan. 2015.

[4] W. Wattanapanitch, M. Fee, and R. Sarpeshkar, "An energy-efficient micropower neural recording amplifier," *IEEE Trans. Biomed Circuits Syst.*, vol. 1, no. 2, pp. 136-47, Jun. 2007.

[5] R. R. Harrison, "The Design of Integrated Circuits to Observe Brain Activity," *Proceedings of the IEEE*, vol. 96, no. 7, pp. 1203-1216, Jul. 2008.

[6] R. R. Harrison and C. Charles, "A low-power low-noise CMOS for amplifier neural recording applications," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 6, pp. 958-965, Jun. 2003.

[7] J. Jang., J. H. Lee., N. R. Choi., and Y. K. Song., "16 channel ultralow power analog front-end for an implantable neural recording microsystem," *IDEC Journal of Integrated Circuits and System*, vol. 2, pp. 46-52, 2016.

[8] F. Zhang, J. Holleman, and B. P. Otis, "Design of ultra-low power biopotential amplifiers for biosignal acquisition applications," *IEEE Trans. Biomed Circuits Syst*, vol. 6, no. 4, pp. 344-55, Aug. 2012.

[9] J. S. Hong, M. C. Ling, M. Y. Haung, T. H. Tasi, and S. Y. Lee, "Analog Front-end Circuit with Low noise amplifier and High pass sigma delta modulator for an EEG or ECoG Acquisition System," in *IEEE International Symposium on Bioelectronics and Bioinformations 2011*, pp. 17-20, 2011.

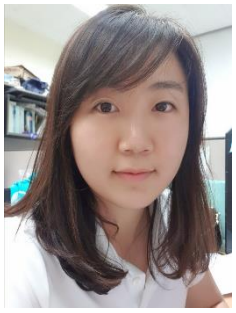
[10] G. S. Anderson. and R. R. Harrison., "Wireless Integrated Circuit for the Acquisition of Electrocorticogram Signals," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*, pp. 2952-2955, 2010.

Jung Woo Jang received the B.S. degree in Electric Engineering from Konkuk University, Seoul, Korea, in 2013 and is currently working toward Ph. D. degree in Nanoscience and Technology from Seoul National University, Korea.

His research interests include BMI system for recording neural signal, wireless data and power transmission, especially ultra-low power and low noise neural recording system.

Yu Ri Kim received the B.S. degree in Electric Engineering from Soongsil University, Seoul, Korea, in 2018 and is currently working toward Master. degree in Nanoscience and Technology from Seoul National University, Korea.

Her main research interest is designing ultra-low power system for Brain Machine Interface and recording Bio-Impedance.



Chae Eun Lee received the B.S degree in Electronics Engineering from Ewha Womans University, in 2017 and is currently working toward Ph.D. degree in Nanoscience and Technology from Seoul National University, Korea.

Her main research interest is developing neural stimulators, especially for visual prostheses, and wireless bidirectional power transfer for implantable Brain Machine Interface.

Yoon-Kyu Song received the B.S. and M.S. degree in Electric engineering form Seoul National University, Korea, in 1992 and 1994, respectively, and the Ph.D. degree from Brown University, Providence, RI, USA in 1999.

His research interests include basic and applied semiconductor optoelectronics, such as vertical cavity lasers and nanostructured light emitters.