A 10-GHz-Band Voltage-Controlled Oscillator Using Harmonic Shaping to Achieve a 184.9dB Figure-of-Merit for Ultra-Low-Jitter PLL Applications

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***Abstract* – This work presents a 10 GHz band voltage-controlled oscillator (VCO) using harmonic shaping, optimized for ultra-low-jitter phase-locked-loop applications. The proposed oscillator utilizes a transformer-coupled resonant network that simultaneously shapes the voltage waveform and enhances tank selectivity at multiple harmonic frequencies. By strengthening the second-harmonic voltage component, the oscillator exhibits an extended low-sensitivity region over the oscillation period, reducing phase perturbations introduced by the active devices. As a result, both close-in and far-out phase noise are effectively suppressed without additional filtering or common-mode resonance circuits. Operating at 10.8 GHz, the prototype achieves phase noise levels of −106.9 dBc/Hz and −130.1 dBc/Hz at 1 and 10 MHz offsets, respectively, while consuming 3.9 mW from the supply.**

***Keywords*—Voltage controlled oscillator (VCO), phase noise (PN), second harmonic resonance, transformer, flicker noise**

I. INTRODUCTION

To achieve high data rates, the design of high-performance phase-locked loops (PLLs) capable of generating high-frequency signals with ultralow jitter has become increasingly critical. However, designing such PLLs is challenging, as modern communication standards demand ever-stringent jitter performance while still meeting strict constraints on silicon area and power consumption. Digital PLLs (DPLLs) have therefore attracted attention due to their high programmability and robustness to PVT variations enabled by digitally controlled loop parameters [1]. The overall noise in a PLL can be categorized into in-band and out-band components. To achieve optimal jitter performance, the loop bandwidth must be carefully selected such that in-band and out-of-band noise contributions are well balanced. In-band noise mainly originates from the reference clock and the PLL building blocks, such as the quantization noise of the bang-bang PD (BBPD) and divider noise. With proper circuit design, these noise contributions can be sufficiently suppressed. Conversely, out-of-band noise is predominantly determined by the oscillator. Since the reference clock is fixed for a given application and its noise cannot be improved by circuit design, further jitter reduction in low in-band noise PLLs, relies heavily on out-

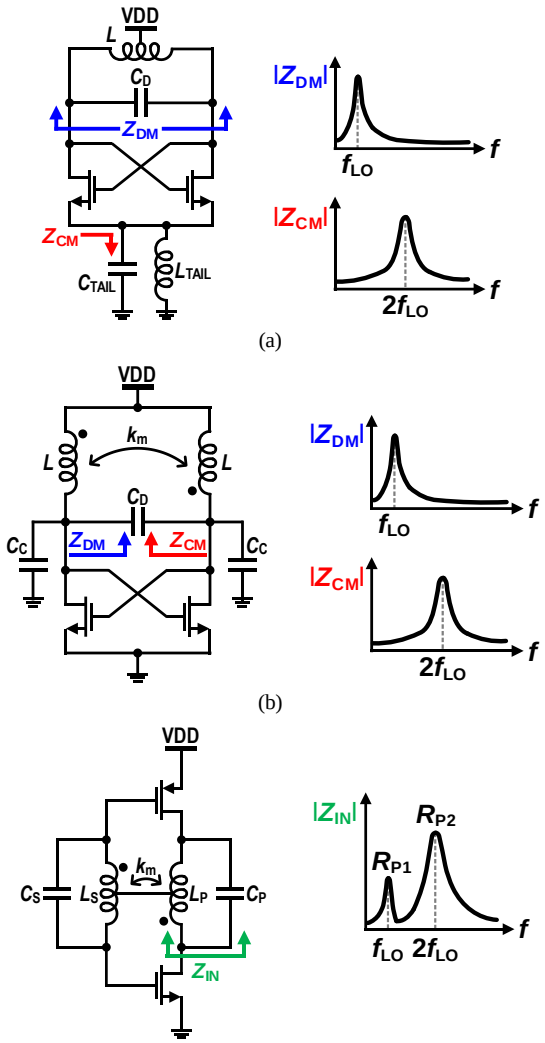

Fig. 1. Schematics of (a) VCO with explicit high CM $2f_{LO}$ impedance by tail tank; (b) VCO with implicit high CM $2f_{LO}$ impedance; (c) proposed inverse class-F VCO.

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band noise. Therefore, the design of the voltage-controlled oscillator (VCO) with a high figure of merit (FoM) is critical. A high FoM VCO not only minimizes out-of-band noise but also enables the PLL to achieve superior jitter performance under limited power budget required by modern systems.

The technique introduced by Hegazi et al., [2], which employs a tuned tail tank with high common-mode impedance at twice the oscillation frequency ($2f_{LO}$), prevents the differential cross-coupled g_m pair from entering triode operation, thereby improving the VCO FoM. This architecture is illustrated in Fig. 1(a). To further enhance the FoM, the VCO tail impedance at $2f_{LO}$ must be sufficiently high, which typically requires a high-quality factor (Q-factor) tail inductor. However, achieving a high Q-factor inductor comes at the expense of significant area consumption. Recently, Shahmohammadi et al. [3] and Murphy et al. [4] proposed an alternative VCO architecture that achieves implicit high common-mode impedance at $2f_{LO}$ by carefully selecting the mutual coupling factor of the inductor and the ratio between single-ended and differential capacitances. This technique, shown in Fig. 1(b), offers improved area efficiency compared to approaches relying on explicit tail inductors. Nonetheless, the inductor used in this design inherently suffers from reduced Q-factor due to unavoidable magnetic flux cancellation, which ultimately limits the attainable FoM.

In this work, an inverse class-F VCO with an intrinsic high Q-factor at $2f_{LO}$ is proposed, eliminating the need for either explicit or implicit common-mode (CM) resonant techniques [5]-[6]. By employing a transformer-based two-port resonator as the VCO tank, intrinsically high Q-factors can be simultaneously achieved at both the fundamental and second harmonic resonances. The proposed architecture is depicted in Fig. 1(c). Furthermore, the transformer provides drain-to-gate voltage gain, which effectively suppresses the noise contribution from the differential cross-coupled g_m pair, thereby enhancing the overall FoM.

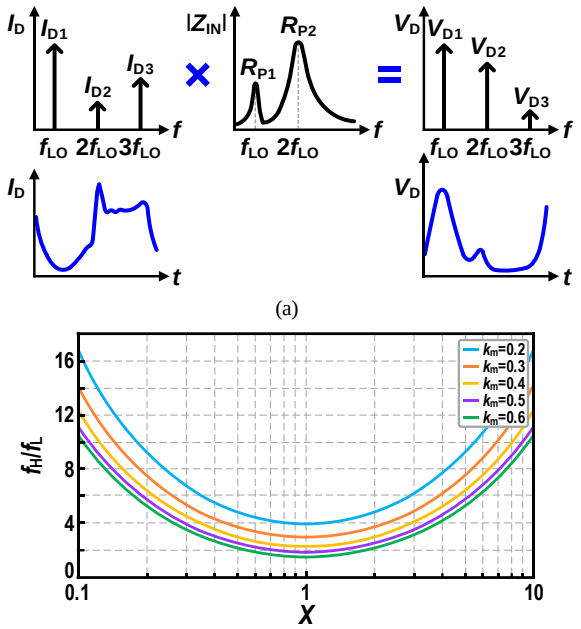
II. DESIGN METHODOLOGY

A. Concept of Inverse Class-F Operation

Fig. 2(a) illustrates the basic concept of the inverse class-F VCO operation. Owing to device nonlinearity, higher-order harmonic components such as $2f_{LO}$ and $3f_{LO}$ are generated in the drain current (I_D) along with the fundamental component. The transformer-based tank impedance ($|Z_{IN}|$) is designed to exhibit two resonant peaks, providing high impedance at both f_{LO} and $2f_{LO}$. When the harmonic-rich I_D is multiplied by the $|Z_{IN}|$, the resulting drain voltage (V_D) becomes enriched with second-harmonic component.

To generate a sufficiently large second harmonic component of V_D (V_{D2}), the transformer-based tank must be carefully designed to provide high impedance at both f_{LO} and $2f_{LO}$. The peak impedance frequencies are mainly determined by the X-factor, defined as the ratio of L_SC_S to L_PC_P, and by the mutual coupling factor between L_S and L_P (k_m). The ratio between the low (f_L) and high (f_H) resonant frequencies of the tank is given by

$$\frac{f_H}{f_L} = \sqrt{\frac{1+X+\sqrt{(1+X)^2-4X(1-k_m{}^2)}}{1+X-\sqrt{(1+X)^2-4X(1-k_m{}^2)}}} \quad (1)$$



(a)

(b)

Fig. 2. (a) Basic concept of the class-F VCO operation; (b) ratio of the two resonant frequencies, f_H and f_L, as a function of the X-factor.

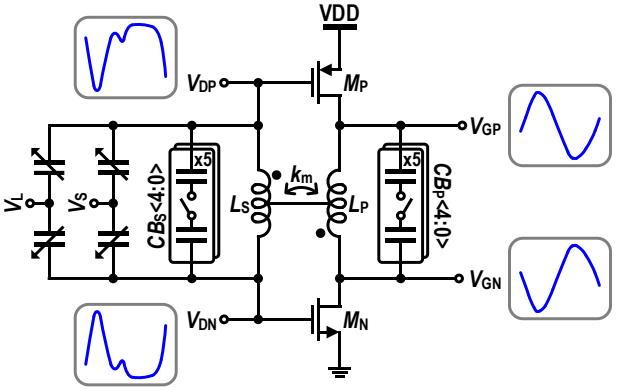


Fig. 3. Schematics of the inverse class-F VCO.

Fig. 2(b) plots the ratio f_H/f_L as a function of X for different values of k_m. To achieve $f_H/f_L = 2$, the coupling factor must be less than 0.6. In this design, the X-factor was selected to be as large as 3 in order to obtain a high drain-to-gate transformer gain [7].

B. Design of the Inverse Class-F VCO

The schematic of the proposed inverse class-F VCO is shown in Fig. 3. The oscillator employs a complementary NMOS/PNOS configuration, which provides the necessary negative resistance to sustain oscillation while improving symmetry of the output waveform and suppressing even-order distortion. Unlike conventional cross-coupled topologies, the complementary structure enhances current

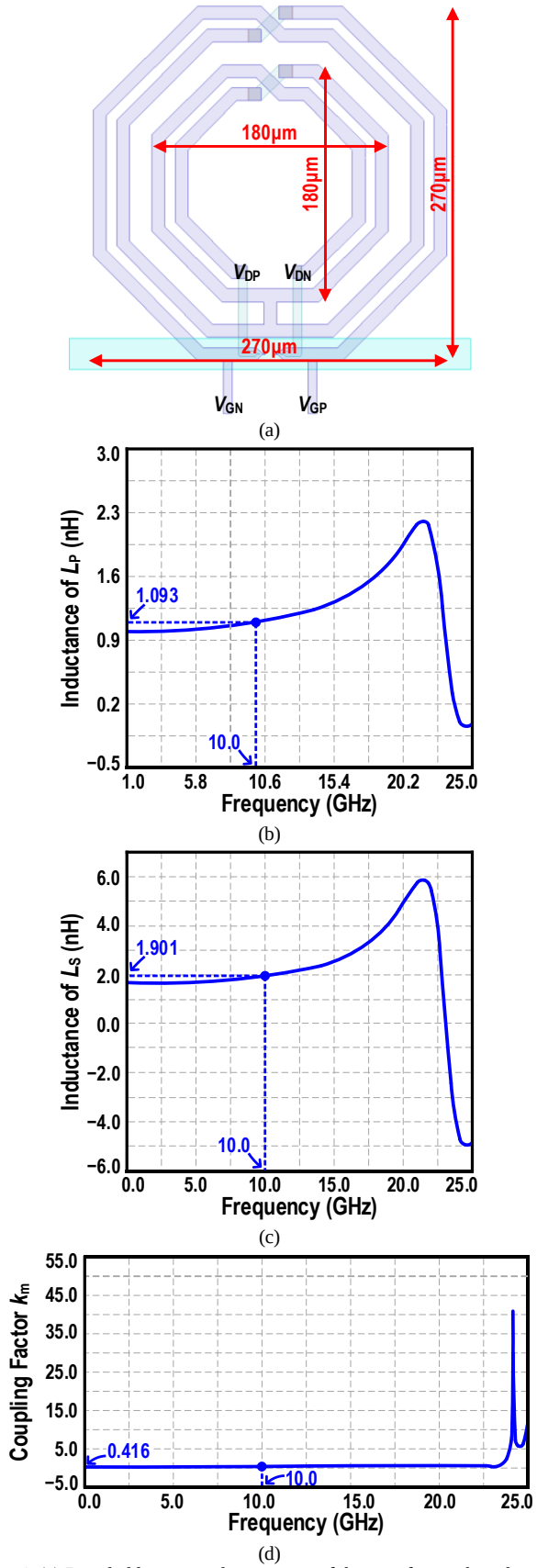


Fig. 4. (a) Detailed layout implementation of the transformer-based coil; (b) simulated inductance of L_P, (c) L_S, and (d) k_m with respect to the frequency.

efficiency and reduces flicker noise up-conversion. The VCO tank is implemented using a transformer-based dual-resonance tank, where the primary coil (L_S) and secondary coil (L_P) are magnetically coupled with a mutual coupling factor (k_m). This dual-resonant structure generates high impedance peaks at both the fundamental and second harmonic frequencies, which is essential for achieving inverse class-F operation with enriched second-harmonic voltage components. For frequency tuning, both coils are connected to 5-bit binary-weighted capacitor banks for coarse tuning. In addition, fine-tuning is achieved by two varactors – a small varactor with ~10 MHz tuning range ad a large varactor with ~200 MHz tuning range – connected across the primary coil. This combination provides both precise frequency control and wideband coverage.

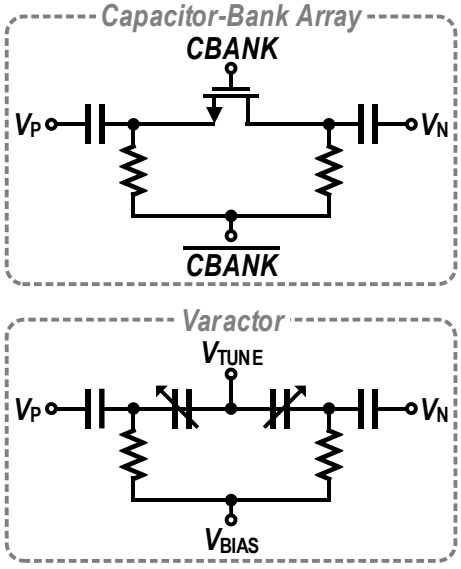


Fig. 5. (a) Schematics of switched capacitor-based capacitor bank; (b) schematics of varactor.

C. Design of the Transformer

The transformer-based dual-resonance tank is implemented by coupling a two-turn coil with smaller inductance (L_P) and a two-turn coil with larger inductance (L_S), as shown in the detailed layout in Fig. 4(a). Figs 4(b), (c), and (d) plot the simulated inductance of L_P, L_S, and k_m with respect to frequency. The simulated inductances of L_P and L_S at 10 GHz are 1.09 nH and 1.90 nH, respectively. This configuration enables the tank to achieve dual resonance at both the fundamental (f_{LO}) and second-harmonic ($2f_{LO}$) frequencies, which is essential for the inverse class-F operation.

D. Design of the Capacitor Bank & Varactor

The capacitor bank is implemented using a switched-capacitor structure, as illustrated in Fig. 5(a). To achieve area efficiency and wide tuning range, the bank is binary weighted, where the capacitance doubles and the resistance halves with each successive bit. This ensures that the high-pass filter pole location remains constant across all tuning codes. The varactor, shown in Fig. 5(b), is designed such that the impedances of the varactor, capacitor and resistor differ

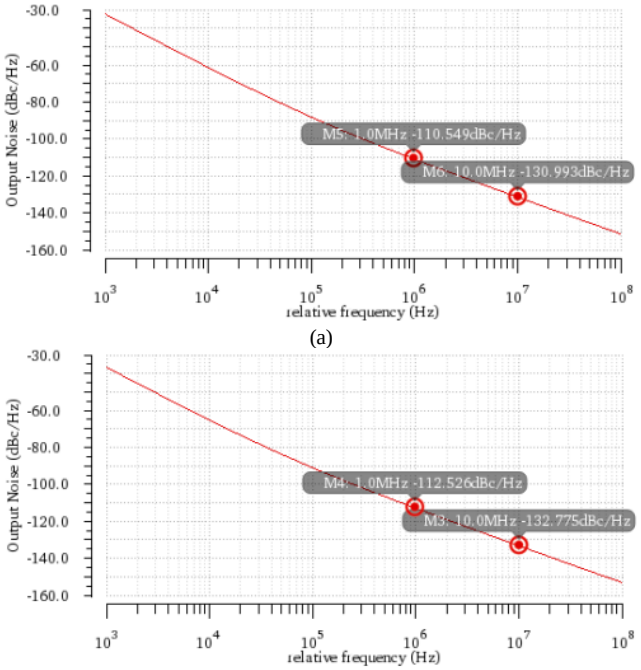


Fig. 6. Post layout phase noise simulation at (a)10 GHz and (b) 10.8 GHz.

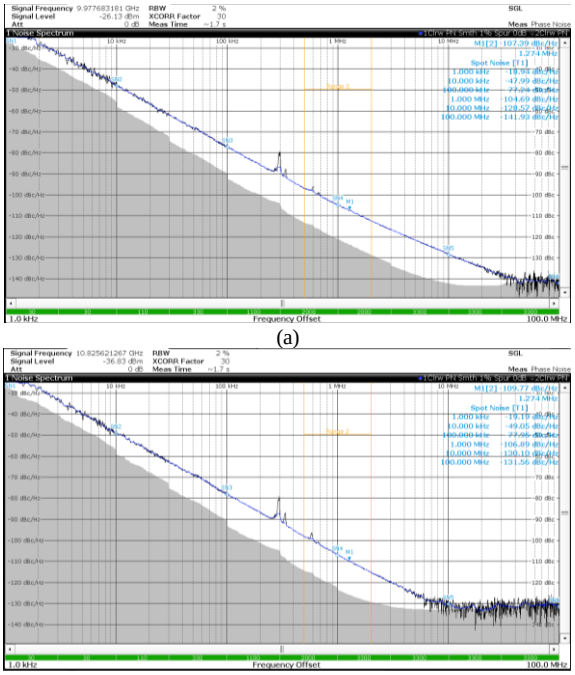


Fig. 7. Measured phase noise at (a)10 GHz and (b) 10.8 GHz.

by approximately a factor of ten. This design minimizes the amplitude modulation effect on the VCO and ensures stable oscillation across the entire tuning range.

III. RESULTS AND DISCUSSIONS

Fig. 6(a) shows the post-layout simulated phase noise of the proposed inverse class-F VCO at a 10 GHz oscillation frequency. The simulated phase noise was -110.5 dBc/Hz at a 1 MHz offset and -131.0 dBc/Hz at 10 MHz offset. Fig. 6(b) presents the simulated phase noise at 10.8 GHz, where the phase noise was -112.5 dBc/Hz at a 1 MHz offset and -132.8 dBc/Hz at 10 MHz offset. The measured phase noise results are shown in Figs. 7(a) and 7(b) for oscillation frequencies of 10 GHz and 10.8 GHz, respectively. In the thermal-noise-dominant region, i.e., frequency offsets above 10 MHz, the measured phase noise closely agrees with simulation, showing only about 2 dB degradation. However, in flicker-noise-dominant region, i.e., frequency offsets below 10 MHz, an additional degradation of up to 6 dB was observed. The flicker noise corner of the inverse class-F VCO is particularly sensitive to the impedance at the second-harmonic frequency. Due to the parasitic capacitances and process-voltage-temperature (PVT) variations, the second peak impedance can easily drift away from its optimal frequency, i.e., twice the oscillation frequency. This frequency shift results in optimal degradation of the phase noise performance in the flicker noise region. The total measured power consumption of the proposed inverse class-F VCO was only 3.9 mW. Fig. 8 shows the die micrograph of the proposed inverse class-F VCO, which occupies an active chip area of 0.027 mm^2.

The proposed inverse class-F VCO was fabricated for operation in a 10 GHz bang-bang phase detector (BBPD)-based digital PLL, as shown in Fig. 9(a). In this PLL

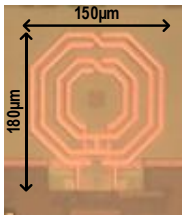


Fig. 8. Die micrograph.

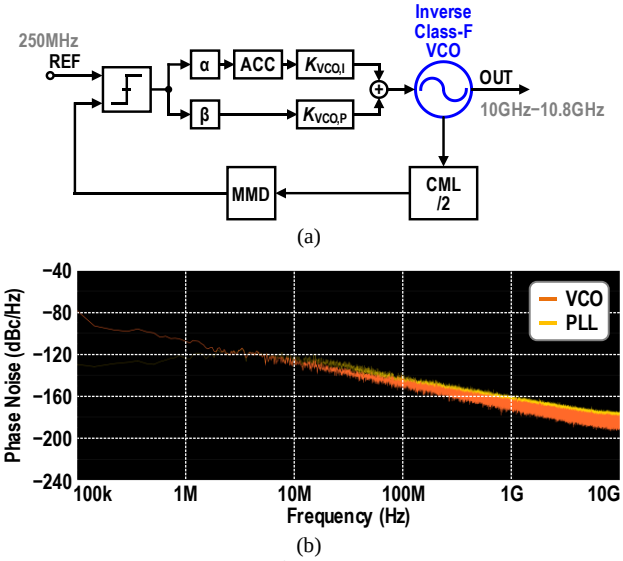


Fig 9. (a) Overall architecture of the 10 GHz BBPD-based digital PLL and (b) simulated phase noise performance of the PLL.

architecture, the in-band phase noise is dominated by the reference, whereas the out-of-band phase noise is dominated by the VCO [8]. Since the reference phase noise exhibits a white-noise characteristic, a relatively narrow loop bandwidth is required to minimize the integrated jitter. To enable such a narrow bandwidth design, the VCO must

TABLE I. Performance Comparison with the State-of-the-Art mmW-VCOs

	This Work	MWTL'23 [9] Y. Li	JSSC'18 [10] Y. Hu	MWTL'23 [11] K. Wang
Process	28 nm CMOS	55 nm CMOS	28 nm CMOS	180 nm CMOS
Architecture	Inverse Class-F VCO	Implicit Class-F_{23} +Tunable XFMR	Implicit Class-F_{23} +3rd-HM Extraction	Inductive Tuned VCO
Output freq., f_{OUT} (GHz)	10.0 to 10.8	12.9 to 15.88	27.3 to 31.2	3.4 to 4.04
Tuning Range	7.69%	20.4%	13.3%	17.2%
100kHz PN (dBc/Hz)	–77.95	–80	–82.8	–80
10MHz PN (dBc/Hz)	–130.1	–128.6	–126.1	–132
Power, P_{DC} (mW)	3.9	15	12	3.6
Active area (mm²)	0.027	0.1	0.15	0.75
$FOM @10MHz	**184.87**	**180.10**	**184.03**	**178.48**
^FOM_T @10MHz	182.59	186.22	186.31	183.19

$FOM = –PN + 20log($f_{OUT}$/Δ$f$) – 10log($P_{DC}$/1 mW) (dB)
^FOM_T = FOM + 20log(TR/10)

exhibit low phase noise performance, particularly in the 1 to 10 MHz offset frequency range. Fig. 9(b) presents the simulated phase noise performance of the PLL by MATLAB. Loop noise such as divider, BBPD, DLF noise are simulated noise from cadence, while the VCO and the reference noise are measured data. The loop bandwidth was set to approximately 2 MHz. Using the proposed inverse class-F VCO, the PLL achieves an rms jitter of 60 fs, integrated from 1 kHz to 100 MHz, which demonstrates sufficiently low phase noise performance.

IV. CONCLUSION

This paper presented a 10-to-10.8 GHz inverse class-F VCO that achieves low flicker noise and high FoM through a transformer-based dual-resonance tank. By utilizing a two-port transformer resonator, intrinsically high-Q impedance peaks were realized at both the fundamental and second-harmonic frequencies without employing any explicit or implicit common-mode resonance techniques. This enables rich second-harmonic voltage generation, enhancing waveform flatness and improving the impulse sensitivity function (ISF), which in turn suppresses phase noise originating from the g_m devices. The proposed VCO achieved a measured phase noise of -106.9 dBc/Hz at 1 MHz offset and -130.1 dBc/Hz offset from a 10.8 GHz carrier, while consuming 3.9 mW of power. Compared with conventional VCOs with implicit or explicit high second harmonic common mode impedance, the proposed inverse class-F topology achieves superior phase noise and power efficiency without requiring additional resonant networks. These results confirm that the inverse class-F architecture is a promising candidate for low-jitter, power-efficient phase-locked loops in next-generation high-speed communication systems.

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