A Fractional-N ADPLL-Based GFSK Modulator with ADC-Assisted TDC and DCO Gain Calibration

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Abstract - **This paper proposes a Fractional-N ADPLL-based GFSK modulator for BLE/IoT applications. The proposed system employs an ADC-assisted coarse-to-fine TDC and achieves wide modulation bandwidth without loop bandwidth constraints through two-point modulation (TPM). However, modulation accuracy can be degraded by quantization error (QE) from the delta-sigma modulator (DSM) required for fractional-N operation, TDC nonlinearity, and gain mismatch between the TPM slow and fast paths. Noting that these issues must be resolved sequentially, this paper proposes a sequential calibration flow that first corrects the phase-measurement path before compensating the modulation gain. Background TDC gain calibration removes DSM QE using sign-sign LMS, foreground TDC nonlinearity calibration compensates TDC nonlinearity through 52 sub-zone-based bias code correction, and DCO gain calibration corrects slow/fast path gain mismatch in real time using a fast-converging error-sign algorithm. The proposed modulator is designed in Samsung 28-nm CMOS with a 4.801-GHz DCO operating frequency, which is divided by two to generate a 2.4-GHz BLE RF output. It is designed and verified through post-layout simulation at a 1.0-V supply voltage, consuming 12.42 mW and occupying a 0.4135-mm² core area. Through TDC nonlinearity calibration, the RMS jitter is reduced from 474.6 fs to 440.7 fs and the fractional spur is improved by 2.95 dB, achieving a final FSK error of 2.83%, confirming the effectiveness of the proposed calibration-based GFSK modulation scheme.**

Keywords — **All-Digital Phase-Locked-Loop (ADPLL), Gaussian Frequency Shift Keying (GFSK), Time-to-Digital Converter (TDC), DCO Gain Calibration**

I. INTRODUCTION

With the increasing proliferation of Bluetooth Low Energy (BLE) and IoT devices, the demand for low-power, low-cost wireless transmitters continues to grow. In such applications, Gaussian Frequency Shift Keying (GFSK) modulation is widely adopted [1], as it not only achieves excellent spectral efficiency through Gaussian filtering but also facilitates low-power transceiver implementation. These characteristics align directly with the power budget constraints of battery-operated IoT devices, and as a result, GFSK has become a key modulation scheme in numerous low-power wireless communication standards, including BLE.

To accurately generate such GFSK signals, the frequency synthesizer in the transmitter must provide a very fine frequency resolution. All-Digital Phase-Locked-Loop (ADPLL) has attracted attention as a promising architecture to meet this requirement, owing to its ease of digital implementation and the benefits of process scaling; however, an integer-N architecture alone cannot achieve the required frequency resolution. To address this, fractional-N architecture is adopted, which requires a Delta-Sigma Modulator (DSM) to dither the division ratio of the multi-modulus divider (MMDIV) on a cycle-by-cycle basis. However, the DSM inherently introduces quantization error (QE), which, if uncompensated, becomes a major source of phase noise degradation and fractional spurs. Therefore, implementing a fractional-N ADPLL-based GFSK modulator requires a calibration technique that accurately estimates and removes this QE. The modulator proposed in this paper adopts a structure in which a 4.8-GHz DCO output is divided by two to generate a 2.4-GHz BLE RF output.

In an ADPLL, this quantization error (QE) is compensated through a separate digital calibration block. This calibration exploits the correlation between the DSM output QE and the TDC output; since the error induced in the TDC output by the DSM QE is proportional to the product of the QE and the TDC gain, this correlation can be used to estimate the TDC gain and digitally cancel the QE. However, the performance of this QE cancellation is inherently limited by the accuracy of the TDC itself. In particular, the TDC often exhibits nonlinearity due to process, voltage, and temperature (PVT) variations, which introduces a deterministic phase error into the TDC output, generating fractional spurs and consequently degrading GFSK modulation accuracy. Therefore, in addition to calibrating the TDC gain, a separate calibration is required to compensate for the TDC nonlinearity itself [2], [3].

Meanwhile, PLL-based frequency modulators have a fundamental limitation in that their low-pass characteristic, determined by the loop bandwidth, restricts the modulation bandwidth. Modulation signals with frequency components higher than the loop bandwidth are attenuated by the negative feedback of the PLL, making it difficult to implement wideband modulation schemes such as GFSK through a single path alone. To overcome this limitation,

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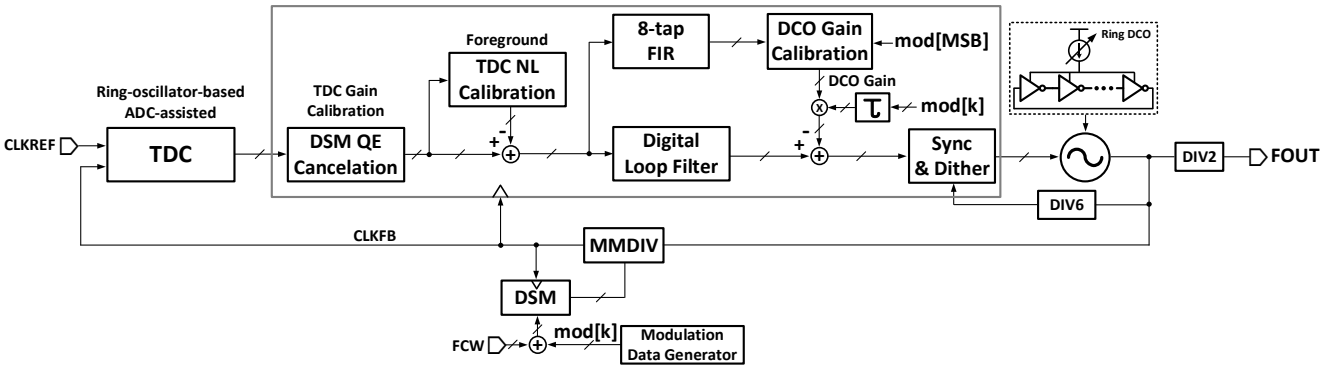

Fig. 1 Block diagram of the proposed ADPLL-based GFSK Modulator.

two-point modulation (TPM) is widely used, in which the modulation data is simultaneously injected into two paths—the slow path (through the divider via the frequency control word (FCW), exhibiting a low-pass characteristic) and the fast path (directly controlling the DCO, exhibiting a high-pass characteristic)—so that the overall system achieves an all-pass response. However, this all-pass characteristic holds only when the gains of the two paths are precisely matched; if a gain mismatch exists between the slow and fast paths, it causes modulation distortion, such as overshoot or insufficient tracking of the target level during the modulation transient. Therefore, in an ADPLL-based modulator employing two-point modulation, DCO gain calibration is essential to maintain gain matching the slow and fast paths in real time [4], [5].

It should be noted that these three issues—DSM QE, TDC nonlinearity, and slow/fast path gain mismatch—cannot be resolved independently. DCO gain calibration uses the residual phase error remaining in the TDC output as an error signal to detect the gain mismatch between the slow and fast paths. However, this TDC output contains both the DSM QE and the deterministic TDC nonlinearity; unless these two components are removed first, DCO gain calibration risks converging based on a distorted error signal. Therefore, only after the errors caused by the DSM QE and the TDC nonlinearity have been resolved can the residual error be reliably used as an indicator of gain mismatch.

This paper proposes a fractional-N ADPLL-based GFSK modulator that sequentially resolves the three issues discussed above—DSM-induced quantization error, TDC nonlinearity, and slow/fast path gain mismatch arising from two-point modulation—according to this dependency. The contribution of this paper lies not in the novelty of the individual calibration techniques themselves, but in jointly securing both modulation accuracy and modulation bandwidth from a practical chip-implementation standpoint. First, background TDC gain calibration digitally removes the quantization error induced by the DSM. Second, foreground TDC nonlinearity calibration compensates for the deterministic phase error caused by TDC nonlinearity, reducing fractional spurs and improving modulation accuracy. Third, based on this reliable phase error information, DCO gain calibration matches the gain between the slow and fast paths, maintaining the all-pass characteristic of two-point modulation and minimizing modulation distortion. These three calibrations operate sequentially—TDC gain calibration, TDC nonlinearity calibration, and DCO gain calibration—ultimately realizing a GFSK modulator that satisfies both wide modulation bandwidth and high accuracy.

The remainder of this paper is organized as follows. Section II introduces the overall system architecture of the proposed GFSK modulator, followed by the ADC-assisted coarse-to-fine TDC structure and the operating principle of ADPLL-based two-point modulation. Section III describes the three calibration techniques—TDC gain calibration, TDC nonlinearity calibration, and DCO gain calibration—in detail. Section IV presents the post-layout simulation results based on a 28-nm CMOS process, and Section V concludes the paper.

II. ARCHITECTURE

A. Overview of GFSK Modulation System

The proposed GFSK modulator limits the input bitstream using a Gaussian filter and converts it into instantaneous frequency deviation, which is delivered to the wireless transmitter through the modulation path of the PLL itself, without a separate RF mixer.

Fig. 1 shows the overall block diagram of the proposed system. The phase difference between CLKREF and CLKFB is converted into a digital code by the TDC, and this TDC output is used for two purposes: first, in the QE cancellation path that estimates and removes the quantization error (QE) induced by the DSM, and second, to compensate for the error caused by the nonlinearity of the TDC itself. The phase error signal, with QE removed, passes through the digital loop filter to control the DCO (Digitally Controlled Oscillator); in this process, an 8-tap FIR filter smooths the error signal for the DCO gain calibration path. The DCO retiming block realigns the control word to the DCO clock, thereby preventing glitches that may arise from path delay differences among the bits constituting the control word. Meanwhile, the dithering block applies ΔΣ-based dithering to the DCO LSB code, shaping the quantization noise out of the loop bandwidth, thereby increasing the

effective frequency resolution of the DCO and improving in-band phase noise. The DCO operates in the 4.8-GHz band, and this output passes through a divide-by-2 block to generate the 2.4-GHz signal corresponding to the actual BLE RF output.

In parallel with this background PLL operation, three calibrations—TDC gain, TDC nonlinearity, and DCO gain calibration—are performed sequentially, as detailed in Section III. The modulation data mod[k], generated by the modulation data generator, is injected into the slow path and the fast path, whose detailed operating principles are described in Section II-C.

B. ADC-Assisted Coarse-to-Fine Conversion TDC

The TDC is a key block within the ADPLL that converts the phase difference between the reference clock (CLKREF) and the feedback clock (CLKFB) into a digital code, and this phase-error information serves as the basis for the QE cancellation and loop filter operations described above. Fig. 2 shows the block diagram of the proposed ADC-assisted coarse-to-fine TDC. The proposed TDC adopts a two-stage coarse-to-fine conversion architecture to simultaneously achieve a wide detection range and high resolution. Coarse conversion is performed through a ring-oscillator counter and multi-phase encoding. Fine conversion uses a flash ADC to finely convert the sub-phase interval that the coarse conversion cannot represent, thereby obtaining a resolution beyond the coarse resolution. By combining the resulting coarse code and fine code, a wide range and high resolution—difficult to achieve simultaneously with a single architecture—can be obtained together.

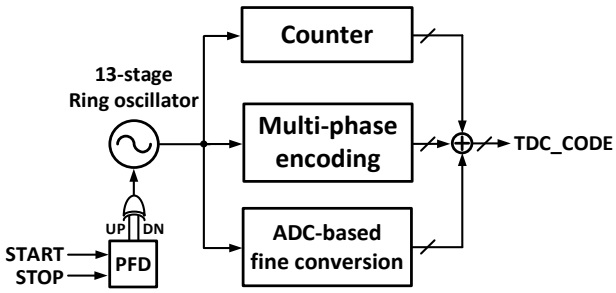

Fig. 2. Block diagram of the ADC-Assisted TDC.

Meanwhile, the TDC exhibits structural nonlinearity due to PVT variation in each delay cell constituting the ring oscillator of the coarse stage. This nonlinearity introduces a deterministic error into the TDC output code, which appears as a fractional spur during fractional-N operation, thereby degrading the accuracy of GFSK modulation. The detailed design and characteristics of this TDC structure are described in [3].

C. Two-Point Modulation Scheme

As mentioned in the Introduction, PLL-based frequency modulators fundamentally have a low-pass characteristic in which the modulation bandwidth is limited by the loop bandwidth. To overcome this, the proposed structure adopts a two-point modulation (TPM) scheme. Fig. 3 shows the proposed TPM structure. TPM simultaneously injects the modulation data (mod[k]) into two paths: the slow path and the fast path. The slow path is the path through which mod[k] changes the division ratio of the feedback divider via the DSM and MMDIV, reflected through the TDC and the digital loop filter (DLF); as shown in Fig. 3, it exhibits a low-pass frequency response. The fast path is the path through which mod[k] multiplied by the DCO gain is directly summed with the DLF output and applied to the DCO, exhibiting a high-pass frequency response. When the frequency responses of the two paths are combined in a complementary manner, the overall modulation path theoretically achieves an all-pass response, enabling a wide modulation bandwidth regardless of the loop bandwidth.

However, this all-pass characteristic holds only under the precondition that the gains of the two paths are precisely matched. If a gain mismatch exists between the slow path and the fast path, it causes modulation distortion, such as overshoot or insufficient tracking of the target level during the modulation transient. In addition to gain mismatch, delay mismatch between the two paths also affects modulation accuracy; if a time delay difference exists between the points at which the slow-path and fast-path signals are combined, an instantaneous frequency error can occur during the transient interval. This paper focuses on the gain mismatch issue and proposes DCO gain calibration, which compensates for it in real time, in Section III.

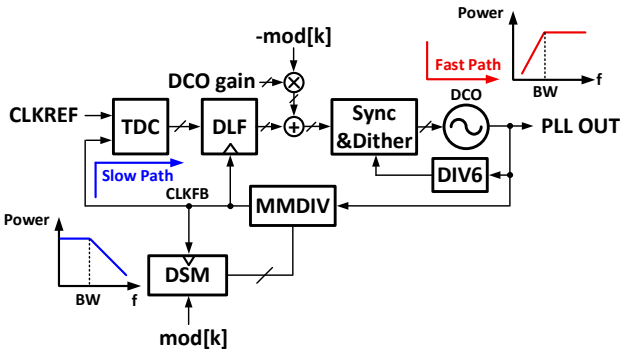

Fig. 3. Block diagram of the two-point modulation.

III. CALIBRATION TECHNUQES

A. TDC Gain Calibration

TDC gain calibration is a technique that estimates and removes the quantization error (QE) caused by the DSM in a background manner. Fig. 4 shows the block diagram of the proposed TDC gain calibration. The QE from the DSM output introduces an error into the TDC output code, and this error code appears as the product of the QE and the TDC gain (QE × TDC gain). Therefore, the TDC gain can be estimated by exploiting the correlation between the TDC output and the DSM QE. However, since a delay exists in the signal path before the QE generated by the DSM is actually reflected in the TDC code, appropriate delays (Z^{-A}, Z^{-B}) must be applied to the TDC MSB and the DSM QE MSB, respectively, to align the timing of the two signals so that the correlation can be accurately obtained. As shown in

Fig. 4, the product of the time-aligned TDC MSB and DSM QE MSB is applied to an integrator to derive the TDC gain. This estimated gain is then multiplied by a separately delayed QE (Z^{-c}) to obtain the TDC code value attributable to the DSM QE, and this value is subtracted from the raw TDC output to remove the QE component. This structure corresponds to a sign-sign least-mean-square (LMS) algorithm that updates the gain using only the sign information of the residual error and the DSM QE, rather than their actual error values, resulting in a simple hardware implementation.

The update magnitude of the gain estimate is determined by the integrator coefficient α; a larger α leads to faster convergence but a larger steady-state error, whereas a smaller α results in slower convergence but a more precise gain estimate. The converged TDC gain estimate is subsequently used to continuously predict the DSM QE in the digital domain, and this predicted QE value is subtracted from the TDC output in real time, thereby removing the phase noise degradation caused by the DSM in a background manner.

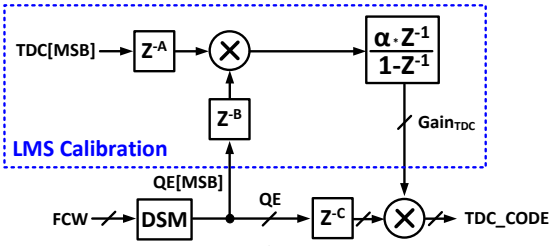

Fig. 4. Block diagram of the TDC gain calibration.

B. TDC Nonlinearity Calibration

TDC nonlinearity calibration is a technique that compensates, in a foreground manner, for the structural nonlinearity of the TDC caused by PVT variation in each delay cell constituting the ring oscillator. The proposed TDC consists of a 13-stage ring oscillator, and each stage interval obtained from the coarse conversion is subdivided into four sub-zones based on the fine ADC code, resulting in a total of 13 × 4 = 52 sub-zones. Fig. 5 shows the block diagram of the proposed TDC nonlinearity calibration, illustrating the structure in which the TDC output is classified into one of the 52 sub-zones through a sub-zone encoder. The detailed configuration of these sub-zones is described in [3].

During calibration operation, the FCW is applied as a near-integer channel with an irregular value. This induces the phase error to sweep evenly across all 52 sub-zones in a complex pattern rather than being biased toward a specific sub-zone, and the TDC error values observed in each sub-zone during a measurement interval of approximately 100 μs are accumulated to compute an average value for each zone. The reason for taking the average is that the TDC error observed at each instant contains not only the component caused by the TDC's nonlinearity but also components caused by the DSM and other system noise. However, while the DSM and other noise components converge to zero when averaged over a sufficiently long time, the component caused by TDC nonlinearity appears as a deterministic error in the same direction repeatedly within the same sub-zone and therefore remains in the average value. Accordingly, the average error value obtained for each sub-zone can be regarded as the bias attributable to the TDC nonlinearity in that zone.

The bias codes for the 52 sub-zones measured in this way are stored in memory, and thereafter, whenever a TDC output occurs during normal operation, the sub-zone to which the corresponding phase error belongs is identified, and the corresponding bias code is subtracted from the TDC output in real time, thereby removing the deterministic phase error caused by the nonlinearity.

The effect of this calibration is confirmed through the reduction of the fractional spur in the phase noise plot of the PLL. Since the deterministic error caused by TDC nonlinearity appears as a fractional spur during fractional-N operation, comparing the phase noise plots before and after calibration directly demonstrates that the nonlinearity calibration effectively suppresses the fractional spur.

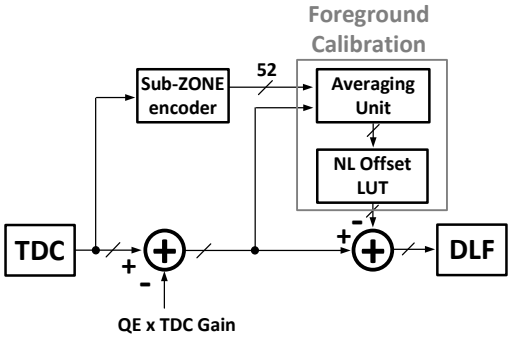

Fig. 5. Block diagram of the TDC nonlinearity calibration.

TABLE 1. Effect of the 25°C Foreground-Calibrated NL Offset on GFSK Performance Under Temperature Variation

Temperature	TDC NL Cal.	Fractional spur (dBc)	RMS jitter (fs)	FSK error (%)
-25°C	None	-54.95	293.3	2.10
-25°C	25°C-calibrated(fixed)	-60.17	348.5	2.58
75°C	None	-45.58	653.8	3.89
75°C	25°C-calibrated(fixed)	-47.01	620.4	4.04

Table 1 compares the performance at -25°C and 75°C with the sub-zone offset obtained from 25°C foreground calibration applied without re-calibration (25°C-calibrated, fixed) versus without offset compensation (None). At both temperatures, applying the fixed offset improves the fractional spur but increases the RMS jitter. This is attributed to the offset—simulated at a different temperature—still suppressing the deterministic sub-zone nonlinearity, but no longer accurately, leaving a residual component that manifests as broadband noise. Consequently, the FSK error also increases relative to the uncompensated case (-25°C: 2.10%→2.58%; 75°C: 3.89%→4.04%). This indicates that retaining the room-temperature sub-zone offset across a wide temperature range can degrade modulation accuracy, supporting the need for foreground re-calibration at the operating temperature prior to GFSK modulation.

C. DCO Gain Calibration

DCO gain calibration detects and corrects, in real time, the gain mismatch between the slow path and the fast path, and operates only after both TDC gain calibration and TDC nonlinearity calibration have converged, as discussed in Section I.

TDC gain calibration is a prerequisite for the PLL to reach lock; without it, the PLL fails to lock, and the phase error does not settle into its steady-state distribution. Under this unlocked condition, the sub-zone-averaged TDC output reflects a mixture of the true offset and residual quantization error (QE), rather than the pure sub-zone nonlinearity offset. Consequently, TDC nonlinearity calibration can extract a valid offset only once the PLL has reached lock, which is why TDC gain calibration must precede TDC nonlinearity calibration.

This dependency is further confirmed by transient simulation. Fig. 6 shows the time-domain convergence or divergence of the TDC gain under three calibration sequence conditions (normal, reversed, and parallel), while Fig. 7 shows the resulting distortion in the DCO output (modulation waveform). Under the normal sequence, the TDC gain converges stably, and the DCO output accordingly toggles cleanly between two target levels. In contrast, reversing the order or running the calibrations in parallel prevents the PLL from reaching lock, causing the TDC gain to diverge and a contaminated sub-zone offset to be injected, which severely distorts the DCO output. Notably, in the parallel condition, divergence begins precisely when the foreground measurement result is applied — consistent with the offset being contaminated by residual QE prior to lock, as discussed above. These results experimentally confirm that the proposed calibration sequence is not merely preferable but necessary.

Fig. 8 shows the block diagram of the proposed DCO gain calibration. The TDC code is extracted as an error signal through an 8-tap FIR filter, and this error is used, together with the correlation with the sign of mod[k], to determine the direction of the gain mismatch. When mod[k] is positive, the DCO should operate to increase the frequency, and when negative, to decrease it. However, if the gains of the slow path and the fast path are not precisely matched, the code applied to the DCO shifts the frequency either excessively or insufficiently relative to the target, and this mismatch appears as a residual phase error in the TDC output. Thus, by observing the correlation between the sign of mod[k] and the error, it is possible to determine whether the DCO gain code has been applied excessively or insufficiently.

The resulting correlation value is multiplied by the gain step (μ) and then accumulated in an integrator (Σ) clocked by CLKFB to produce the DCO gain value. An error-sign algorithm is adopted as the gain correction algorithm. Whereas the sign-sign LMS method used in TDC gain calibration (Section III-A) adjusts the value by a fixed gain step using only the signs of the error and the reference, the error-sign method determines the correction amount using both the sign and the magnitude of the error together with the gain step. This enables the gain value to converge considerably faster than with the sign-sign method.

The converged DCO gain value is multiplied by mod[k] of the fast path and applied to the DCO, as shown in Fig. 1; at this point, mod[k] passes through a delay element (τ) to align its arrival time with that of the slow path before being multiplied by the gain. This is intended to compensate for the delay mismatch between the slow and fast paths and is a separate timing-alignment process distinct from the calibration loop that corrects the gain mismatch.

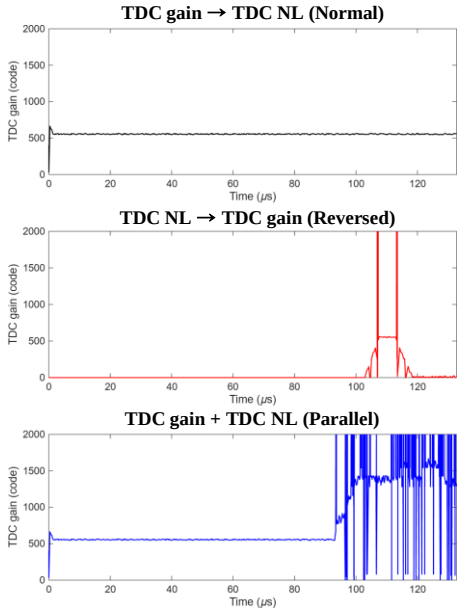

Fig. 6. TDC gain convergence under normal, reversed, and parallel calibration sequences.

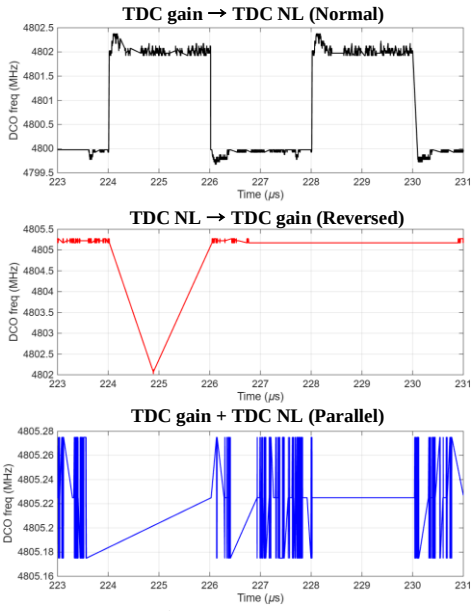

Fig. 7. Modulation waveform under normal, reversed, and parallel calibration sequences.

The DCO gain calibration logic consists of 67 flip-flops and 3,112 combinational cells, occupying an area of 1,724 μm² — approximately 0.42% of the total core area. TDC gain calibration improves the intrinsic performance of the ADPLL core (spur suppression); because estimation stability is prioritized over convergence speed for this stage, a sign-

sign LMS calibration, which processes only the sign of the residual error, is employed. In contrast, DCO gain calibration begins only after TDC gain calibration and TDC nonlinearity calibration have converged and must be completed before GFSK data transmission begins. The error-sign algorithm therefore employs a coarse-to-fine step-size transition ($2^6 \rightarrow 2^1$). A large step size is used initially to accelerate convergence and shorten the transmission-readiness time, after which the step size is reduced to minimize the steady-state error and ensure modulation accuracy (FSK error). Given that this algorithm occupies only 0.42% of the total core area, the associated hardware overhead is justified.

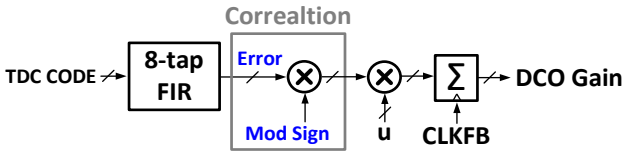

Fig. 8. Block diagram of the DCO gain calibration.

Fig. 9 shows that DCO gain mismatch causes overshoot or insufficient tracking during the modulation transient, whereas a properly converged DCO gain calibration eliminates such distortion. Table 2 summarizes the design parameters of the proposed GFSK modulator architecture.

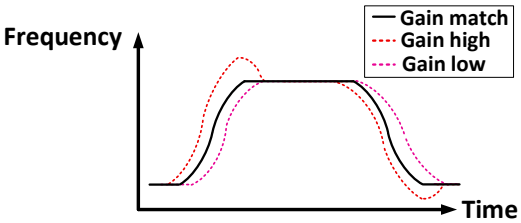

Fig. 9. Effect of DCO gain mismatch on transient response.

TABLE 2. Summary of Design Parameters

Parameter	Value
Reference clock frequency	80 MHz
PLL loop bandwidth	1 MHz
Fractional-N DSM order	MASH 1-1
Digital loop filter structure	PI-type (proportional + integral)
TDC gain step (α)	2^0
DCO gain step (μ)	2^6 (coarse) -> 2^1(fine)
8-tap FIR filter	8-tap moving average filter
Fast-path delay (τ)	12.5 ns
TDC gain convergence time	10us (background)
TDC nonlinearity calibration time	100us (foreground)
DCO gain convergence time	800us (background)
Total Convergence time	910us

IV. SIMULATION RESULTS

The proposed Fractional-N ADPLL-based GFSK modulator is designed in Samsung 28-nm CMOS process, and the overall layout is shown in Fig. 10. The circuit operates at a 1.0-V supply voltage, consuming a total of 12.42 mW. The overall chip core area occupies approximately 0.4135 mm².

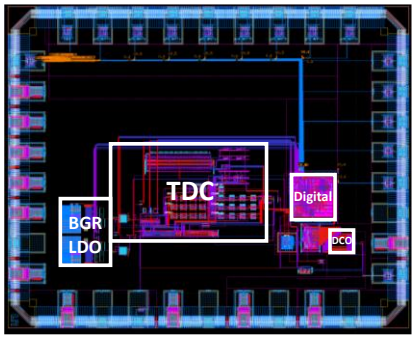

Fig. 10. Layout view of ADPLL-based GFSK modulator implemented using 28-nm CMOS process.

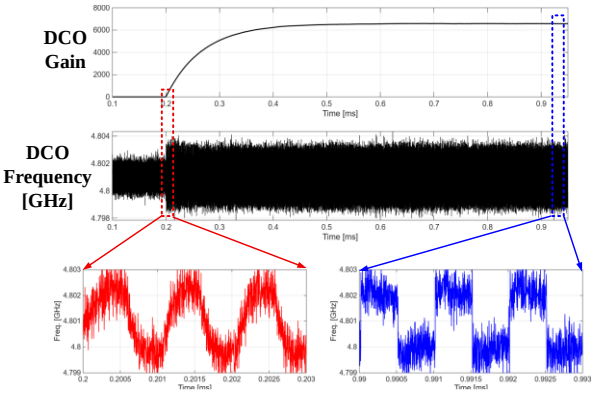

Fig. 11. Transient response of DCO gain calibration convergence.

Fig. 11 shows the convergence characteristics of the DCO gain calibration. The DCO gain estimate rapidly converges toward the target value within the initial hundreds of microseconds and subsequently reaches a stable steady state. The magnified waveforms at the bottom of the figure show the DCO frequency response during the initial convergence interval (red) and after convergence is completed (blue), respectively; distortion in the modulation waveform is observed in the initial interval where the gain has not yet been accurately corrected, whereas after convergence, the DCO frequency accurately and stably tracks the modulation data.

All digital cells, including the calibration logic, are implemented in RTL, while the remaining analog blocks are simulated with STAR-RC-based post-layout parasitic extraction. The DCO, however, is represented as a behavioral model due to the excessive simulation time required for closed-loop simulation with a fully extracted netlist; this model is designed to reflect the phase noise obtained from post-layout simulation.

Fig. 12 compares the phase noise plots before and after applying TDC nonlinearity calibration. Without calibration (TDC gain calibration only), the largest fractional spur is -50.52 dBc, and the RMS jitter integrated over the 10-kHz to 100-MHz band is 474.6 fs. With TDC nonlinearity calibration applied, the deterministic phase error caused by delay-cell variation in the ring oscillator is suppressed, reducing the fractional spur to -53.47 dBc (a 2.95-dB improvement) and improving the RMS jitter to 440.7 fs. The resolution-bandwidth (RBW)-based constant used to

normalize the offset-frequency axis of the phase noise plot is determined solely by the FFT length and the average period and is therefore expected to remain identical regardless of the calibration condition. These results demonstrate that the 52 sub-zone-based bias code correction effectively removes the phase error caused by the structural nonlinearity of TDC. Under the calibrated condition, the in-band phase noise within the PLL loop bandwidth is confirmed to be approximately −111 dBc/Hz (@2.4005 GHz), and this value is used as the comparison metric in Table 5.

Table 3 compares the fractional spur, RMS jitter, and FSK error across calibration stages. Notably, applying TDC nonlinearity calibration alone, without TDC gain calibration, results in a fractional spur (-29.44 dBc) and RMS jitter (7206.4 fs) that are worse than with no calibration applied at all, and the FSK error fails to converge. As discussed in Section III, this occurs because the PLL cannot reach lock without TDC gain calibration, causing TDC nonlinearity calibration to measure a sub-zone offset contaminated with residual quantization error, which further distorts the phase-error signal. This result experimentally corroborates the theoretical requirement that TDC gain calibration must precede TDC nonlinearity calibration.

Fig. 13 shows the DCO output of the proposed modulator in the time domain. The top plot shows the Gaussian-filtered data waveform when an <11110000> pattern is applied at 2 Mbps, and the bottom plot shows the corresponding time-domain response of the DCO frequency. A signal with a frequency deviation of ±1 MHz around the 4.801-GHz DCO center frequency accurately transitions according to the data pattern, which corresponds to the BLE standard condition (±500 kHz) at the 2.4-GHz RF output after divide-by-2. This result is achieved by DCO gain calibration matching the gain between the slow and fast paths, under the condition that the accuracy of the phase-measurement path has been secured through TDC gain calibration and TDC nonlinearity calibration. The FSK error is computed from the DCO output (4.801 GHz) rising-edge timestamps. For each symbol interval (0.5 μs at 2 Mbps), the leading and trailing 20% of the interval are excluded, and the average frequency is calculated over the remaining steady-state portion and compared to the target frequency deviation of ±1 MHz. The RMS of the resulting errors is normalized to the ±1 MHz peak frequency deviation to define the FSK error. The simulated FSK error was 2.83%.

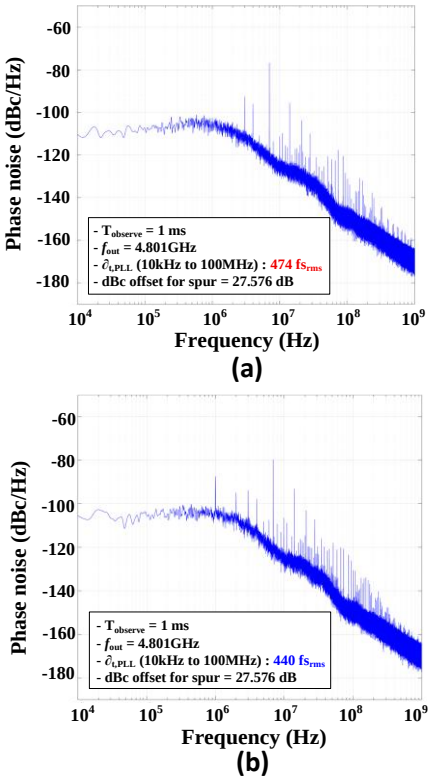

Fig. 12. Simulated phase noise (a) without and (b) with TDC nonlinearity calibration.

TABLE 3. Fractional Spur, RMS Jitter, and FSK Error Under Different Calibration Conditions

	Fractional spur (dBc)	RMS jitter (fs)	FSK error (%)
No Cal.	-39.96dBc	4659.9fs	Not converged
TDC gain Cal. only	-50.52dBc	474.6fs	2.85%
TDC NL Cal. only	-29.44dBc	7206.4fs	Not converged
TDC gain +NL Cal.	-53.47dBc	440.7fs	2.83%

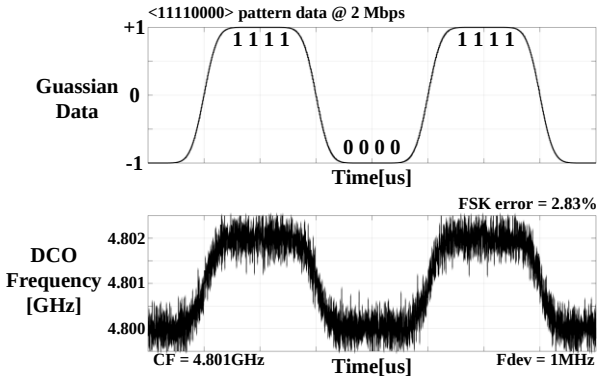

Fig. 13. Simulated transient response of the GFSK modulator.

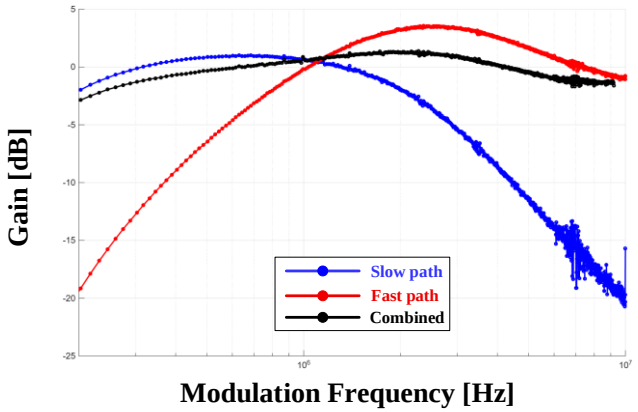

Fig. 14. Simulated modulation transfer functions of the slow path, fast path, and combined path.

The transfer functions, shown in Fig. 14, were obtained by sweeping a chirp signal from 100 kHz to 10 MHz at the tx-data input under three conditions: slow path alone, fast path alone, and combined (both paths driven simultaneously). The slow and fast paths cross near 1.14 MHz, matching the designed 1-MHz PLL loop bandwidth, and exhibit complementary low-pass and high-pass characteristics, respectively. The combined response shows a gain ripple of 1.87 dB over 1–5 MHz, with no -3-dB roll-off observed up to 10 MHz — confirming that two-point modulation extends the modulation bandwidth by at least an order of magnitude beyond the intrinsic loop bandwidth.

Fig. 15 shows the GFSK modulation spectrum of the proposed modulator referenced to the 2.4-GHz RF output. The frequency-domain characteristics of a properly modulated signal are confirmed under the conditions of a 2.4005-GHz carrier frequency, a 500-kHz frequency deviation, a 2-Mbps data rate, and BT = 0.5, which is consistent with the time-domain result in Fig. 13 through the divide-by-2 relationship.

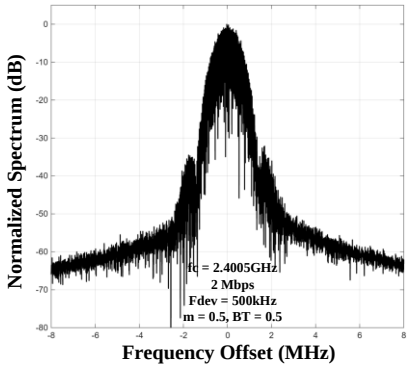

Fig. 15. Simulated GFSK modulation spectrum

Table 4 presents the power breakdown analysis of the GFSK Modulator. As reported in [3], the TDC employs a flash-ADC-assisted 6-bit sub-conversion using 63 comparators, accounting for the largest share of power consumption (43.6%). This additional power enables a high-speed reference clock and fine TDC resolution, directly contributing to the improved in-band phase noise performance. The Ring DCO and output buffer account for the second-largest share (38.9%), reflecting the overhead of driving a 4.8 GHz output at full digital swing.

While the total power consumption (12.42 mW) exceeds that of the prior works listed in Table 5 (1.55–5.3 mW), this additional power funds the three-stage sequential calibration (TDC gain, TDC nonlinearity, DCO gain) and two-point modulation architecture, achieving the lowest in-band phase noise (-111 dBc/Hz) and a competitive FSK error (2.83%) among the compared works.

TABLE 4. Power Breakdown of the Proposed GFSK Modulator

Power Consumption (mW)	
TDC [3]	5.42 (43.6%)
Ring DCO + Buffer	4.83 (38.9%)
Digital logic + Loop filter	1.37 (11.0%)
Divider	0.80 (6.4%)
Total	12.42 (100.0%)

TABLE 5. Performance Summary and Comparison

	This Work	**TCAS-1 '22 [6]**	**RFIC '20 [7]**	**JSSC'19 [8]**	**JSSC'19 [9]**
Tech (nm)	**28**	40	65	40	28
Result Type	**Post-layout Sim.**	Measurement	Measurement	Measurement	Measurement
PLL Architecture	**ADPLL**	ADPLL	BB-DPLL	DPLL	Analog PLL
Operating Frequency (GHz)	**2.4005**	2.4	1.2	2.402	2.428
GFSK Modulation	**Two -Point**	Two -Point	Two -Point	Single -Point	Single -Point
Data Rate (Mb/s)	**2**	0.971	1	1	1
Background Calibration	**yes**	yes	no	yes	yes
In-Band Noise (dBc/Hz)	**-111 (@2.4005 GHz)**	-94 (@2.4GHz)	-98 (@1.2 GHz)	-85 (@2.402 GHz)	-83 (@2.428 GHz)
FSK error (%)	**2.83**	2.3	2.86 (EVM)	9.1	2.84
Power (mW)	**12.42**	4.85	5.3	1.55	3.97
Core Area (mm^2)	**0.4135**	0.48	0.383	0.017	0.53

V. CONCLUSION

This paper has presented a Fractional-N ADPLL-based GFSK modulator that employs an ADC-assisted coarse-to-fine TDC and two-point modulation to achieve wide modulation bandwidth without loop bandwidth constraints.

To address the three key issues arising in this architecture—DSM-induced quantization error, TDC nonlinearity, and slow/fast path gain mismatch—TDC gain

calibration, TDC nonlinearity calibration, and DCO gain calibration were sequentially applied. TDC nonlinearity calibration reduced the RMS jitter from 474 fs to 440 fs and improved the fractional spur by approximately 3 dB, while DCO gain calibration corrected the slow/fast path gain mismatch in real time, achieving accurate GFSK modulation with an FSK error of 2.83%.

The proposed modulator was designed and verified in a Samsung 28-nm CMOS process through post-layout simulation, consuming 12.42 mW at a 1.0-V supply and occupying a 0.4135-mm² core area. As summarized in Table 5, the proposed modulator achieves competitive modulation accuracy—an in-band phase noise of -111 dBc/Hz (@2.4005GHz) and an FSK error of 2.83% compared with prior work. These results confirm the effectiveness of the proposed sequential calibration flow in jointly securing phase-measurement accuracy and modulation bandwidth, demonstrating its feasibility for low-power wireless transmitters in BLE and IoT applications.

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REFERENCES

[1] S. M. Dartizio et al., "34.2 A 380μW and −242.8dB FoM Digital-PLL-Based GFSK Modulator with Sub-20μs Settling Frequency Hopping for Bluetooth Low-Energy in 22nm CMOS," *2025 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2025, pp. 1-3.

[2] C. -W. Yao et al., "A 14-nm 0.14-psrms Fractional-N Digital PLL With a 0.2-ps Resolution ADC-Assisted Coarse/Fine-Conversion Chopping TDC and TDC Nonlinearity Calibration," in *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3446-3457, Dec. 2017.

[3] Solmon Shin, Hyunwoo Son, Youngsik Kim and Shinwoong Kim. (2025). A 1.12-ps Resolution Flash ADC-assisted Coarse-to-fine Time-to-digital Converter with Adaptive Reference-voltage Calibration and Digital Linearity Correction. JOURNAL OF SEMICONDUCTOR TECHNOLOGY AND SCIENCE, 25(6), 711-720.

[4] R. B. Staszewski, J. Wallberg, Chih-Ming Hung, G. Feygin, M. Entezari and D. Leipold, "LMS-based calibration of an RF digitally controlled oscillator for mobile phones," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 3, pp. 225-229, March 2006.

[5] Kim, N.-S. An ADPLL-Based GFSK Modulator with Two-Point Modulation for IoT Applications. *Sensors* 2024, *24*, 5255.

[6] H. Huang et al., "A 2 nJ/bit, 2.3% FSK Error Fully Integrated Sub-2.4 GHz Transmitter With Duty-Cycle Controlled PA for Medical Band," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no. 12, pp. 5018-5029, Dec. 2022.

[7] Y. Liu, W. Rhee and Z. Wang, "A 1Mb/s 2.86% EVM GFSK Modulator Based on ΔΣ BB-DPLL without Background Digital Calibration," *2020 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Los Angeles, CA, USA, 2020, pp. 7-10.

[8] X. Chen et al., "Analysis and Design of an Ultra-Low-Power Bluetooth Low-Energy Transmitter With Ring Oscillator-Based ADPLL and 4 x Frequency Edge Combiner," in *IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1339-1350, May 2019.

[9] S. Yang, J. Yin, H. Yi, W. -H. Yu, P. -I. Mak and R. P. Martins, "A 0.2-V Energy-Harvesting BLE Transmitter With a Micropower Manager Achieving 25% System Efficiency at 0-dBm Output and 5.2-nW Sleep Power in 28-nm CMOS," in *IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1351-1362, May 2019.

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