A 12V-to-Sub-1V Dual Inductor Middle Hybrid Step-Down Converter with Reduced Inductor Current

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***Abstract* – Modern data centers require high-current, low-voltage power supplies with high power density to support AI accelerators and high-performance processors. To achieve high power density, passive components such as inductors must be minimized while maintaining high conversion efficiency. In addition, reducing the voltage stress across power devices enables the use of low-voltage MOSFETs with lower on-resistance and smaller silicon area. This paper presents a 12V to 0.6-1V hybrid step down DC-DC converter for data center applications. By employing hybrid conversion architecture with mode transition, the proposed converter reduces inductor current, enabling compact implementation and improved efficiency over a wide output voltage range.**

***Keywords*— Data center, Power density, Mode Transition, Inductor current**

I. INTRODUCTION

The increasing power demand of modern AI accelerators and high-performance processors has driven the need for efficient 12V to 0.6-1V power conversion in data center power delivery systems. A lower supply voltage enables processors to draw higher load currents for high-performance operation, making low-voltage, high-current power delivery essential.

Conventional buck converters suffer from large inductor currents under high-current operation, resulting in significant inductor DCR loss and necessitating the use of bulky inductors. In addition, the power switches must withstand the full input voltage, requiring high-voltage LDMOS devices that occupy a large silicon area. Furthermore, since the voltage conversion ratio of a buck converter is proportional to the duty cycle, converting 12V to a sub-1V output requires an extremely small duty cycle. This leads to challenges such as increased switching loss, limited control resolution, degraded transient performance, and difficulties in high-frequency operation.

To overcome these limitations, various hybrid step-down converters have been proposed [1]–[4]. These converters employ switched-capacitor networks to achieve high step-down conversion ratios while reducing switch voltage stress and extending the effective duty cycle. As shown in Fig. 1, however, their output current is delivered through the dual-inductor output stage. Although the load current is shared by the two inductors, the total inductor current remains high.

To reduce the total inductor current, the converters in [5] and [6] employ capacitive current paths that deliver a portion of the output current, as shown in Fig. 2. However, their inductor-current reduction becomes less effective as the duty ratio decreases.

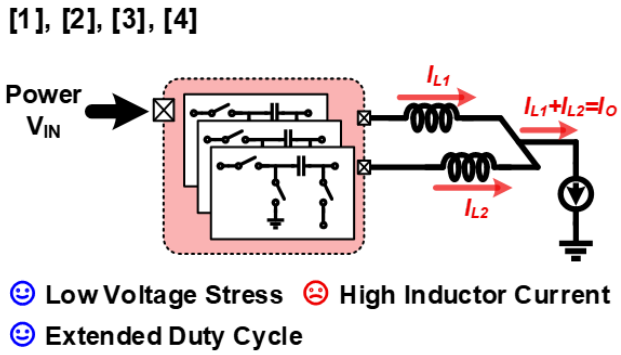

Fig. 1. Hybrid Converters with Dual-Inductor Output Stages [1] – [4].

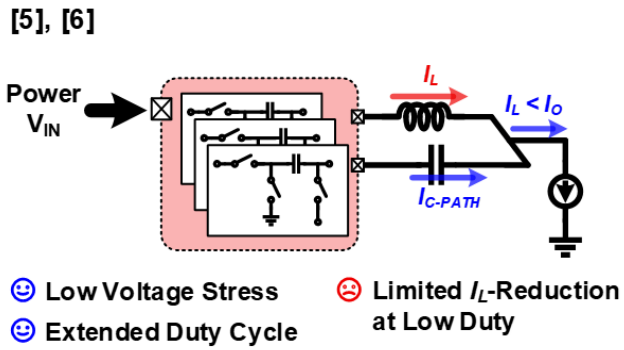

Fig. 2. Hybrid Converters with Capacitive Current Paths [5], [6].

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In this work, a dual-inductor middle hybrid step-down converter with two operating modes is proposed. By selecting the operating mode according to the duty ratio, the proposed converter maintains a low I_L/I_O ratio, even in the low-duty-ratio region.

II. ANALYSIS OF PROPOSED CONVERTER

A. Proposed Topology

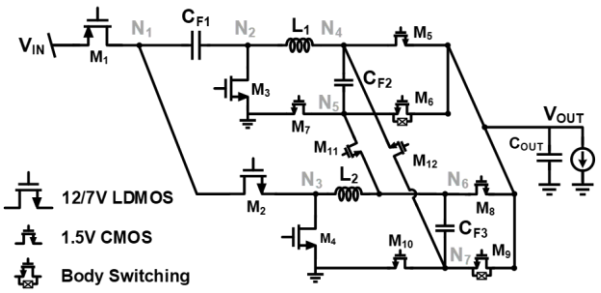


Fig. 3. Proposed step-down converter.

Fig. 3 shows the proposed hybrid step-down converter. The proposed power stage consists of two inductors, three flying capacitors, and twelve power switches. Power switches M_1, M_3, and M_4 are implemented using 7V LDMOS devices, and M_2 employs a 12V LDMOS device to withstand the maximum input voltage. The remaining switches, M_5-M_{12}, are realized using eight 1.5V CMOS devices. M_6 and M_9 are implemented with body-switching techniques.

The proposed topology places the inductors between two conversion stages. The first stage adopts a double step-down structure to reduce the voltage stress and switching loss across the power devices. The second stage employs a 2:1 switched capacitor (SC) network. A portion of the output current is supplied through the flying capacitors rather than the inductor, substantially reducing the inductor current stress. In addition, switches M_{11} and M_{12} form a bridge connection between the two stages, allowing a voltage of $3V_{OUT}$ to be applied across the inductor. As a result, the voltage conversion ratio is further extended compared to the case without the bridge structure.

B. Operation of Proposed Converter

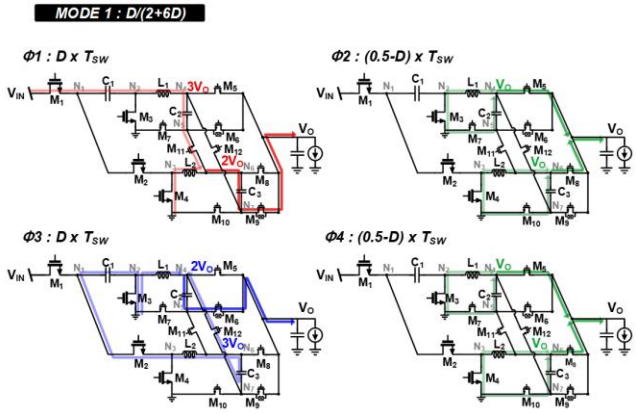
Mode 1 Operation

During Φ1, L_1 is energized while flying capacitors C_{F1}, C_{F2}, C_{F3} are charged. Meanwhile, L_2 releases its stored energy to the output. During Φ2, both inductors are discharged and deliver energy to the load. In addition, C_{F2} and C_{F3} supply a portion of the output current, thereby reducing the current flowing through the inductors. During Φ3, C_{F1} is discharged to energize L_2, while L_1 continues to discharge. Finally, Φ4 operates similarly to Φ2, where both inductors transfer their stored energy to the output.

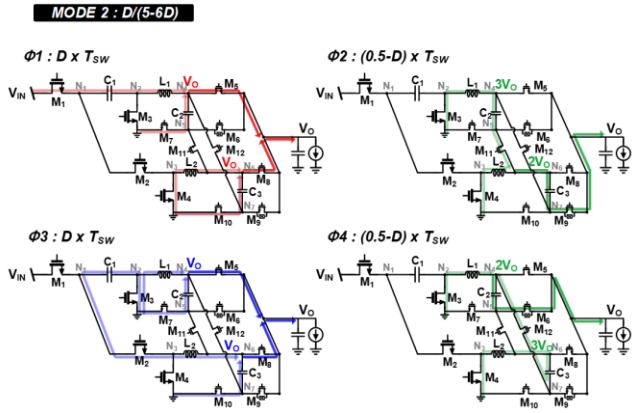
Applying the volt-second balance condition,

$$\left(\frac{V_{IN}}{2} - 3V_O\right)D - V_O(0.5 - D) - 2V_O D - V_O(0.5 - D) = 0$$

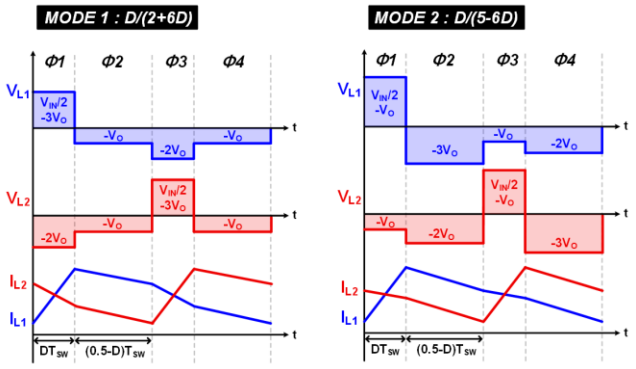
$$\frac{V_O}{V_{IN}} = \frac{D}{2 + 6D} \quad (0 < D < 0.5) \qquad (1)$$



(a) Mode 1 operation.



(b) Mode 2 operation.



(c) Inductor voltage and current.

Fig. 4. (a) Mode 1 operation. (b) Mode 2 operation. (c) Inductor voltage and current.

Mode 2 Operation

Mode 2 is derived by reconfiguring the switched-capacitor network in the second stage while maintaining the same operation in the first stage. Unlike Mode 1, where the series-connected capacitor configuration precedes the

parallel-connected configuration, Mode 2 reverses the operating sequence. Specifically, the inductor and capacitors are first configured in parallel and subsequently reconfigured in series. This modification changes the voltage applied to the inductors.

Applying the volt-second balance conditions,

$$\left(\frac{V_{IN}}{2} - V_O\right)D - 3V_O(0.5 - D) - V_O D - 2V_O(0.5 - D) = 0$$

$$\frac{V_O}{V_{IN}} = \frac{D}{5 - 6D} \quad (0 < D < 0.5) \tag{2}$$

Mode Transition

To reduce the inductor current, mode transition is employed according to the duty cycle. Therefore, the current delivered by the inductors and flying capacitors is analyzed to derive the inductor current ratio with respect to the output current.

Fig. 4(a) shows the current distribution in Mode 1. The output current is supplied by both the inductors and the flying capacitors. The current contribution of the inductors and flying capacitors in each switching phase is analyzed as follows.

$$\begin{cases} I_{O,\Phi1} = DI_{L1} + DI_{L2} \\ I_{O,\Phi2} = (0.5 + D)I_{L1} + 0.5I_{L2} \\ I_{O,\Phi3} = DI_{L1} + DI_{L2} \\ I_{O,\Phi4} = 0.5I_{L1} + (0.5 + D)I_{L2} \end{cases} \tag{3}$$

By summing the current contributions from all switching phases, the overall output current is obtained as

$$I_O = I_{O,\Phi1} + I_{O,\Phi2} + I_{O,\Phi3} + I_{O,\Phi4} \tag{4}$$

$$I_O = (1 + 3D)I_{L1} + (1 + 3D)I_{L2} \tag{5}$$

Therefore, with the total average inductor current defined as $I_L = I_{L1} + I_{L2}$, the inductor current ratio in Mode 1 can be expressed as

$$\frac{I_L}{I_O} = \frac{1}{1 + 3D} \quad (0 < D < 0.5) \tag{6}$$

Fig. 4(b) shows the current distribution in Mode 2. Similar to Mode 1, the current contribution of the inductors and flying capacitors in each switching phase is analyzed as follows.

$$\begin{cases} I_{O,\Phi1} = (1 - D)I_{L1} + 0.5I_{L2} \\ I_{O,\Phi2} = (0.5 - D)I_{L1} + (0.5 - D)I_{L2} \\ I_{O,\Phi3} = 0.5I_{L1} + (1 - D)I_{L2} \\ I_{O,\Phi4} = (0.5 - D)I_{L1} + (0.5 - D)I_{L2} \end{cases} \tag{7}$$

By summing the current contributions from all switching phases, the overall output current is obtained as

$$I_O = (2.5 - 3D)I_{L1} + (2.5 - 3D)I_{L2} \tag{8}$$

Using the same definition of I_L, the inductor current ratio in Mode 2 is given by

$$\frac{I_L}{I_O} = \frac{1}{2.5 - 3D} \quad (0 < D < 0.5) \tag{9}$$

Based on the derived (I_L/I_O) expressions for Mode 1 and Mode 2, the inductor current ratio as a function of the duty cycle is plotted in Fig. 5. When the duty ratio is lower than 0.25, Mode 2 provides a lower inductor current ratio. In contrast, when the duty ratio is higher than 0.25, Mode 1 becomes more effective in reducing the inductor current.

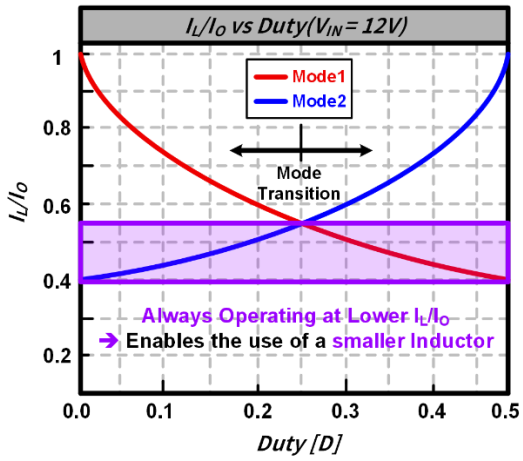


Fig. 5. I_L/I_O versus Duty Ratio.

Therefore, by selecting the proper operating mode according to the duty cycle, the proposed converter maintains a low inductor current over the entire operating range.

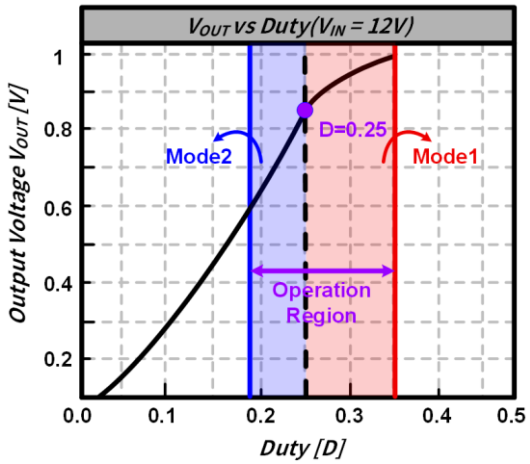


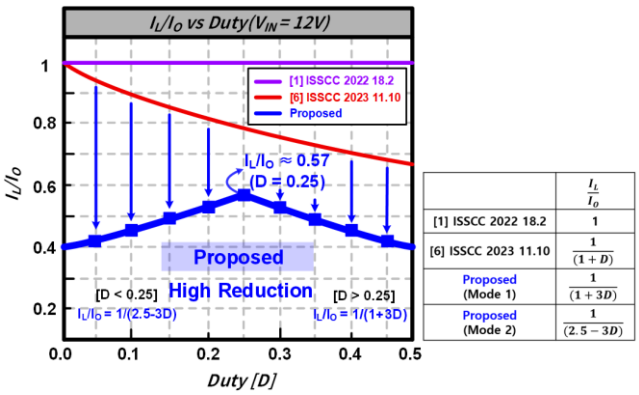
Fig. 6. V_{OUT} versus Duty Ratio.

Fig.6 shows the operating duty cycle range of the proposed converter for a 12V to 0.6-1V conversion. It can be observed that the converter operates near a duty ratio of 0.25 over the entire output voltage range. Since the intersection point of Mode 1 and Mode 2 occurs at D=0.25, the proposed mode-transition scheme enables the converter to always operate with the lower (I_L/I_O) ratio. Consequently, a reduced

inductor current is maintained throughout the operating range, allowing the use of smaller inductors and achieving higher power density.

C. Comparison

Fig.7 compares the normalized inductor current ratio (I_L/I_O) of the proposed converter with recently reported hybrid converters. In the conventional DSD converter, the entire output current is supplied by the inductors, resulting in I_L/I_O=1 regardless of the duty cycle. In ISSCC 2023 11.10, the flying capacitors partially contribute to load current delivery, reducing the required inductor current. However, the inductors still carry a significant portion of the output current over the entire operating range.



	$\frac{I_L}{I_O}$
[1] ISSCC 2022 18.2	1
[6] ISSCC 2023 11.10	$\frac{1}{(1+D)}$
Proposed (Mode 1)	$\frac{1}{(1+3D)}$
Proposed (Mode 2)	$\frac{1}{(2.5-3D)}$

Fig. 7. I_L/I_O Comparison with Prior Works.

In the proposed converter, the flying capacitor network supplies a significant portion of the output current, thereby reducing the required inductor current. Furthermore, the proposed mode-transition technique selects the operating mode with the minimum I_L/I_O ratio according to the duty cycle. As a result, the proposed converter achieves the lowest inductor current among the compared topologies, with a maximum I_L/I_O of approximately 0.57 and a minimum value of 0.4. This significantly reduces inductor current stress and DCR loss, relaxing the DCR requirement and enabling the use of smaller inductors, thereby improving power density.

III. CIRCUIT IMPLEMENTATION

Fig. 8 shows the overall architecture of the proposed converter. To provide gate-drive power for the high-voltage PMOS switch M_1 and NMOS switch M_2, dedicated on-chip voltage regulators are employed. The gate drivers for M_3 and M_4 are supplied directly from the VDD power domain.

For M_5-M_{12}, the gate-driver supply is generated using two methods: 1) regulated and clamped supplies derived from VDD power and 2) auxiliary capacitors charged during the $3V_O$ phases. As shown in Fig. 9, the stored voltage in the auxiliary capacitors is utilized to power the gate drivers.

The main controller consists of a Type-III compensation network, a ramp generator, and a mode selector. The Type-III compensator regulates the output voltage through PWM control, while the mode selector determines the operating mode according to the duty cycle. Specifically, the generated PWM signal V_{PWM} is compared with a reference pulse corresponding to D=0.25. When the duty cycle exceeds 0.25, Mode 1 is selected, otherwise, Mode 2 is activated.

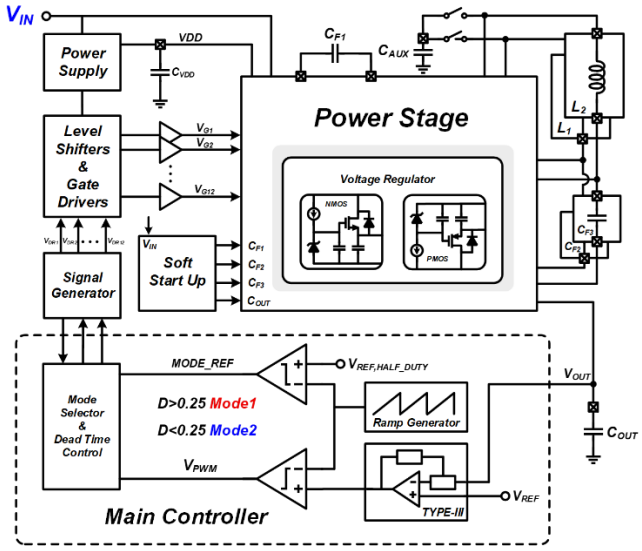


Fig. 8. Overall Architecture of the Proposed Converter.

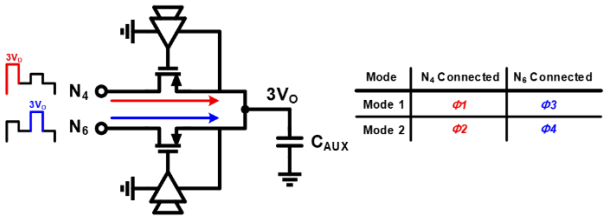


Fig. 9. Auxiliary Power Supply.

To ensure reliable start-up operation, a soft-start block is incorporated. Prior to normal operation, the flying capacitors and output capacitor are gradually pre-charged to their target voltages. As a result, excessive inrush current and unwanted transient behavior are suppressed, allowing stable converter start-up.

Soft Start Up Process

Fig.10 illustrates the proposed start-up sequence. During the first step, switch M_3 is turned on and a current mirror is utilized to charge C_{F1} to approximately $V_{IN}/2$. After C_{F1} reaches its target voltage, M_3 is turned off.

In the second step, switches M_5, M_7, M_8 and M_{10} are turned on. Since the steady-state voltages of C_{F2} and C_{F3} are equal to V_{OUT}, the output capacitor C_{OUT} is charged through the current mirror. As a result, C_{F2} and C_{F3} are charged to the same voltage as C_{OUT}. Meanwhile, C_{F1} is connected to C_{F2} through the inductors, causing its voltage to increase accordingly and establishing the required capacitor voltage distribution for normal operation.

Once the flying capacitors and output capacitor are pre-charged to their desired voltages, the start-up process is completed. The converter then begins normal operation upon assertion of the ENABLE signal.

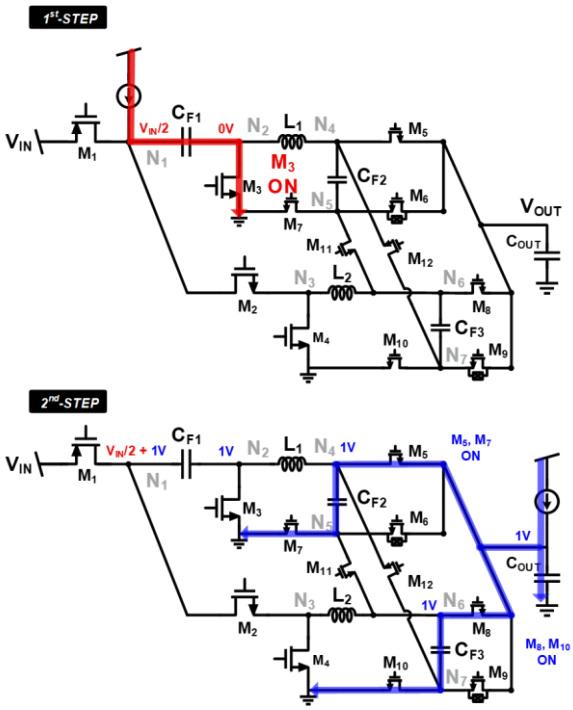


Fig. 10. Soft Start Up Process.

IV. SIMULATION RESULTS

Fig.11(a) shows the simulated steady-state waveforms of Mode 1 operation at V_{OUT} = 1V. Fig.11(b) shows the simulated steady-state waveforms of Mode 2 operation at V_{OUT} = 0.6V. The results verify the intended operation of the proposed converter in each mode.

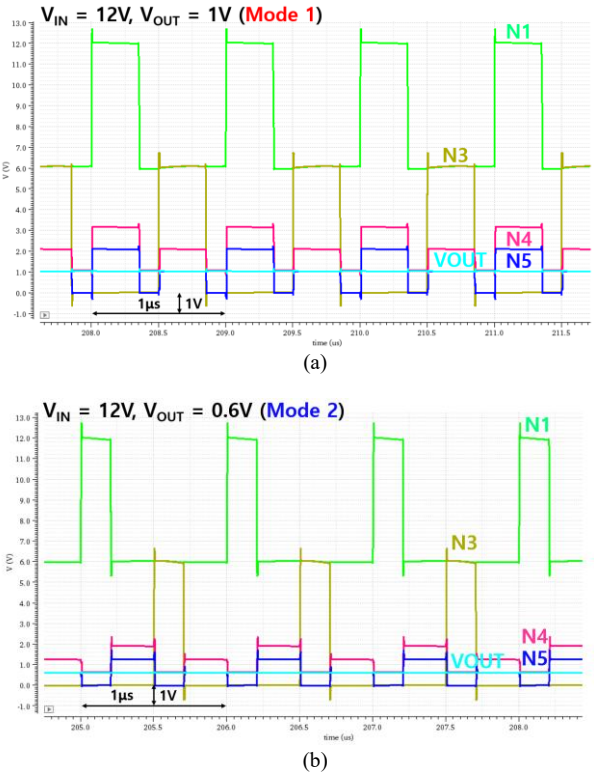


Fig. 11. Simulated Steady-State Waveforms for Each Mode. (a) Mode 1 (b) Mode 2

Fig. 12 shows the simulated load-transient response of the proposed converter. The load current is stepped from 1 A to 2.5 A with 1μs edge time.

Fig. 13 shows the simulated mode-transition waveforms of the proposed converter. As the target output voltage changes between 1 V and 0.6 V, the duty ratio crosses the mode-selection boundary of D=0.25, resulting in an automatic transition between the two operating modes. The left figure illustrates the transition from Mode 2 to Mode 1, while the right figure shows the transition from Mode 1 to Mode 2. During both transitions, the inductor currents I_{L1} and I_{L2} remain continuous without abrupt current discontinuities, demonstrating seamless mode transition.

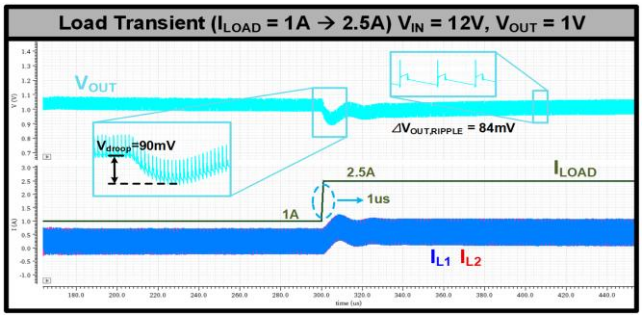


Fig. 12. Simulated Load Transient Response Waveforms.

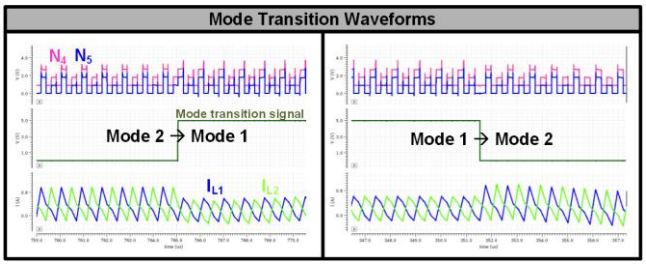


Fig. 13. Simulated Mode Transition Waveforms.

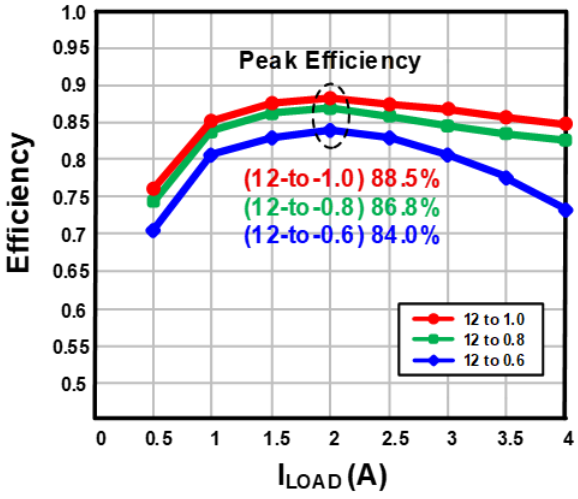


Fig. 14. Simulated Efficiency.

Fig. 14 shows the simulated power-conversion efficiency of the proposed converter for output voltages of 0.6 V, 0.8 V, and 1.0 V. The converter achieves peak efficiencies of 84.0%, 86.8%, and 88.5% at V_O = 0.6V, 0.8 V, and 1.0 V, respectively.

TABLE I. Performance Comparison to Prior Works

Design	ISSCC'22[1]	ISSCC'23[5]	ISSCC'23[6]	**This work**
Process	0.18μm	0.18μm	0.18μm	**0.13μm**
V_{IN} [V]	12/24	9-16	12	**12**
V_{OUT} [V]	1	0.6-1.6	1-1.8	**0.6-1.0**
F_{SW} (MHz)	1	1	1	**1**
Inductors (DCR[Ω])	1.8uH×2 (N.A)	680nH×1 (N.A)	1uH×2 (48m)	**1uH× 2 (60m)**
C_{FLY}	10uF×1	10uF×4	22uF×3	**1uF×1 22uF×2**
VCR	D/2	$\frac{D}{3+2D}$	$\frac{D}{2(1+D)}$	$\frac{\boldsymbol{D}}{\boldsymbol{2+6D}}/\frac{\boldsymbol{D}}{\boldsymbol{5-6D}}$
I_L/I_O	1	$\frac{3}{3+2D}$	$\frac{1}{(1+D)}$	$\frac{\boldsymbol{1}}{\boldsymbol{1+3D}}/\frac{\boldsymbol{1}}{\boldsymbol{2.5-3D}}$
Min. I_L/I_O	1	0.6	0.67	**0.4**
Peak η [%] (V_{IN}/V_{OUT})	83.5(24/1) 88.3(12/1)	94.5(12/1.2) 93.4(12/1) 90.5(12/0.6)	93.7(12/1.8) 92.3(12/1.5) 89(12/1)	**88.5(12/1) 86.8(12/0.8) 84.0(12/0.6)**

V. CONCLUSION

This paper presented a hybrid step-down DC-DC converter for direct 12V-to-0.6–1V conversion in data center power delivery applications. By combining a double step-down first stage, a switched-capacitor second stage, and a mode-transition scheme, the proposed converter achieves both voltage-stress reduction and significant inductor current reduction. The flying-capacitor network actively contributes to load current delivery, enabling reduced I_L/I_O ratio over the entire operating range through optimal mode selection. As a result, the proposed architecture allows the use of smaller inductors and low-voltage CMOS devices, leading to higher power density and reduced conduction loss. Simulation results demonstrate peak efficiencies of 88.5%, 86.8%, and 84.0% for 12V-to-1.0V, 0.8V, and 0.6V conversion, respectively. The proposed converter provides an effective solution for high-density and high-efficiency power delivery in next-generation data center systems.

ACKNOWLEDGMENT

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REFERENCES

[1] J. Yuan, Z. Liu, F. Wu and L. Cheng, "A 12V/24V-to-1V DSD Power Converter with 56mV Droop and 0.9us 1% Settling Time for a 3A/20ns Load Transient," *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2022, pp. 1-3.

[2] K. Wei, Y. Ramadass and D. B. Ma, "Direct 12V/24V-to-1V Tri-State Double Step-Down Power Converter with Online VCF Rebalancing and In-Situ Precharge Rate Regulation," in *IEEE Journal of Solid-State Circuits*, vol. 56, no. 8, pp. 2416-2426, Aug. 2021.

[3] C. Chen, J. Liu and H. Lee, "A 2.5-5MHz 87% Peak Efficiency 48V-to-1V Integrated Hybrid DC-DC Converter Adopting Ladder SC Network with Capacitor-Assisted Dual-Inductor Filtering," *2022 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2022, pp. 234-236.

[4] T. Hu, M. Huang, R. P. Martins and Y. Lu, "A 12-to-1 Flying Capacitor Cross-Connected Buck Converter with Inserted D > 0.5 Control for Fast Transient Response," in *IEEE Journal of Solid-State Circuits*, vol. 58, no. 11, pp. 3207-3218, Nov. 2023.

[5] X. Yang *et al.*, "11.8 A 5A 94.5% Peak Efficiency 9-16V-to-1V Dual-Path Series-Capacitor Converter with Full Duty Range and Low V.A Metric," *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2023, pp. 196-198.

[6] W. -L. Zeng *et al.*, "11.10 A 12V-Input 1V-1.8V-Output 93.7% Peak Efficiency Dual-Inductor Quad-Path Hybrid DC-DC Converter," *2023 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2023, pp. 10-12.

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Kunhee Cho received the B.S. and M.S. degrees in electrical and electronic engineering from Yonsei University, Seoul, South Korea, in 2007 and 2009, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Texas at Austin, Austin, TX, USA, in 2016.

From 2009 to 2012, he was with the Fairchild Semiconductor, Bucheon, South Korea, where he designed power management integrated circuits (ICs). In 2015 and 2016, he was a Graduate Research Intern with the Texas Instruments Incorporated, Dallas, TX, USA, in the low-power RF team. From 2017 to 2020, he was with Qualcomm Technologies Incorporated, Santa Clara, CA, USA, where he designed power management ICs for battery

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