A 40-Gb/s 0.78-pJ/bit PAM-4 Transceiver with Unterminated Signaling for Chiplet Interface in 28-nm CMOS

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Abstract - **In this paper, we propose a 40-Gb/s single-ended PAM-4 unterminated transmitter for chiplet interface in next-generation high-performance computing (HPC) and artificial intelligence (AI) accelerator systems. With recent advancements in heterogeneous integration, bandwidth density and energy efficiency have emerged as critical metrics for die-to-die (D2D) communications. While previous unterminated PAM-4 drivers required three voltage sources, using multiple supply rails increases design complexity and cost in practical implementations. To address this issue, the proposed transceiver implements an unterminated PAM-4 driver that achieves high data-rate and power efficiency using a single voltage source. To minimize the power consumption of PAM-4 signaling, the driver adopts an N-over-N architecture. In this paper, a simulation was performed using the on-chip channel. Designed using a 28-nm CMOS process, the transmitter achieves a power efficiency of 0.78 pJ/bit at 40 Gb/s and maintains a stable eye-opening even with a channel loss of -0.8 dB at the Nyquist frequency.**

Keywords—**Unterminated, PAM-4 signaling, Single-ended, Chiplet**

I. INTRODUCTION

To support higher performance, the die size of high-performance AI semiconductor chips has been increasing [1]. Consequently, the transition to chiplet-based architectures, which enhance design flexibility and optimize manufacturing costs, has become an inevitable choice for the continued growth of the semiconductor industry [2]. The chiplet architecture integrates dies with heterogeneous functions within a single package, offering increased system flexibility while reducing overall costs. In response to this trend, standard interface specifications, such as Universal Chiplet Interconnect Express (UCIe), have been established [3].

A critical requirement for chiplet interfaces is high bandwidth. The relatively low I/O speed, compared to modern computational power, creates a bottleneck that limits overall system performance. Therefore, achieving high bandwidth is essential to alleviate the "Memory Wall" effect. Another key characteristic is low power consumption. To achieve this, the UCIe specification optionally supports unterminated signaling, which forgoes conventional impedance matching.

While unterminated NRZ is the most basic scheme, it is inherently bandwidth limited because it can only transmit one bit per unit interval (UI) [4]. To overcome this, research is ongoing into unterminated PAM-3, PAM-4, capacitively driven, and simultaneous bi-directional (SBD) signaling [5]. Although unterminated PAM-3 offers improved bandwidth density over NRZ, its performance is limited compared to the superior data rate of PAM-4. Unterminated capacitively driven architectures can reduce power consumption by blocking static current but require passive components and additional blocks to manage DC floating issues [6]. Similar to PAM-4, simultaneous bi-directional (SBD) signaling achieves a data rate of twice the Nyquist frequency by facilitating simultaneous two-way communication over a single link [7]. However, the necessity of termination leads to significant power and area overhead [7]. In contrast, unterminated PAM-4 signaling achieves twice the data rate of NRZ at the same Nyquist frequency while maintaining low power. Recently, a PAM-4 method utilizing three voltage sources (VDDH, VDDM, and VDDL) was proposed to reduce static current [8]. However, using multiple voltage sources increases design complexity and integration costs.

To address these challenges, this paper proposes an unterminated PAM-4 driver that operates from a single voltage source. To minimize static power dissipation, the proposed transmitter employs a distinct operational approach compared to conventional voltage-mode (VM) drivers, utilizing an N-over-N architecture to effectively reduce overall power consumption. Additionally, considering design complexity and implementation costs, the driver is designed to operate from a single voltage source. The remainder of this paper is organized as follows. Section II introduces the architecture and operation of both the conventional VM-driver and the proposed driver. Section III details the circuit design and implementation of the low-power PAM-4 unterminated transmitter in a 28-nm CMOS process. Section IV presents simulation results verifying the signal integrity and energy efficiency, along with a comparative analysis. Finally, Section V concludes the paper.

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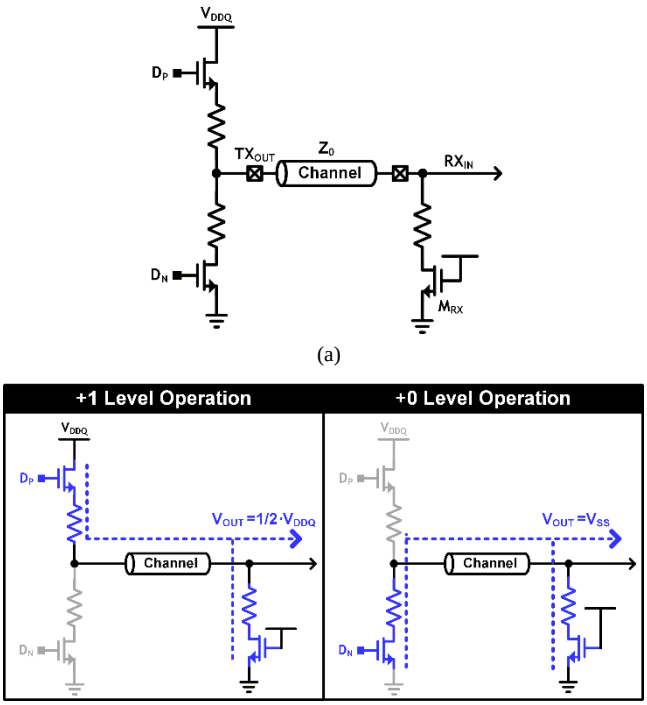


Fig. 1 Conventional VM-NRZ driver of (a) architecture and (b) operation

II. UNTERMINATED PAM-4 DRIVER

Fig. 1(a) shows the architecture of a conventional terminated NRZ VM driver. Conventional terminated VM drivers are typically composed of passive resistors and MOSFETs. In this configuration, the TX driver utilizes resistors and MOSFETs, and the receiver-side termination is assumed to have a structure identical to that of the TX pull-down network. Fig. 1(b) shows the operation of this conventional terminated NRZ VM driver. During the +1 level operation, D_P is high, which activates the pull-up (PU) NMOS. Simultaneously, the termination NMOS, located between the channel and the RX input, remains active. Consequently, the supply voltage (VDDQ) passes through the PU path, including the NMOS and a passive resistor, and the signal is passed to the channel via voltage division with the termination NMOS. During the +0 level operation, D_N is high, which activates the pull-down (PD) NMOS. Identical to +1 level operation, the termination NMOS remains active. In this state, the voltage at the output node is pulled down to the ground through the PD path and the termination NMOS [9].

Fig. 2(a) shows the architecture of a conventional terminated PAM-4 VM driver. Same as terminated NRZ VM, to ensure consistent impedance matching across all four PAM-4 levels, the driver is constrained by the requirement that the total number of active MOSFET segments must remain constant to provide a stable output impedance. Fig. 2(b) shows the operation of the conventional terminated PAM-4 VM driver. The +3 level and +0 level operations of the NRZ VM driver, with the termination NMOS always on. During +2 level operation MSB_P, LSB_N are high, activating the MSB PU NMOS and LSB PD NMOS. The V_{OUT} level of

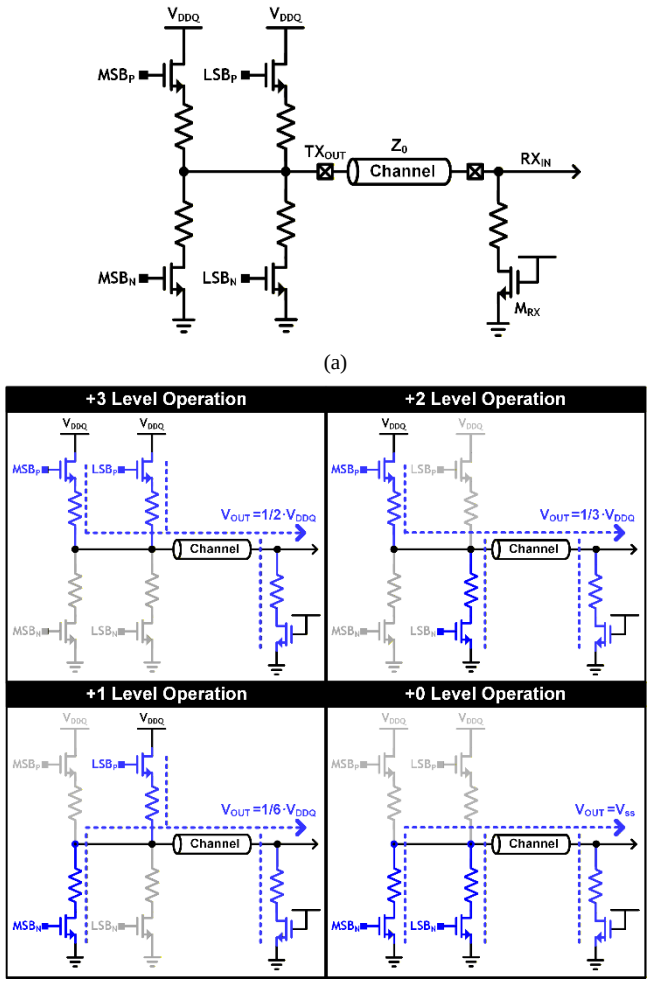
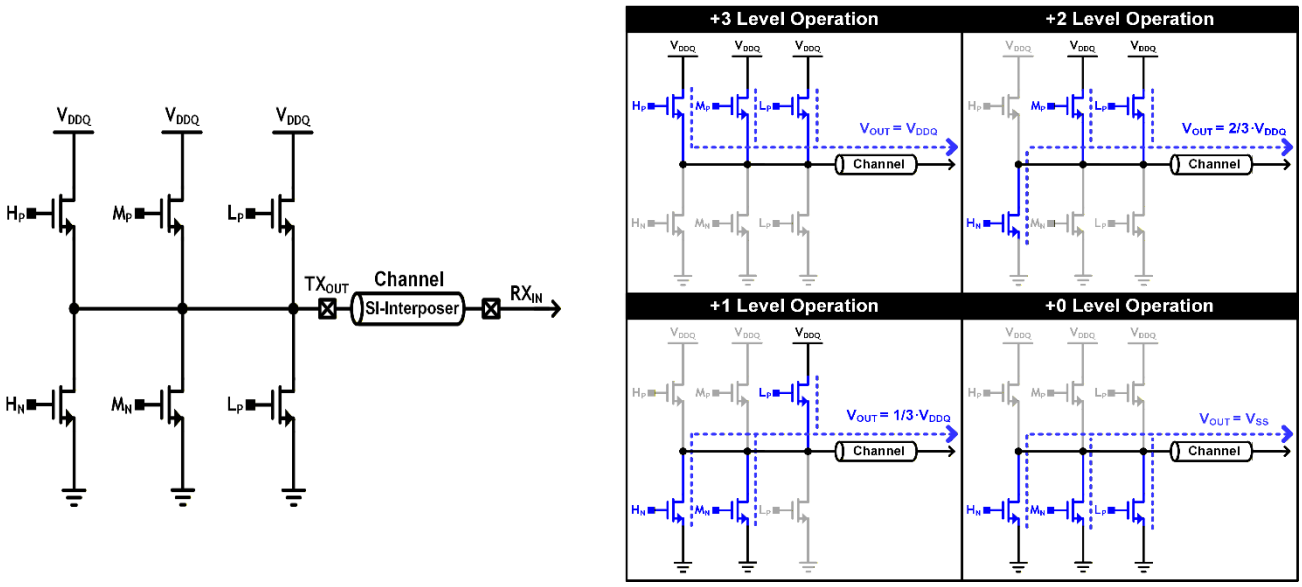


Fig. 2 Conventional VM-PAM-4 driver of (a) architecture and (b) operation

1/3 VDDQ is achieved through voltage division among the MSB PU path, the LSB PD path and the termination NMOS. Conversely, for +1 level operation, the MSB PD NMOS and the LSB PU NMOS are enabled, reversing the switching states of the +2 level [9].

Since conventional terminated drivers are unsuitable for chiplet interface due to their significant power and area overhead, this paper proposes an unterminated PAM-4 architecture to achieve high bandwidth with low power consumption. Fig. 3(a) shows the architecture of the proposed unterminated PAM-4 driver. The four PAM-4 levels are implemented exclusively using NMOS transistors operating in the triode region, eliminating the need for external termination. In an unterminated environment, impedance matching is not required; thus, there is no need to maintain a constant number of active MOSFETs for each level. Fig. 3(b) shows the operation of the proposed unterminated PAM-4 driver. For +3 level operation, the H_P, M_P and L_P NMOS devices are turned on, allowing V_{DDQ} to pass through each path. As a result, V_{OUT} achieves a full-swing level of V_{DDQ}. In +2 level operation, the H_N, M_P and L_P NMOS are activated, making V_{OUT} of 2/3 V_{DDQ}. Similarly, for +1 level, the H_N, M_N and L_P NMOS are activated to achieve a V_{OUT} of 1/3 V_{DDQ}. Finally, at the +0



(a) (b)

Fig. 3 Proposed unterminated VM PAM-4 driver of (a) architecture and (b) operation

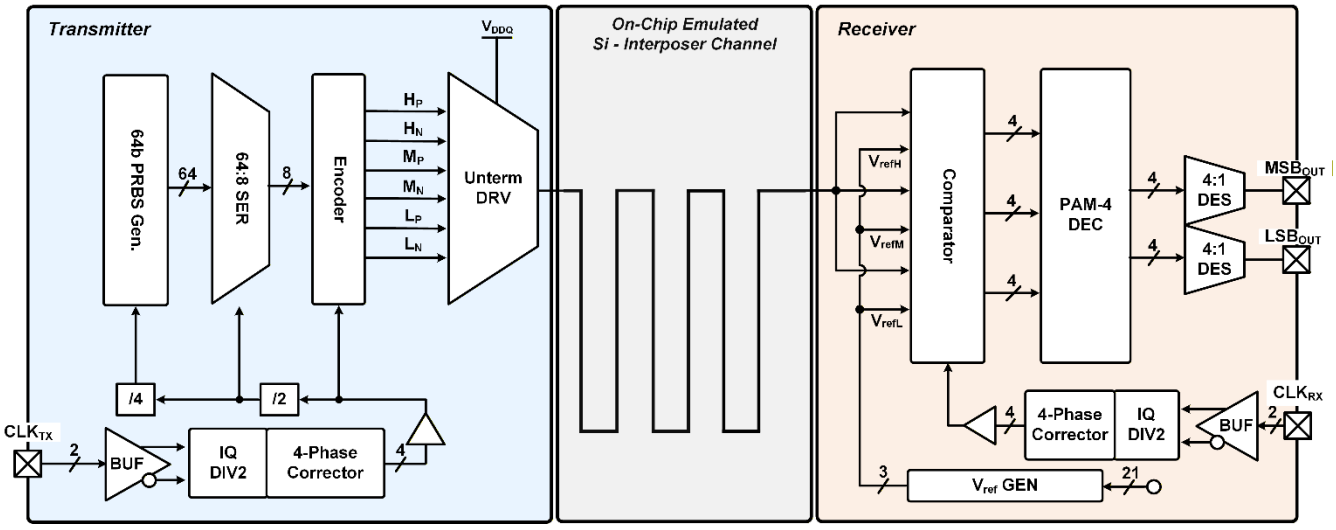


Fig. 4 TOP architecture

level, the H_N, M_N and L_N NMOS are enabled, pulling V_{OUT} down to V_{SS}. This unterminated driver achieves high efficiency in terms of both area and power consumption.

III. CIRCUIT IMPLEMENTATION

A. TOP Architecture

Fig. 4 shows the TOP architecture of the transceiver used in this paper. The TX data path consists of a 64-bit Pseudo-random binary sequence (PRBS) generator, a 64:8 serializer, a PAM-4 encoder, and an unterminated driver. The RX data path consists of comparators, a PAM-4 decoder, and a deserializer. Both the transmitter and receiver receive an external differential clock, convert it to a quarter-rate clock through an IQ DIV2, 4-phase corrector distributes quarter-rate clock to each circuit. The input data required for operation is generated through the PRBS. The 64-bit parallel data generated by the PRBS is serialized to 8 bits through a 64:8 serializer. It is then fed into the channel through the encoder and driver. The data input to the receiver passes through a quarter-rate comparator and is then decoded into an NRZ signal by a PAM-4 decoder. Finally, it is output through a 1:4 deserializer.

B. Encoder and Pre-driver

Fig. 5 shows the structure of the PAM-4 encoder and the pre-driver. The PAM-4 encoder acts as a signal generator, while the pre-driver functions as both a signal data buffer and a signal distributor. The 8-bit data output from the serializer is processed by the PAM-4 encoder to generate multi-level signaling components required for the output stage. Specifically, the encoder transforms the 8-bit input into a 12-bit encoded stream (4 bits each for high, mid and low signals) through distinct logic paths: the H-signals are generated by applying a 2-input AND gate operation to the 8-bit data. This logic reduces the initial data to a 4-bit output, specifically designed to trigger the upper voltage levels of the PAM-4 signal. Conversely, the L-signals are formed

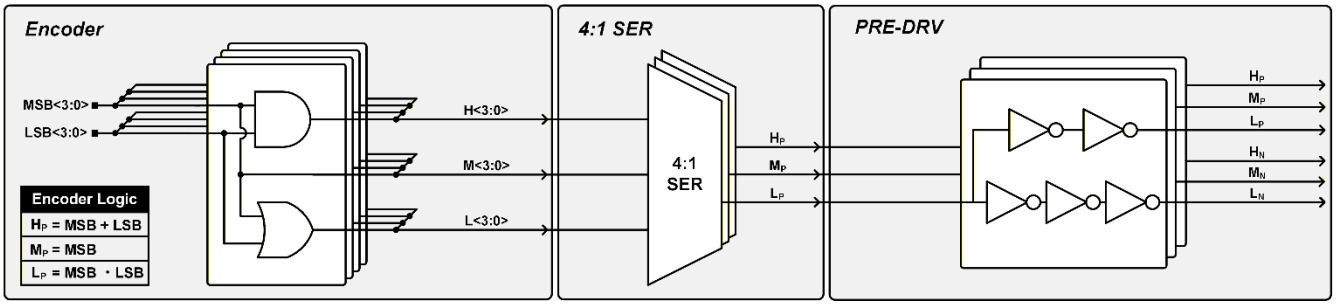


Fig. 5 Encoder and pre-driver architecture

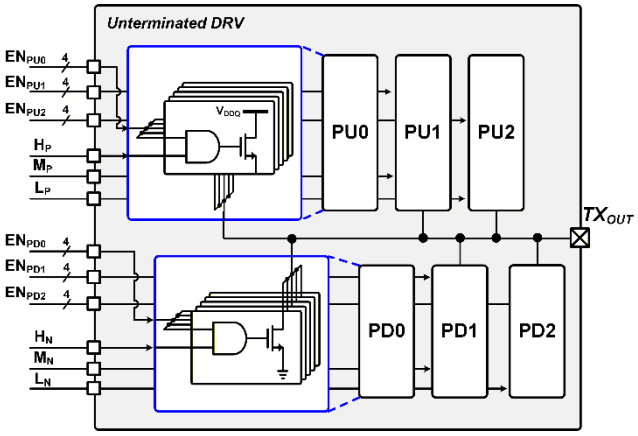


Fig. 6 Proposed unterminated PAM-4 driver architecture

through a 2-input OR gate operation on the 8-bit data. This 4-bit output ensures the appropriate transitions for the lower voltage levels. The M-signals path is implemented using single-input buffers consisting of inverters. While the H-path and L-path use 2-input gates to process 8 bits into 4 bits, the M-path actively buffers 4 bits of the input data. To ensure that the M-path maintains the same electrical characteristics as the other paths, the remaining 4 unused bits are terminated with dummy inverters. These dummy inverters provide a matched capacitive load that perfectly replicates the input impedance of the active buffers. This meticulous load-matching ensures that the propagation delay of the M-path is synchronized with the H-path and L-path, thereby minimizing timing skew and deterministic jitter prior to the 4:1 serializer [9], [10]. Following the encoder stage, the resulting 12-bit parallel data is fed into a 4:1 serializer, which multiplexes the encoded bits to generate a data stream operating at 40-Gb/s. This serialized data is then delivered to the pre-driver. The pre-driver not only provides the necessary driving current but also functions as a differential signal generator, producing precise complementary pairs (H_P/H_N, M_P/M_N, L_P/L_N) for the complementary switching of the output stage.

C. Proposed Unterminated PAM-4 Driver

Fig. 6 illustrates the detailed structure of the proposed unterminated PAM-4 driver. The output stage utilizes a segmented architecture consisting of three pull-up segments (PU0, PU1, PU2) and three pull-down segments (PD0, PD1, PD2). Each segment is independently controlled by an AND gate that processes the data signal (H_P/H_N, M_P/M_N, L_P/L_N)

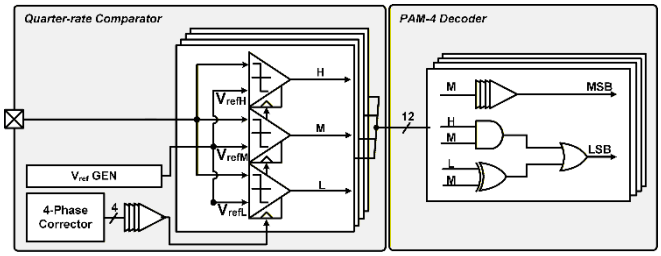


Fig. 7 Comparators and decoder architecture

TABLE I. PAM-4 Driver Operation Comparison

	Control Signals	Active PU & PD	Resistance Ratio	Output Voltage
+3	H_P, M_P, L_P	3 & 0	1	VDDQ
+2	H_N, M_P, L_P	2 & 1	2/3	2/3·VDDQ
+1	H_N, M_N, L_P	1 & 2	1/3	1/3·VDDQ
+0	H_N, M_N, L_N	0 & 3	0	VSS

and corresponding enable signal (EN_{PU0-3}, EN_{PD0-3}). This configuration allows the driver to selectively activate specific segments to define the output voltage levels. By independently scaling the number of active units for each PAM-4 symbol, the driver optimizes the resistance ratio to achieve precise voltage levels while minimizing unnecessary current flow. Unlike conventional voltage-mode drivers that often maintain a constant output impedance, this flexible segmented approach prioritizes both level accuracy and power efficiency. Table I illustrates the resistance ratios and output levels determined by the pull-up/pull-down ratio at each PAM-4 symbol. In this design, a low supply voltage of V_{DDQ} = 0.4 V is employed to implement low-voltage swing terminated logic (LVSTL). By adopting this reduced V_{DDQ}, the driver significantly limits the voltage swing at the output node, which directly leads to a substantial reduction in dynamic power consumption. The combination of a 0.4 V low-voltage swing and the unterminated architecture allows the proposed driver to achieve superior energy efficiency while maintaining the signal integrity required for high-speed PAM-4 transmission.

D. Receiver

The chiplet interface is characterized by low insertion loss (IL) due to the ultra-short-reach (USR) silicon interposer with transmission distances limited to a few millimeters. In this environment, conventional equalization blocks such as FFE, DFE, and CTLE are often redundant due to the inherently low IL [5], [7], [11]. Furthermore, their inclusion

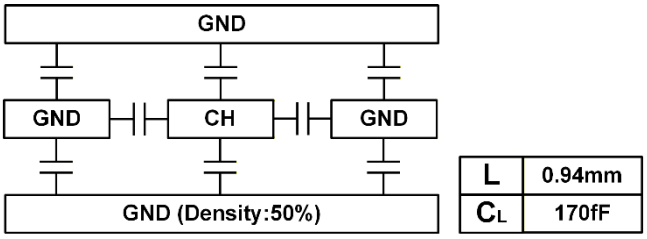


Fig. 8 On-chip channel architecture

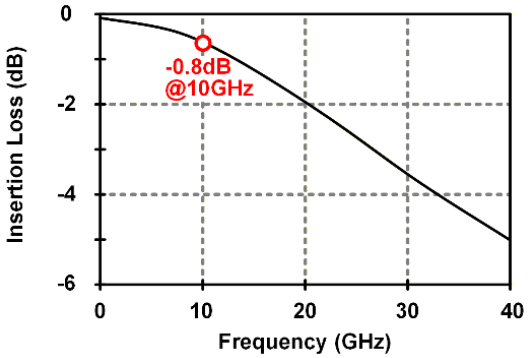
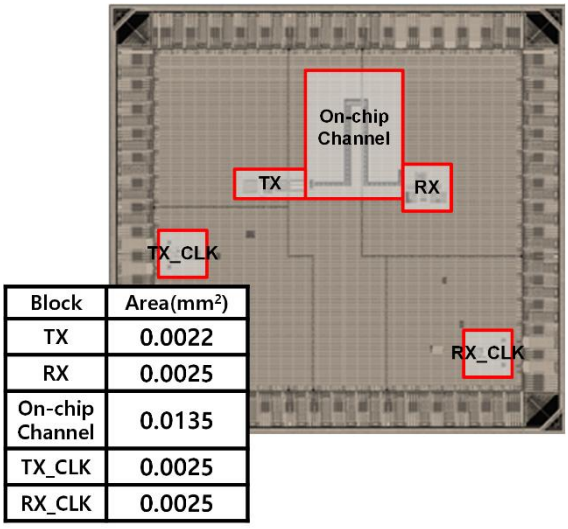


Fig. 9 Channel response



Block	Area(mm²)
TX	0.0022
RX	0.0025
On-chip Channel	0.0135
TX_CLK	0.0025
RX_CLK	0.0025

Fig. 10 Chip layout

would incur significant power and area overhead. Therefore, the proposed transceiver is implemented without an equalizer to maximize energy efficiency [12].

Fig. 7 shows the structure of the quarter-rate comparator and the PAM-4 decoder. The comparator operates at a quarter-rate. Similar to the transmitter, an external differential clock is processed through an IQ DIV2 and a 4-phase corrector to generate the required quarter-rate clock phases. The comparator outputs are delivered to a decoder that converts the PAM-4 signal back into NRZ data, which is then output through a 1:4 deserializer.

E. On-chip Channel

Fig. 8 shows the on-chip channel configuration used in this paper. To ensure high-density signaling, the channel is designed with a pitch of 4 um and a total length of 0.94-mm.

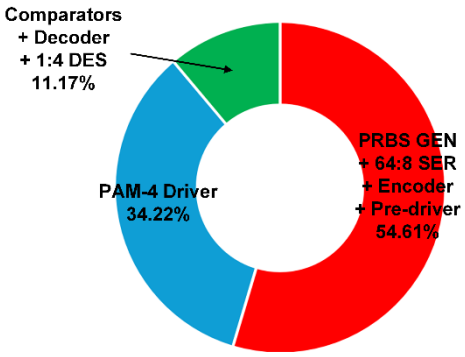
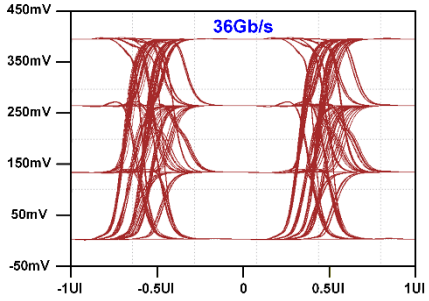
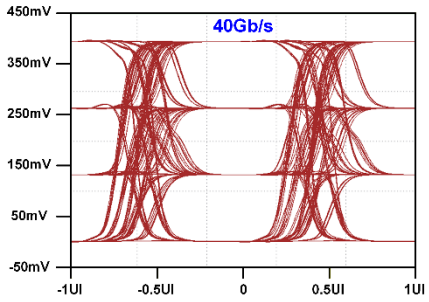


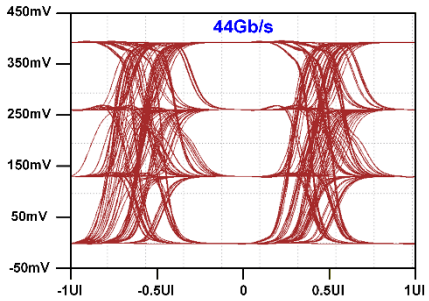
Fig. 11 Power consumption at 40-Gb/s



(a)



(b)



(c)

Fig. 12 Eye diagram at (a) 36Gb/s, (b) 40Gb/s and (c) 44Gb/s

The physical attributes were carefully determined to achieve the target characteristic impedance while ensuring high-speed signal propagation. The electrical characteristics of the proposed channel are presented in Fig. 9. The channel has an insertion loss of less than 1 dB at 10 GHz [13].

IV. SIMULATION RESULTS

Fig. 10 shows the layout of a chiplet PAM-4 Transceiver fabricated in a 28-nm CMOS process. The transceiver is

TABLE II. Performance Summary and Comparison Table

	This work	[6]	[8]	[14]
Technology (nm)	28	28	28	16
Supply Voltage (V)	1/0.4	1	0.95/0.45 /0.3/0.15	1.1
Signaling	PAM-4	PAM-4	PAM-4	[a] CNRZ-5
Driver Type	VM	Capacitively-driven	VM	VM
Data Rate (Gb/s)	*40	24	**16	20.83
Power Efficiency (pJ/bit)	*0.78	0.458	**0.053	[b] 1.02

*: Post-layout simulation result, **: Pre-layout simulation result
[a]: Correlated NRZ, [b]: Include clock path

connected using the on-chip channel of the 0.94 mm chip.

Fig. 11 shows the power consumption graph of the chip proposed in this paper. Excluding the driver, TX consumes 16.94 mW, RX consumes 3.47 mW, and the unterminated driver consumes 10.61 mW at 40 Gb/s. Consequently, the total power consumption is 31.02 mW.

Fig. 12(a), (b) and (c) shows the eye diagram at 36 Gb/s, 40 Gb/s and 44 Gb/s. The eye diagram at 40 Gb/s exhibits an eye height of 132mV and an eye width of 0.64 UI.

Table II summarizes the performance of the proposed chiplet-PAM4 transceiver and compares it with other recent works on D2D and similar interfaces. The proposed transceiver achieves a data rate of 40 Gb/s and a power efficiency of 0.78 pJ/bit with an unterminated PAM-4 driver.

V. CONCLUSION

In this article, we propose a single-ended, low-power PAM-4 VM-driver for a high-speed chiplet interface. The proposed TRX operates at V_{DDA} = 1 V, V_{DDQ} = 0.4 V utilizing PAM-4 signaling. By achieving energy efficiency of 0.78 pJ/bit at 40 Gb/s through an unterminated and N-over-N architecture, we demonstrate its applicability to next-generation chiplet systems.

ACKNOWLEDGMENT

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REFERENCES

[1] J. Choquette, “NVIDIA Hopper H100 GPU: Scaling performance”, *IEEE Micro*, vol. 43, no. 3, pp. 9–17, May-Jun. 2023.

[2] S. Naffziger, K. Lepak, M. Paraschou, and M. Subramony, “2.2 AMD chiplet architecture for high-performance server and desktop products,” in *2020 IEEE International Solid-State Circuits Conference (ISSCC)*, San Francisco, CA, USA, 2020, pp. 44–45.

[3] "Universal Chiplet Interconnect Express (UCIe) Specification Rev 1.1," in *UCIe Consortium*, 2023. [Online]. Available: https://www.ucieexpress.org/

[4] X. Zheng et al., "A 4–40 Gb/s PAM4 transmitter with output linearity optimization in 65 nm CMOS," in *2017 IEEE Custom Integrated Circuits Conference (CICC)*, Austin, TX, 2017, pp. 1-4.

[5] Y. Nishi et al., “A 0.190-pJ/bit 25.2-Gb/s/wire inverter-based AC-coupled transceiver for short-reach die-to-die interfaces in 5-nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 59, no. 4, pp. 1146–1157, Apr. 2024.

[6] S. Kim et al., “A 0.458-pJ/bit 24-Gb/s/pin capacitively driven PAM4 transceiver with PAM-based crosstalk cancellation for high-density die-to-die interfaces,” *IEEE J. Solid-State Circuits*, vol. 59, no. 11, pp. 3730–3740, Nov. 2024.

[7] Y. Nishi et al., ‘‘A 0.297-pJ/bit 50.4-Gb/s/wire inverter-based short-reach simultaneous bidirectional transceiver for die-to-die interface in 5-nm CMOS,’’ IEEE J. Solid-State Circuits, vol. 58, no. 4, pp. 1062–1073, Apr. 2023.

[8] J. You et al., "Design and Analysis of Static-Free PAM-4 Transmitter for HBM TSV Interface," in *2025 International Conference on Electronics, Information, and Communication (ICEIC)*, Osaka, Japan, 2025, pp. 1-4.

[9] Y.-U. Jeong et al., “A 0.64-pJ/bit 28-Gb/s/pin high-linearity single-ended PAM-4 transmitter with an impedance-matched driver and three-point ZQ calibration for memory interface,” *IEEE J. Solid-State Circuits*, vol. 56, no. 4, pp. 1278–1287, Apr. 2021.

[10] J.-Y. Kim, J. Lee, K. Kim et al., “A 5 Gb/s time-interleaved voltage-mode duobinary encoding scheme for 3-D-stacked IC,” *IEEE J. Solid-State Circuits*, vol. 57, no. 6, pp. 1913–1923, Jun. 2022.

[11] S. Chen et al., “A 50Gb/s CMOS optical receiver with si-photonics PD for high-speed low-latency chiplet I/O,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 11, pp. 4271–4282, Nov. 2023.

[12] H. Park, Y.-U. Jeong, and S. Kim, ‘‘A 24-Gb/s/pin single-ended PAM-4 receiver with 1-tap decision feedback equalizer using inverter-based summer for memory interfaces,’’ *IEEE Access*, vol. 10, pp. 91888–91896, 2022.

[13] Y. Kwon et al., “A 33-Gb/s/pin 1.09-pJ/bit single-ended PAM-3 transceiver with ground-referenced signaling and time-domain decision technique for multi-chip module memory interfaces,” *IEEE J. Solid-State Circuits*, vol. 58, no. 8, pp. 2314–2325, Aug. 2023.

[14] A. Tajalli et al., “A 1.02-pJ/b 20.83-Gb/s/wire USR transceiver using CNRZ-5 in 16-nm FinFET,” *IEEE J. Solid-State Circuits*, vol. 55, no. 4, pp. 1108–1123, Apr. 2020.

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