Compact Noise and Linearity Model of a Dynamic Amplifier for Behavioral ADC Modeling

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***Abstract* – This paper introduces the behavioral model of dynamic amplifier which is designed in 28nm CMOS process. First, the gain of the dynamic amplifier is analyzed from various perspectives, such as input common mode voltage, input differential mode voltage and pulse width. Next, the method that is to implement the gain value non-linearity model of the amplifier and the noise model through SPICE simulations is described in detail. The gain model including nonlinearity exhibits –6.7%～5.4% of modeling error rate and the noise model shows –11.2%～13.5% of modeling error rate. The proposed model in this paper is applied to the 1.1Gs/s 7-bit pipelined ADC design verification to confirm the reliability. In addition, design efficiency of the proposed behavioral model is described.**

***Keywords*—Behavioral Modeling, Dynamic Amplifier, Pipelined SAR ADC.**

I. INTRODUCTION

Dynamic Amplifier is widely used in low power and high-speed ADC design because it can quickly amplify voltage in discrete-time with low power [1,2]. Specifically, it is used to implement a residue amplifier between stages of a high-speed pipelined SAR A/D converter [3] or it is also used in the implementation of the feedback path amplifier in noise-shaping SAR ADC [4]. Traditionally, the ADC design uses an opamp based closed-loop amplifier [5] for high-precision amplification. In this case, it has a good characteristic that the gain of the amplifier is insensitive to changes in PVT(Process Voltage Temperature). On the other hand, traditional closed-loop amplifiers cannot take advantage of process refinement and it is difficult to design large gain opamp at low supply voltages. For this reason, techniques which apply a method of correcting the gain in a different way to a high-speed ADC using dynamic amplifier is attracting lots of attention these days.

Dynamic amplifiers operate quickly and consume very little static current, so they consume very low power. However, since the voltage gain varies with variables such as common input voltage, differential input voltage and pulse width, it exhibits a nonlinearity different from that of traditional amplifier designs, so design verification must be performed more carefully.

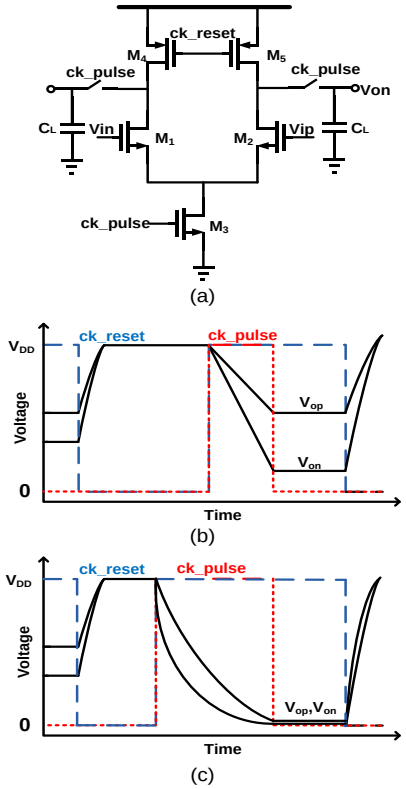

Fig. 1 Operation of dynamic amplifier (a)Architecture of dynamic amplifier (b)Operation waveform of dynamic amplifier (c)Operation waveform of dynamic amplifier (In case the pulse width is too wide)

For example, if a dynamic amplifier is used in applications such as the residue amplifier of a Pipelined SAR ADC, it is necessary to verify the performance of the SNDR or effective resolution (Effective Number of Bits, ENOB) of ADC through comprehensive simulations in addition to the operating range of a dynamic amplifier. In this paper, assuming that it is applied as a residue amplifier of a pipelined SAR ADC, we preset the range of input common mode voltage for the amplifier from 480mV to 540mV. When the peak-to-peak voltage of the ADC is 300mV and the resolution of the first stage is 3-bit, a maximum of 75mV can be input differentially, the range was set as a reference. At this time, if the target system has a large complexity, it can be a heavy design burden to do lots of SPICE simulations required for verification of a dynamic amplifier. Therefore,

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in this paper, we implemented the behavioral model that considers noise and nonlinearity of a dynamic amplifier and verified its reliability by comparing it with SPICE simulation.

The behavioral model proposed in this paper has a gain error rate from - 6.7% to + 5.4% compared to SPICE simulation which makes it possible to predict nonlinearity in the range of input common mode 480-540 [mV], the differential-mode range of 1-80 [mV], and the pulse width of 44ps to 54ps. In the input common-mode range of 480-530[mV], the differential-mode range of 10-80[mV], and the pulse width of 48ps~56ps, the error rate of the noise model was -11.2%~13.5%. The behavioral model using the proposed technique is later used for dynamic amplifier modeling in simulation systems such as Verilog-A, CppSim [6], X-model [7], etc., and can be helpfully used for quick design verification.

This paper is organized as follows. In section II, the basic concept and non-ideal operation of dynamic amplifier is introduced. In particular, the common-mode voltage variance, input differential mode voltage, and the change of gain by noise are discussed. The nonlinearity of the dynamic amplifier designed with 28nm CMOS process is explained and the method of noise model implementation is also described in section III. The reliability of the proposed model is confirmed and the comparisons with operation speed are presented in section IV. Conclusions are given in section V.

II. DYNAMIC AMPLIFIER OPERATION AND NON-IDEALITY

A. operation of dynamic amplifier

Fig. 1.(a) is the most basic form of a NMOS-based dynamic amplifier [8]. It operates by two phases in ck_reset and ck_pulse, and the operation waveform is shown in Fig. 1.(b). When ck_reset is 0, both the differential outputs Vop and Von are reset to VDD. When ck_pulse becomes VDD, a differential current proportional voltage of the input discharges the charge on the output node and makes output voltages as

$$V_{op} \approx V_{DD} - \frac{I_{D0} - \frac{g_m}{2}\Delta V_{in}}{C_L} T_P \quad (1)$$

$$V_{on} \approx V_{DD} - \frac{I_{D0} + \frac{g_m}{2}\Delta V_{in}}{C_L} T_P \quad (2)$$

T_P is the operation time of ck_pulse, C_L is the total capacitance of the output node, I_{D0} is the total current flowing through M3, and ΔV_{in} is the difference between the differential input V_{ip} and V_{in}. Thus, the differential gain is defined as

$$A_{diff} = \frac{V_{op} - V_{on}}{V_{ip} - V_{in}} \approx \frac{g_m}{C_L} T_P \quad (3)$$

Therefore, the differential gain of the dynamic amplifier is determined by the transconductance (g_m) and the time (T_P) that the ck_pulse operates. However, the ideal gain A_{diff} of a dynamic amplifier deviates from the ideal value due to various factors and have nonlinearity.

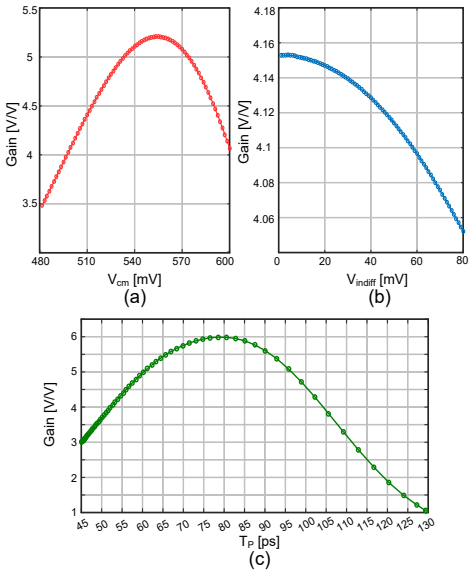

Fig. 2. The gain dependency of dynamic amplifier (a) on input common mode voltage, (b) on differential input voltage, (c) on clock pulse width.

In order to find out the components that affect the gain of the dynamic amplifier which is designed in the process of 28nm CMOS shown in Fig. 1.(a). The ck_pulse is amplified for 50ps and the gain is around 4 [V/V] when C_L is 35fF. M1, M2, M3 are sized as 10u/0.03u and 2u/0.03u for M4 and M5 respectively.

B. Impact of the input common mode voltage

Since dynamic amplifiers are not biased with current, the change of input commode voltage almost induces a change in Vgs of the input transistor. When the input transistor operates in saturation mode, the transconductance is

$$g_m = \mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{th}) \quad (4)$$

Thus, as the common mode voltage increases, the gain proportionally goes higher due to the increased g_m. However, if the common mode voltage is too high, input transistors (M1 and M2 in Fig. 1.(a)) enter the triode region so that g_m decreases, resulting in lower gain. These characteristics are verified through the simulation, and the gain has a maximum at a specific common mode voltage as shown in Fig. 2.(a).

C. Impact of differential input voltage

The voltage at the output node of the dynamic amplifier is expressed as

$$V_{op} \approx V_{DD} - \frac{I_{DN}}{C_L} T_P, V_{on} \approx V_{DD} - \frac{I_{DP}}{C_L} T_P \quad (5)$$

$$A_{diff} = \frac{V_{op} - V_{on}}{V_{ip} - V_{in}} \approx \frac{I_{DP} - I_{DN}}{C_L(V_{ip} - V_{in})} T_P \quad (6)$$

in terms of current. I_{DP} and I_{DN} are current flowing through M1 and M2 respectively in Fig. 1.(a). Without using small-signal model, difference between I_{DP} and I_{DN} is

$$I_{DP} - I_{DN} = \sqrt{\mu_n C_{ox} \frac{W}{L} I_D}(V_{ip} - V_{in})\sqrt{1 - \frac{\mu_n C_{ox} \frac{W}{L}}{4I_D}(V_{ip} - V_{in})^2} \quad (7)$$

Thus, considering (6) and (7), differential gain is represented as

$$A_{diff} = \frac{\sqrt{\mu_n C_{ox} \frac{W}{L} I_D}\sqrt{1 - \frac{\mu_n C_{ox} \frac{W}{L}}{4I_D}(V_{ip} - V_{in})^2}}{C_L} T_P \quad (8)$$

The equation (8) explains the fact that the differential gain decreases as the difference between $V_{ip} - V_{in}$ increases. It is verified by the simulation as shown in Fig. 2.(b). This compressive characteristic leads to nonlinearity operation of a dynamic amplifier.

D. Impact of pulse width

The width of ck_pulse in Fig. 1.(a) is an important factor which determines the gain of a dynamic amplifier. This is because, in the case of a dynamic amplifier, the current flow time (TP) is determined by the width of ck_pulse and the gain changes accordingly. In general, the wider the pulse width, the longer the current flows, increasing the gain of the dynamic amplifier. However, the increase of the pulse width and gain does not show completely linear since the current does not flow fixedly. Fig. 2.(c) represents the relationship between the pulse width and the gain of the dynamic amplifier and it shows nonlinearity increase. Note that when using a dynamic amplifier, if the pulse width is too wide, the output voltage significantly decreases. Thus, the drain voltage of M3 in Fig. 1.(a) and the source voltage of M1, M2 become almost the same so that the gain of the amplifier approaches 0 as shown in Fig. 1.(a). Therefore, the proposed modeling also has a gain similar to that of an actual circuit only with a pulse width within a limited range.

E. Impact of noise

The noise equation of dynamic amplifier is represented as

$$\Delta V_{output} = A(\Delta V_{input} + V_{noise}) \quad (9)$$

where $A\Delta V_{input}$ is ΔV_{output} without noise so that input referred noise can be estimated. In case of a constant current flowing amplifier, the power density of the input referred noise is simply

$$\overline{V_n^2} = \frac{4kT\gamma}{g_m} [V^2/Hz] \quad (10)$$

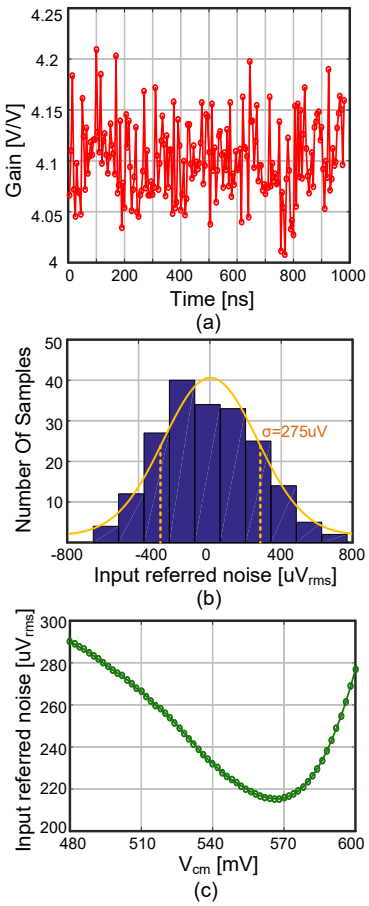

Fig. 3. (a) Noise time domain simulation, (b) on differential input voltage, (c) on clock pulse width.

However, in case of a dynamic amplifier, since the g_m changes during the amplification time, the magnitude of the input referred noise is not constant. The correlation between the gain of the amplifier and the magnitude of the input noise is similar to that of the conventional amplifier. This is because when g_m increases and the gain increases linearly, since the magnitude of the current noise at the output increases in proportion to the $\sqrt{g_m}$, the magnitude of the input referred noise decreases as the amplifier gain increases. Fig. 3. shows the results of verifying this correlation by the transient SPICE simulation. Fig. 3.(a) is the result of time domain noise simulation using SPICE, and it shows that the gain of the amplifier is distributed around a specific average value due to the influence of noise. Fig. 3.(b) is a histogram of the magnitude of the input referred noise using the gain distribution. These values correspond to the distribution of the sampled values after the noise current is integrated into the output capacitor during the amplifying time and assuming a Gaussian distribution, the standard deviation is $\sigma = 275\mu V$, which corresponds to the rms value of input referred noise. Fig. 3.(c) represents the relationship between input common mode V_{cm} and input referred noise and verifies tendency that the magnitude of the input referred noise changes due to the inverse relationship with the trend of the gain in Fig. 2.(a).

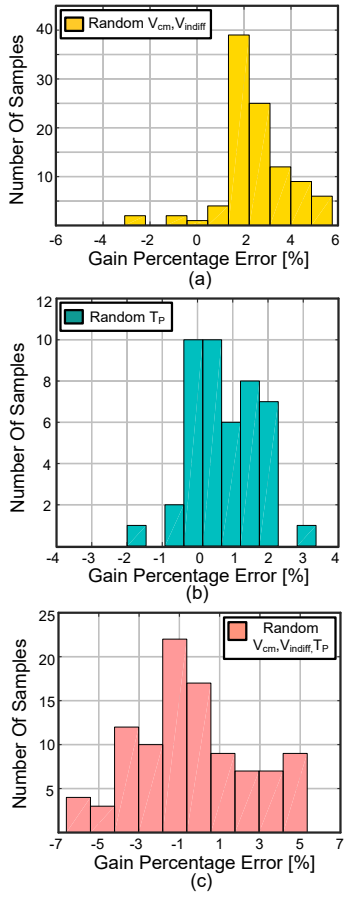

Fig. 4. Output differential voltage error rate with (a) random common & differential mode voltage, (b) random pulse width, (c) random common & differential mode voltage, pulse width.

TABLE I. Coefficient of equation (7), (8).

a_0	-1972.22	b_0	140.12
a_1	2818.65	b_1	-61.25
a_2	-1308.19	b_2	0.108
c	200.2		
d_0	$-2.89628\cdot10^{2}$	d_3	$6.59602\cdot10^{9}$
d_1	$2.80872\cdot10^{5}$	d_4	$-2.29624\cdot10^{11}$
d_2	$7.00444\cdot10^{7}$	d_5	$3.08286\cdot10^{12}$

TABLE II. Coefficient of equation (15) when V_σ = 10mV

e_0	$1.74916\cdot10^{7}$	e_3	$-2.56488\cdot10^{7}$
e_1	$-4.62439\cdot10^{7}$	e_4	$6.69906\cdot10^{6}$
e_2	$4.87790\cdot10^{7}$	e_5	$-6.91940\cdot10^{5}$

III. GAIN AND NOISE MODELING

A. Gain Modeling

The gain of the dynamic amplifier can be expressed as a function of the common mode input voltage, differential input voltage, and pulse width. As shown in Fig. 2, there is a non-linear relationship between common mode input and differential input. Thus, assuming a fixed pulse width, the gain equation is modeled as a nonlinear third-order polynomial for two variables (common mode input voltage and differential mode input voltage) as follows.

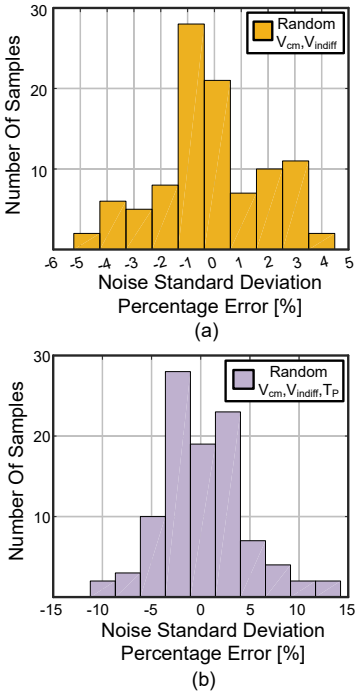

Fig. 5. Standard deviation error rate with (a) random common & differential mode voltage, (b) random common & differential mode voltage, and pulse width

$$\boldsymbol{A(x,y) = a_0V_{cm}^3 + a_1V_{cm}^2 + a_2V_{cm} + b_0V_{diff}^3 + b_1V_{diff}^2 + b_2V_{diff} + c} \tag{11}$$

V_{cm} is common mode input voltage and V_{diff} is differential mode input voltage. The equation (6) can be derived as

$$\boldsymbol{\Delta I = \frac{C_L}{T_P} \cdot A_{diff}(\Delta V_{in}, V_{CM}, T_P)} \tag{12}$$

Assuming a pulse width is fixed, the equation (12) can be expressed as

$$\boldsymbol{\Delta I = C_L \cdot A_{diff}(\Delta V_{in}, V_{CM})} \tag{13}$$

Through current source modeling, a corresponding behavioral model in a fixed pulse can be designed based on these equations.

Next, the coefficient of A_{diff} in the equation of (12) which is related unfixed pulse width can be calculated as follows. The magnitude of the output current according to the pulse width tends to be proportional to the pulse width. However, when the pulse width becomes more than a certain level, the output voltage significantly drops and the gain decreases again as shown in Fig. 1.(c). To consider this effect, the equation (11) is modeled as a fifth order polynomial

$$G(x,y,z) = G(x,y)(d_0T_P^5 + d_1T_P^4 + d_2T_P^3 + d_3T_P^2 + d_4T_P + d_5) \quad (14)$$

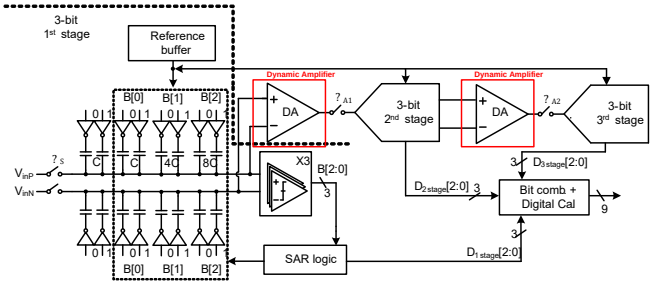

Fig. 6. Block Diagram of 1.1GS/s 7-bit pipelined SAR ADC using Dynamic Amplifiers.

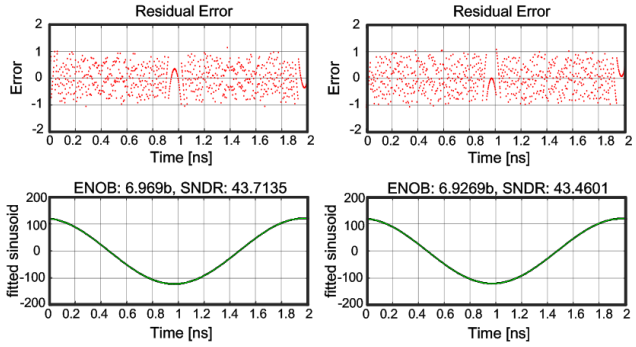

Fig. 7. Effective Number of Bits in (a) SPICE simulation, (b) Verilog-A modeling

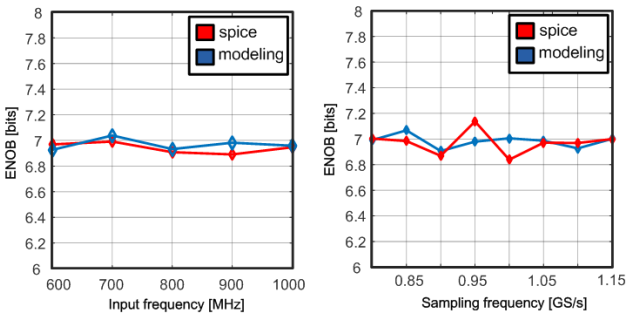

Fig. 8. Effective Number of Bits with (a) input signal frequency, (b) sampling frequency

where T_P is magnitude of pulse width. The coefficients of the polynomial are calculated using the optimization algorithm using the values from the SPICE simulation as target values. Finally, the coefficient of the equation (14) modeled according to three variables is summarized in Table I.

B. Noise Modeling

As mentioned earlier in Chapter 2, section E, noise is affected by the input common voltage. The standard deviation is obtained by performing 196 different noise simulations changing V_{cm} of the dynamic amplifier. The standard deviation of the gain for V_{cm} is modeled by 5th order and a random distribution with this standard deviation is generated so that the equation (12) yields the equation (15) as the output voltage noise. The coefficient of the equation (15) is showed in Table II when V_σ = 10mV.

$$V_\sigma = \begin{pmatrix} e_0V_{cm}^5 + e_1V_{cm}^4 + e_2V_{cm}^3 \\ +e_3V_{cm}^2 + e_4V_{cm} + e_5 \end{pmatrix} \sqrt{T_P} \quad (15)$$

It is important to note that the standard deviation of the output noise should be modeled to be proportional to $\sqrt{T_{pulse}}$ during the time which current is integrated. This is because when white noise is added on the time axis, the variance is proportional to time, and thus the effect on the standard deviation by the pulse width is proportional to the $\sqrt{T_{pulse}}$ as shown in Equation (15). Also, the differential input voltage is considered to improve the accuracy of the noise model. Since it is difficult to model the change of noise by differential input voltage with a general polynomial, find the equation (14) for the expected differential input voltage. Modeling is carried out by applying the standard deviation equation corresponding to each range of differential input voltages to the modeling.

Since the output voltage noise model obtained from Equation (15) needs to be converted into a current noise model to integrate with the gain model obtained earlier, we can apply the equation (16) so that standard deviation of current is calculated.

$$I_\sigma = \frac{V_\sigma C_L}{\sqrt{2T_P}} \quad (16)$$

IV. NUMERICAL EXPERIMENT

To confirm the performance of the gain model proposed in this paper, first the gains of a dynamic amplifier designed at the transistor level and the modeled dynamic amplifier is compared by putting several pairs of random variables. When comparing 100 pairs of random common mode input voltage (480mV~600mV) and differential mode input voltage (1mV~80mV) at a fixed pulse width (53ps) as shown in Fig. 4.(a), the error rate is -5.2% ~ +3.2%. Also, when comparing 50 pairs of random pulse widths (48ps to 111ps) with fixed common mode input voltage (500mV) and differential mode input voltage (30mV), the error rate is within -2% to 3.5% as shown in Fig. 4.(b). When comparing 100 pairs of common mode input voltage (480mV~540mV), differential mode input voltage (1mV~80mV), and random pulse width (44ps~54ps), the error rate is -6.7% ~ +5.4% as shown in Fig. 4.(c). Lastly, when comparing all random 100 pairs, the error rate is -6.7% ~ +5.4% as shown in Fig. 4.(c).

Next, the standard deviation of the amplifier modeled with the noise simulation is compared with several pairs of random variables. When comparing 100 pairs of random common mode input voltage (480mV~600mV) and differential mode input voltage (1mV~80mV) at a fixed pulse width (53ps), the error rate is -5.3% ~ +4.6% as shown in Fig. 5.(a). When comparing 100 pairs of common mode input voltage (480mV~530mV), differential mode input voltage (10mV~80mV), and random pulse width

(48ps~56ps), the error rate is -11.2% ~ +13.5% as represented in Fig. 5.(b).

Fig. 6 shows a top-level block diagram of a 7-bit pipelined SAR ADC we used to verify the performance of our behavioral model. It consists of two gain-of-4 stages with 1-bit redundancy, so two dynamic amplifiers are used. As a result of the design verification, Fig. 7-(a) shows that ENOB (Effective Number of Bits) of the SPICE simulation is 6.9269 bit. Fig. 7-(b) shows that ENOB of using the Verilog-A dynamic amplifier is 6.969 bit so that almost similar performance is obtained. ENOB in Fig. 7. is calculated by using least square fitting IEEE ENOB [10]. In addition, as shown in Fig. 8, the ENOB difference is within 0.0915bit in the input frequency range from 600MHz to 1GHz, and the ENOB difference in the sampling frequency range 800MS/s ~ 1.15GS/s is within 0.1664 bit.

V. CONCLUSION

In this paper, we focused on the fact that the gain of the dynamic amplifier is sensitively changed by various factors such as common mode input voltage, differential mode input voltage, and pulse width so that analyzed the gain change and modeled it based on the result of simulation in the CMOS 28nm process. The error rate of the gain model is -6.7% to +5.4%, making it possible to predict nonlinearity, and the error rate of noise is -11.2% to 13.5%. Since the design verification using the behavioral model improves the simulation operating speed compared to the actual transistor level design, more efficient design is possible when designing a complex system using a behavioral model with dynamic amplifier.

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