Ku-Band Class-J CMOS Power Amplifier Using Sequential Harmonic Impedance Technique

Dana Moon, Jisu Kim, and Juntaek Oh[a]
Department of Intelligent Semiconductors, Soongsil University
Department of Quantum Information Engineering, Sungkyunkwan University (Juntaek Oh)
E-mail : [a]kingojt@skku.edu

***Abstract*— This paper presents a Ku-Band Class-J CMOS Power Amplifier (PA) designed in a 65-nm CMOS process using a single-stage differential cascode topology. To overcome the complexity of the output matching network for high-efficiency Class-J operation, a sequential harmonic impedance technique using a parallel-resonance-based transformer is proposed. This technique simplifies the design process by sequentially optimizing the fundamental and harmonic impedances. Furthermore, a Cold-FET linearizer is utilized to compensate for AM-AM distortion, while a second-harmonic shorting network leveraging the virtual ground of the differential structure is employed to suppress AM-PM distortion to less than 1.6°. Simulation results demonstrate that the PA achieves a peak power-added efficiency (PAE) of 40.2 %, a saturated output power (P_{sat}) of 21.3 dBm, and a large signal gain of 15.2 dB at 14 GHz. These results verify that the PA simultaneously satisfies the requirements for high efficiency and linearity.**

***Keywords*—CMOS, Ku-band, power amplifier, Class-J, harmonic tuning**

I. INTRODUCTION

As satellite communications (SATCOM) and 6G Frequency Range 3 (FR3) applications continue to expand, the demand for high-performance power amplifiers (PAs) operating in the Ku-band has surged [1]–[5]. In this frequency regime, CMOS technology is highly preferred for realizing fully integrated RF transceivers due to its high integration density and cost-effectiveness. However, the inherent low breakdown voltage and lossy silicon substrate of scaled CMOS processes pose significant challenges in securing sufficient output power and efficiency while maintaining linearity [6].

To overcome the power and efficiency limitations of CMOS devices, harmonic-tuned switching modes, such as Class-F and Class-J, have been actively researched. Among them, Class-J operation is particularly advantageous for modern wireless systems as it utilizes a complex fundamental load with capacitive harmonic termination, offering wider bandwidth and simpler implementation compared to the stringent harmonic shorts or opens required by Class-F [7]. However, designing an output matching network (OMN) that simultaneously satisfies the complex impedance conditions for both fundamental and harmonic frequencies is non-trivial. Conventional Class-J OMNs often rely on bulky passive networks or complex transformer structures to control multiple harmonics, which inevitably degrades the passive quality factor (Q-factor) and increases the chip area. Although some designs have achieved high efficiency, they often suffer from design complexity where fundamental and harmonic impedances are coupled, making the optimization process iterative and time-consuming.

Furthermore, implementing modern communication systems with high spectral efficiency, such as 64-QAM, requires stringent linearity to prevent signal distortion. While digital pre-distortion (DPD) can effectively linearize the PA, it consumes substantial system power and computational resources, making analog linearization techniques integrated within the PA core more desirable. Consequently, Cold-FET-based linearizers have been widely adopted to compensate for AM-AM distortion because they consume negligible DC power and are easily integrated. However, addressing amplitude-to-phase (AM-PM) distortion remains a critical bottleneck. In differential topologies, a second-harmonic appears as a common-mode signal, creating a floating impedance node at the common source that induces significant phase deviation [8]. To suppress this AM-PM distortion, conventional methods often employ additional filtering stages or bulky capacitor banks, which lead to increased insertion loss and degraded overall efficiency.

To overcome these challenges, this paper proposes a highly linear and efficient Ku-band Class-J CMOS PA utilizing a sequential harmonic impedance technique. Unlike conventional approaches that struggle with coupled impedance tuning, the proposed design employs a parallel-resonance-based transformer OMN. This structure strategically utilizes the resonance between the primary inductance and parasitic capacitance to secure the Class-J harmonic condition first, followed by independent fundamental matching, thereby simplifying the design procedure. Moreover, to achieve high linearity without compromising efficiency, two distinct linearization mechanisms are integrated: an adaptive Cold-FET linearizer for AM-AM compensation and a second-harmonic shorting network leveraging the virtual ground concept for AM-PM

a. Corresponding author; kingojt@skku.edu

Manuscript Received Jan. 30, 2026, Revised Sep. 15, 2026, Accepted Sep. 15, 2026

This is an Open Access article distributed under the terms of the Creative Commons Attribution Non-Commercial License (http://creativecommons.org/licenses/by-nc/4.0) which permits unrestricted non-commercial use, distribution, and reproduction in any medium, provided the original work is properly cited.

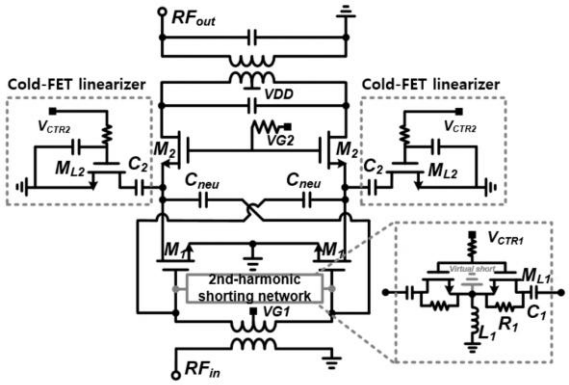


Fig. 1. Schematic of the proposed CMOS PA with the Cold-FET linearizer (M_{L2}, C_2) and the second-harmonic shorting network (M_{L1}, L_1, C_1).

suppression. This integrated approach allows for a compact, high-performance Ku-band PA that effectively balances the trade-offs between design complexity, efficiency, and linearity.

II. DESIGN METHODOLOGY

Fig. 1 shows the schematic of the proposed Ku-band Class-J PA designed using a 65-nm RF CMOS process. A differential cascode topology is adopted to overcome the low breakdown voltage limitation and enable a large output voltage swing. The power cell is optimized with total gate widths of 739.2 μm for the common-source (CS) stage and 369.2 μm for the common-gate (CG) stage. To enhance stability and reverse isolation, a cross-coupled neutralization capacitor (C_{neu}) of 161 fF is employed to cancel the parasitic gate-drain capacitance (C_{gd}). Both the input matching network (IMN) and output matching network (OMN) utilize on-chip edge-coupled transformers to achieve a high-quality factor (Q-factor) and to provide inherent DC isolation between stages without requiring additional blocking capacitors, thus improving integration density.

The OMN is designed based on an edge-coupled transformer with a parallel resonant structure to support high-efficiency Class-J operation. Class-J operation employs a complex fundamental load with an inductive component and a capacitive harmonic termination, which shapes a phase shift between the drain voltage and current waveforms to reduce the overlap region, thereby minimizing power dissipation and maximizing efficiency. As illustrated in the equivalent circuit in Fig. 2(a), the proposed OMN exploits a parallel resonance mechanism involving the primary inductance (L_{O1}), the parasitic drain-source capacitance (C_{ds}), and an additional parallel capacitor (C_{O1}) to sequentially control harmonic impedances. The design proceeds sequentially as follows. Once the parallel resonance at the fundamental frequency (f_0) is enforced, i.e., $L_{O1}(C_{ds} + C_{O1}) = 1/\omega_0^2$, the primary-side admittance at the second harmonic becomes $Y_P(2\omega_0)=j[2\omega_0(C_{ds}+C_{O1})-1/(2\omega_0 L_{O1})] = j3/(2\omega_0 L_{O1})$, so that the second-harmonic impedance reduces to $Z_P(2f_0) \approx -j(2/3)\omega_0 L_{O1}$ and is governed by L_{O1} alone. Accordingly, L_{O1} is first chosen to realize the capacitive second-harmonic termination required for the voltage-

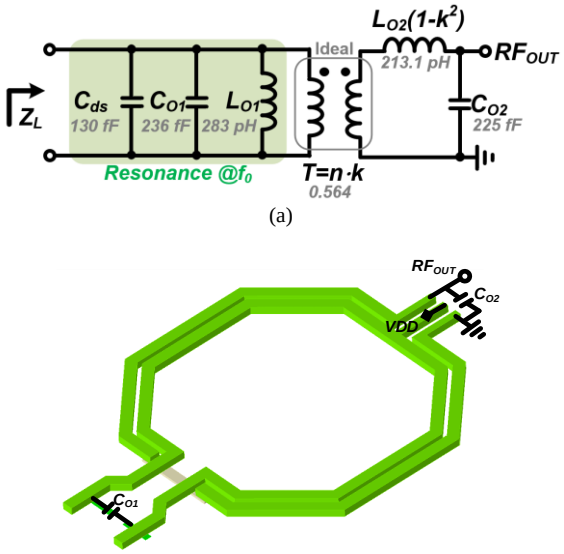


Fig. 2. Proposed parallel-resonance-based output matching network: (a) odd mode equivalent circuit and (b) Layout.

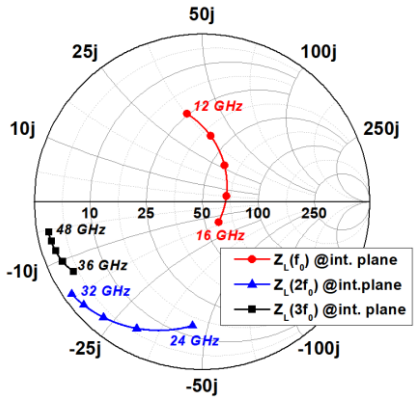
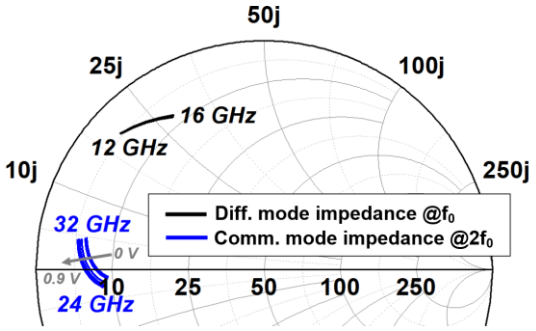


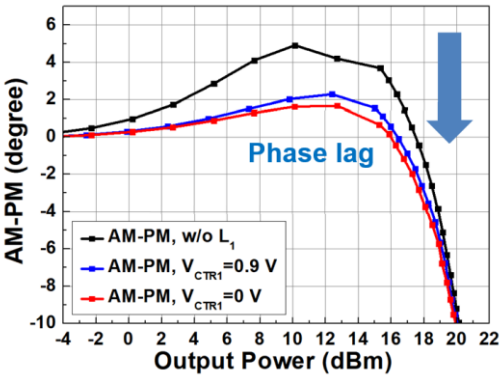
Fig. 3. Simulated impedance of the proposed output matching network at fundamental and harmonic frequencies.

peaking characteristic of Class-J operation, and C_{O1} is then determined from the resonance condition so that the tank presents a high impedance at f_0. This high-impedance condition effectively decouples the fundamental matching from the harmonic termination, and consequently the fundamental load impedance is determined solely by the secondary-side parameters—specifically the secondary inductance (L_{O2}), matching capacitor (C_{O2}), and the coupling coefficient (k).

Furthermore, at the third harmonic ($3f_0$), the total shunt capacitance provides a low-impedance path, approximating a short-circuit condition ($Z_P(3f_0) \approx -j(3/8)\omega_0 L_{O1}$ under the same resonance condition). In this design, the component values are optimized to L_{O1}=283 pH, C_{ds}=130 fF, C_{O1}=236 fF, and C_{O2}=225 fF to ensure precise Class-J impedance termination across the target bandwidth, as shown in the layout in Fig. 2(b). The resulting simulated load impedance trajectories are plotted in Fig. 3, confirming that the optimal Class-J impedances are achieved. For the final component values, the lumped model of Fig. 2(a) predicts $Z_P(2f_0) \approx -j23$ Ω at 28 GHz, in good agreement with the EM-simulated trajectory in Fig. 3. It should be noted that, without C_{O1}, L_{O1} and C_{ds} alone would resonate near 26 GHz, so that the



(a)



(b)

Fig. 4. Simulated results versus bias voltage V_{CTR1}: (a) fundamental and second-harmonic impedances and (b) AM-PM characteristics.

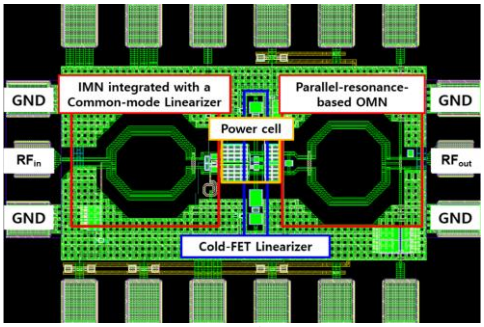


Fig. 5. Chip Layout of the proposed PA.

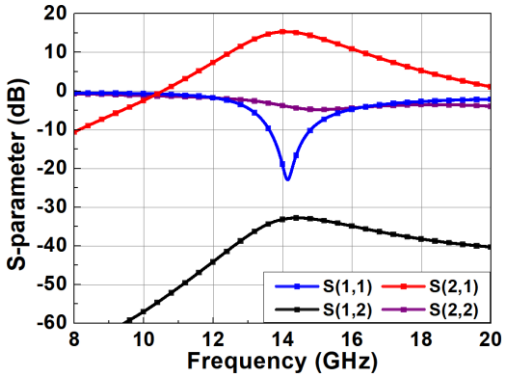


Fig. 6. Simulated S-parameters of the proposed PA.

second-harmonic impedance would approach an open circuit ($|Z_P| > 300\ \Omega$) rather than the required capacitive termination; adding C_{O1} shifts the resonance down close to f_0 and moves $Z_P(2f_0)$ into the capacitive region, which is the essence of the proposed sequential tuning. The secondary-side elements (L_{O2}, C_{O2}, and k) were finally fine-tuned by EM co-simulation for the fundamental match, since they have a negligible influence on the harmonic impedances.

To achieve high linearity alongside high efficiency, two distinct linearization mechanisms are integrated into the proposed PA: a Cold-FET linearizer for AM-AM compensation and a second-harmonic shorting network for AM-PM compensation. First, to alleviate gain compression at high power levels, an adaptive Cold-FET linearizer is incorporated between the differential CS and CG stages as shown in Fig. 1. This auxiliary transistor operates in the deep triode region as a voltage-dependent variable resistor with zero drain-to-source voltage [9]. As the input power increases, the large voltage swing at the gate causes the effective channel resistance of the Cold-FET to increase. This variable resistance generates a gain expansion characteristic that counteracts the inherent gain compression of the main amplifier, thereby extending the output 1-dB compression point (OP_{1dB}) and improving linearity. The gate width of the Cold-FET (M_{L2}) is optimized to 32 μm with series capacitor (C_2) of 1.3 pF and the bias voltage is optimized to 0.46 V.

The linearizer is inserted at the interstage node between the CS and CG devices because this node is inherently low-impedance (approximately $1/g_m$ of the CG device) and is isolated from both the IMN and the OMN; the shunt Cold-FET branch (C_2 in series with M_{L2}) therefore modulates the signal-current division at this node without disturbing the high-Q input and output matching networks [6]. Since the branch is a shunt element whose channel resistance is much larger than the node impedance, its loss appears only as a slight reduction of the small-signal gain rather than as a series insertion loss, and this effect is included in all the reported results (Figs. 6–10).

Second, to suppress phase distortion, a second-harmonic shorting network is integrated with the input matching network as shown in Fig. 1. As shown in the inset of Fig. 1, the network consists of two MOS capacitors (M_{L1}) connected from the differential gate nodes of the CS stage to a common center node, which is grounded through L_1. For the fundamental (odd-mode) signal, the center node acts as a virtual ground. However, the second-harmonic component appears as a common-mode signal, for which the differential IMN provides no low-impedance return path; the resulting floating second-harmonic impedance re-modulates the input capacitance of the CS devices and induces significant phase deviation [5]. To address this, the series LC resonator formed by L_1 and the two parallel-connected C_1 (effectively $2C_1$) is tuned to the second-harmonic frequency ($2f_0$) to provide a low-impedance common-mode path, preventing harmonic feedback and minimizing phase deviation across the output power range. The resonator utilizes a spiral inductor (L_1) of approximately 95 pH and a capacitor (C_1) of 174 fF implemented via a MOSFET (M_{L1}) with a width of 44 μm. In this structure, the second-harmonic impedance can be fine-tuned by adjusting the bias voltage, while the differential-mode impedance at f_0 remains purely reactive and nearly independent of the bias, so that it is simply absorbed into the IMN, as shown in Fig. 4(a). Furthermore, Fig. 4(b) demonstrates that the addition of inductor L_1 significantly reduces the peak phase distortion. Based on

simulation results, the bias voltage is optimized to 0.9 V to minimize phase deviation.

A MOSFET is employed as C_1 instead of a fixed MIM capacitor so that the resonance frequency of the shorting network can be fine-tuned by V_{CTR1} (Fig. 4(a)), which provides a means to compensate for the process variation of L_1 and the layout parasitics after fabrication. Since M_{L1} is biased in strong inversion (V_{CTR1} = 0.9 V), its gate capacitance lies in the flat region of the C–V characteristic, so that the capacitance variation with the signal swing is small; in addition, the fundamental voltage swing at the gate node is much smaller than that at the drain. The residual power-dependent capacitance variation is inherently captured by the harmonic-balance simulations in Fig. 9, which include the full nonlinear model of M_{L1}.

III. RESULT AND DISCUSSION

Fig. 5 presents the layout of the proposed Ku-band Class-J PA. The circuit was designed using the TSMC 65-nm RF CMOS process, occupying a compact chip area of 0.5 × 0.74 mm^2 including all probe pads. In this design, a parallel-resonance-based transformer is employed at the output stage to perform sequential harmonic impedance tuning for high-efficiency operation. To verify the circuit performance, post-layout simulations were conducted using Keysight ADS, incorporating electromagnetic (EM) models for all passive components and interconnects. The PA is biased at a supply voltage of 2.2 V, while the gate bias voltages for the common-source and the common-gate stages are set to 0.285 V and 1.45 V, respectively, for Class-AB operation. Under these bias conditions, the simulated S-parameters are plotted in Fig. 6.

The PA achieves a peak small-signal gain (S_{21}) of 16.5 dB at 13.4 GHz, the 3-dB bandwidth spans from 12.4 to 14.8 GHz, confirming the input (S_{11}) and output (S_{22}) return losses exhibit good matching characteristics across the operating band. Although the large-signal results below are reported at 14 GHz, the load impedance trajectories in Fig. 3 remain within the Class-J region over 12–16 GHz and the small-signal response is flat over the 3-dB bandwidth, indicating that the large-signal performance is maintained over the Ku-band of interest. Fig. 7 illustrates the simulated time-domain voltage and current waveforms to verify the operational mode of the proposed output matching network for Class-J PA. The results demonstrate that the current waveform exhibits the reactive second-harmonic termination, which minimizes the overlap between high voltage and current regions, thereby reducing power dissipation and enhancing efficiency. All transistors are standard thin-oxide (1.2-V) devices, and the peak drain voltage of the cascode (≈ 4.3 V, Fig. 7) is shared between M_1 and M_2. Because the CG gate is biased at 1.45 V, the drain of M_1 is held at approximately $V_{G2} - V_{GS2}$ (≈ 1 V), so that M_1 sees only a small drain–source swing while M_2 sustains the remaining swing, with a peak V_{DS} of about 3.3 V and a peak gate–drain voltage of about 2.9 V. As shown in Fig. 7, the voltage peak coincides with the current minimum, i.e., the high-voltage excursion occurs while M_2 is nearly off; this minimizes hot-carrier stress, which

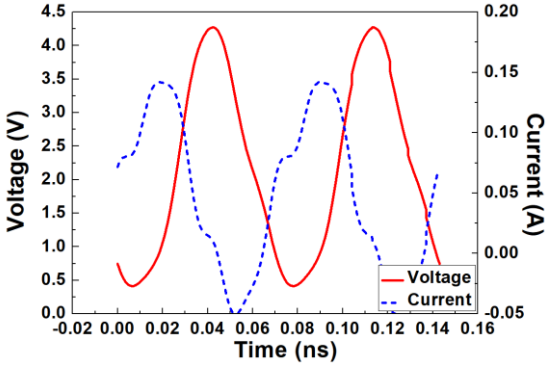


Fig. 7. Simulated drain voltage and current waveforms.

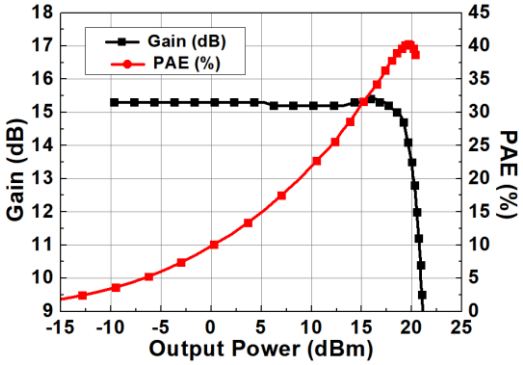


Fig. 8. Simulated gain and PAE versus output power at 14 GHz.

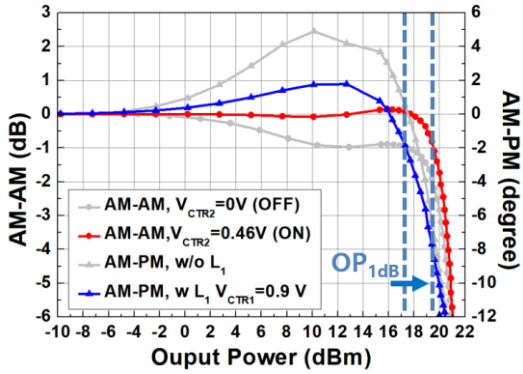


Fig. 9. Simulated AM-AM and AM-PM distortion versus output power.

requires simultaneously high V_{DS} and high current, so that the oxide stress during the short voltage peak is the primary reliability concern. This stress level is comparable to that commonly accepted for thin-oxide cascode CMOS PAs operating from 2-V-class supplies, and the long-term reliability under continuous RF operation remains to be verified by measurement. Fig. 8 plots the simulated large-signal gain and power-added efficiency (PAE) versus output power at 14 GHz. The PA achieves a saturated output power (P_{sat}) of 21.3 dBm and a peak PAE of 40.2 % while the large-signal gain remains high at 15.2 dB. Since these results are obtained from post-layout simulation, some degradation is expected in silicon measurement, mainly due to the modeling inaccuracy of the transformers (coupling coefficient and Q-factor), the pad and interconnect parasitics, and the accuracy of the transistor model at high frequency. As typically observed for Ku-band CMOS PAs, a reduction of about 1–2 dB in P_{sat} and gain and a few percentage points in PAE, together with a slight downward shift of the center

TABLE I. Comparison of Recently Reported CMOS PA.

	[1]	[9]	[10]	[11]	This work*
Technology	65nm CMOS	65nm CMOS	90nm CMOS	65nm CMOS	**65nm CMOS**
Results	Meas.	Meas.	Meas.	Meas.	Post-layout sim.
Freq. (GHz)	13.7-16.7	31	18	31	**14**
Gain (dB)	21.9	18.9	10.71	16.4	**15.2**
Peak PAE (%)	54.1	38.2	42.7	36.4	**40.2**
P_{sat} (dBm)	14.5	17.2	14.14	15.92	**21.3**
Architecture	2-stage/CS	2-stage/Cascode	1-stage/CS(CCF)	2-stage/ combiner-based(CCF)	**1-stage/ Cascode(CJ)**
Size (mm^2)	0.3**	0.47	0.43	0.31	**0.37**
FoM***	73.3	81.7	66.3	77.8	**75.5**

*: post-layout simulation results (references: measured results), **: Core area excluding pads.
***: FoM=P_{SAT}[dBm] + Gain [dB] + 20log10(f_c[GHz]) + 10log$_{10}$(PAE_{MAX}[%])

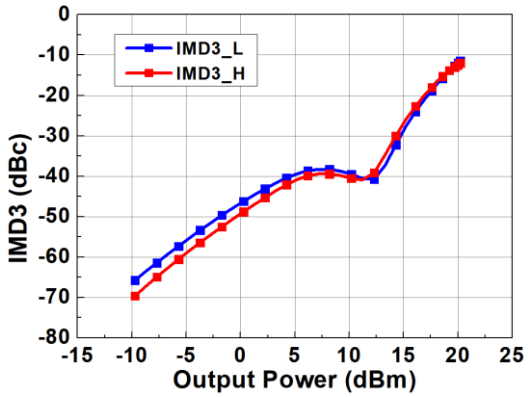


Fig. 10. Simulated IMD performance with 100-MHz tone spacing at 14 GHz.

frequency, are anticipated. The bias-tunable second-harmonic shorting network (V_{CTR1}) and the Cold-FET bias (V_{CTR2}) provide means to partially recover the linearity after fabrication.

To validate the effectiveness of the proposed linearization techniques, Fig. 9 compares the simulated AM-AM and AM-PM distortion characteristics with and without the linearizers. The AM-AM distortion plot reveals that without the Cold-FET linearizer (OFF)state, the PA suffers from early gain compression, whereas when the Cold-FET is enabled (ON state), it generates a gain expansion characteristic thereby significantly extending the output 1-dB compression point (OP_{1dB}) and flattening the gain response. Simultaneously, the AM-PM distortion performance is analyzed to verify the second-harmonic shorting network. By employing the proposed LC resonator to shorten the second harmonic, the feedback path induced by the floating impedance is effectively blocked, thereby suppressing severe phase deviation. Consequently, the total phase distortion is suppressed to less than 1.6°. Finally, Fig. 10 presents the simulated third-order intermodulation distortion (IMD3) performance with a 100-MHz tone spacing, which maintains low levels across the linear power range. The IMD3 remains below −38 dBc up to an output power of 12 dBm and exhibits a local minimum (sweet spot) near 11–12 dBm, which is the characteristic signature of the third-order nonlinearity cancellation between the gain expansion of the Cold-FET linearizer and the gain compression of the main amplifier shown in Fig. 9.

IV. CONCLUSION

This paper presents a Ku-band Class-J PA designed in a 65-nm CMOS process. To achieve high efficiency while resolving the design complexity of harmonic-tuned modes, a sequential harmonic impedance technique using a parallel-resonance-based transformer was proposed. This configuration utilizes a parallel resonance to simplify the matching network structure, thereby enabling a sequential optimization process for the harmonic and fundamental impedances. Additionally, a Cold-FET linearizer and a virtual-ground-based second-harmonic shorting circuit were integrated to minimize amplitude and phase distortions, respectively. The proposed PA exhibits a saturated output power (P_{sat}) of 21.3 dBm, a peak PAE of 40.2 %, and a large-signal gain of 15.2 dB, occupying a core area of 0.37 mm^2. The simulation results confirm the effectiveness of the proposed linearizers, showing a suppressed AM-PM distortion of less than 1.6°. Consequently, the proposed design offers a promising solution for PAs requiring simultaneously high efficiency and linearity.

ACKNOWLEDGMENT

The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), Korea. This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT). (No. RS-2025-25444462).

REFERENCES

[1] J. Zhong, D. Zhao, and X. You, "A Ku-band CMOS power amplifier with series-shunt LC notch filter for satellite communications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 5, pp. 1869–1881, May 2021.

[2] J. Xu, et al., "A Compact Doubly Neutralized Ku-Band Power Amplifier With 39% Peak PAE and 23-dBm Output Power in 22FDX+ EDMOS for 6G FR3," *IEEE Microwave and Wireless Technology Letters*, 2025.

[3] J.-H. Kim *et al.*, "An efficient Ku-band two-way vertical-like power-combining power amplifier using merged inter-stage transformers achieving 23–23.4 dBm P_{sat} and 45.2–46.6% peak PAE in 65nm CMOS," in *IEEE Radio Frequency Integrated Circuits Symposium (RFIC) Dig.*, Washington, DC, USA, Jun. 2024.

[4] J. Yang, J. Lee, S. Jang, H. Jeong, C. Kim, and C. Park, "Ku-band CMOS power amplifier with three-stack power stage to enhance output power and efficiency," *Applied Sciences*, vol. 12, no. 9, p. 4432, Apr. 2022.

[5] S. Lim *et al.*, "A Ku-band CMOS power amplifier with 37.6% peak PAE and 22.5 dBm P_{sat} for 6G applications," in *Proc. IEEE Int. Symp. Radio-Frequency Integration Technology (RFIT)*, Kagoshima, Japan, 2025, pp. 7–9, doi: 10.1109/RFIT65667.2025.11364570.

[6] J. Yang et al., "A 3.3-V Ku-Band Front-End Module With 2.6-dB NF and 18.9-dBm OP1dB in 65-nm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 4, pp. 1163–1167, Apr. 2021.

[7] Y. Dong, L. Mao, and S. Xie, "Fully integrated Class-J power amplifier in standard CMOS technology," *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 1, pp. 64–66, Jan. 2017.

[8] M. Yang, D. Zhao, and X. You, "A Ku-band CMOS balanced driver amplifier with transformer-based notch filter for SATCOM phased arrays," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 9, pp. 3318–3322, Sep. 2023.

[9] J. Park, S. Kang, and S. Hong, "Design of a Ka-band cascode power amplifier linearized with cold-FET interstage matching network," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 2, pp. 1429–1438, Feb. 2021.

[10] T. -W. Huang, Y. -W. Wang, J. -H. Huang, K. -J. Chuang and J. -H. Tsai, "A K-Band 42.7% PAE Power Amplifier Supporting Two Carrier Aggregation in 90 nm CMOS," *IEEE 2024 Asia-Pacific Microwave Conference (APMC)*, pp.13-15, Nov. 2024.

[11] A. Batabyal *et al.*, "A 0.9-V 36% PAE Broadband Continuous Class-F CMOS mm-Wave Power Amplifier Using Novel Current-Mode Power Combiner," *IEEE Transactions on Microwave Theory and Techniques*, vol. 73, no. 2, pp. 938-952, Jul. 2024.

Dana Moon (Student Member, IEEE) received the B.S. degree in electronic engineering from Soongsil University, South Korea, in 2024, where she is currently pursuing the M.S. degree with the Department of Intelligent Semiconductors. Her research interests include radar systems and RF ICs for 6G communications.

Jisu Kim received the B.S. degree in the Department of Robotics Engineering, Yeungnam University, Gyeongsan, Korea, in 2021. She is currently pursuing her integrated M.S. and Ph.D. degree in electronic engineering from Soongsil University, Seoul, Korea.

Her research interests include CMOS IC, quantum computers and radar systems.

Juntaek Oh received his B.S., M.S., and Ph.D. degrees in Electronics and Electrical Engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 2010, 2012, and 2016, respectively.

From 2016 to 2018, he was with the Advanced Medical Device Research Division, Korea Electrotechnology Research Institute (KERI), Ansan, South Korea. From 2018 to 2020, he was an Assistant Professor with the Department of Robotics Engineering, Yeungnam University, Gyeongsan, South Korea. From 2020 to 2026, he was with the School of Electronic Engineering and the Department of Intelligent Semiconductors, Soongsil University, Seoul, South Korea, where he was an Associate Professor. Since 2026, he has been with the Department of Quantum Information Engineering, Sungkyunkwan University, Suwon, South Korea, where he is currently an Associate Professor.

His main research interests include integrated circuits for large-scale quantum computers, AI-based automated RF circuit design, RF wireless power transfer, radar sensor ICs, and communication systems for 6G and LEO satellites.