A CMOS Temperature Independent Resistor Using a Bilinear Switched-Capacitor for Temperature Sensor

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Abstract - **High-precision analog circuits, such as integrated voltage references, are severely constrained by the intrinsic thermal drift of passive CMOS resistors, whose high Temperature Coefficients (TCs) fail to meet modern stability requirements (often <1 ppm/°C). This paper proposes a robust, nearly temperature-independent resistor utilizing a bilinear switched-capacitor (SC) circuit. By dynamically defining the equivalent resistance, the proposed architecture leverages the temperature characteristic of a capacitor—which is significantly smaller than that of a conventional resistor—thereby demonstrating superior temperature independence.**

Simulation results demonstrate exceptional thermal robustness: the SC resistor achieved a TC of 1.25 ppm/°C range, representing a stability improvement of approximately 2.24 times over leading prior active and SC-based reference circuits. This work establishes the SC equivalent resistor as a high-precision, area-efficient, and electronically controllable reference solution.

Keywords—**Temperature sensor, switched capacitor, temperature coefficient, CMOS resistor**

I. INTRODUCTION

Precision analog and mixed-signal circuits, such as bandgap voltage references and high-accuracy temperature sensors, critically depend on stable resistor ratios to define temperature-invariant reference indicators, with high-performance applications demanding stability often below 1 ppm/◦C [1]-[2]. However, integrated resistors fabricated in standard CMOS processes, typically using doped polysilicon or diffused regions, exhibit inherent thermal instability which is primarily caused by the complex and competing temperature dependencies of carrier mobility and carrier concentration within the semiconductor material [2]. Realizing true temperature independence is challenging because passive compensation, such as optimizing doping to find a zero temperature coefficient(TC) point or combining components with opposite TCs, is highly sensitive to fabrication process variations and often leaves unacceptable residual second-order drift, thereby limiting precision.

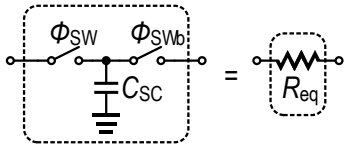

Figure 1. The structure of switched capacitor circuit, and its representation as equivalent resistor

This architectural challenge motivates the use of a capacitor as a temperature-independent resistor, rather than modifying the temperature characteristic of a passive resistor. This approach can be realized for two reasons: 1) the temperature coefficient of a capacitor is typically ten times smaller than that of a poly resistor, and 2) a capacitor can function as an equivalent resistor through a switched capacitor topology. Figure 1 shows the structure of switched capacitor. The switches placed beside the capacitor turn on and off based on the switching clock frequency, and this operation makes the switched capacitor seen as a resistor.

This paper proposes a temperature-independent resistor implemented by exploiting the equivalent resistance inherent in a switched capacitor network. The equivalent resistance of the circuit is dynamically tunable via the switching frequency and the circuit's capacitance, offering a significant functional and control advantage over the fixed, material-dependent values of passive CMOS resistors. Furthermore, this work explores the use of the bilinear resistor topology—a structural variation of the switched capacitor circuit—demonstrating that this configuration allows for the achievement of identical resistance values using smaller capacitor areas or slower switching frequencies, thereby supporting the key benefits of the SC approach in terms of silicon area efficiency and power optimization.

II. DESIGN METHODOLOGY

A. Basic idea of switched capacitor

The fundamental switched capacitor structure, illustrated in Figure 1, is composed of a single sampling capacitor and surrounding switches. These switches operate on distinct, non-overlapping clock phases to achieve discrete charge transfer. During the first phase, the capacitor stores a specific

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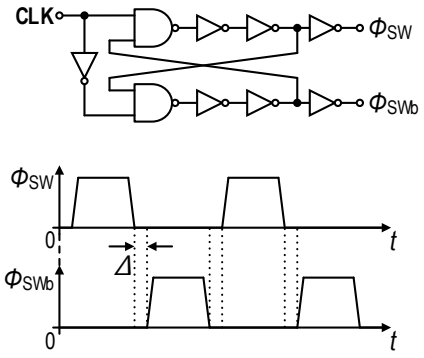

Figure 2. The circuit of non-overlapping clock generator, and timing diagram of its outputs.

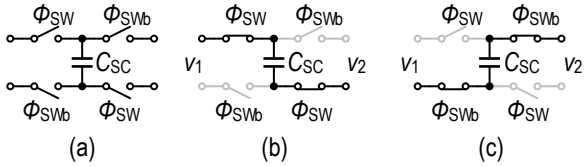

Figure 3. (a)The structure of bilinear switched capacitor resistor, and (b,c)switching operation of the structure.

amount of charge from the input node, and in the subsequent phase, the switches reconfigure to transfer this stored charge packet to the output node.

The implementation of two non-overlapping clock signals is crucial; this ensures that both switches are never simultaneously enabled during clock transitions, preventing potential short-circuit paths and preserving the integrity of the charge transfer. The required non-overlapping clock signals are typically generated by a dedicated circuit, shown in Figure 2, which is designed to logically enforce that one clock output is forced low before the other transitions high, thereby producing the precise timing sequence required for robust SC operation.

The SC's continuous charge transferring operation can be depicted as constant current flowing, and this operation can be seen as resistor. Based on these operation, SC circuit can be seen as equivalent resistance R_{eq}, where the amount of resistance is

$$R_{\mathrm{eq}} = \frac{T_{\mathrm{SC}}}{C_{\mathrm{SC}}} = \frac{1}{C_{\mathrm{SC}} f_{\mathrm{SC}}} \quad (1)$$

where C_{SC} the capacitance of the circuit, T_{SC} and f_{SC} the period, and frequency of switching clock, respectively.

B. The equivalent resistance of bilinear switched capacitor resistor structure

The structure of SC can have several variations based on the placement of switches. Figure 3 shows one of SC structure called bilinear switched capacitor resistor [3].

Figure 3(b,c) shows switching operation of bilinear SC structure. The charge transferred from node v_1 to v_2 for Figure 3(b) and 3(c) are

$$\Delta q_1 = C_{\mathrm{SC}}(v_1 - v_2) - C_{\mathrm{SC}}(v_2 - v_1) = 2C_{\mathrm{SC}}(v_1 - v_2) \quad (2)$$

and

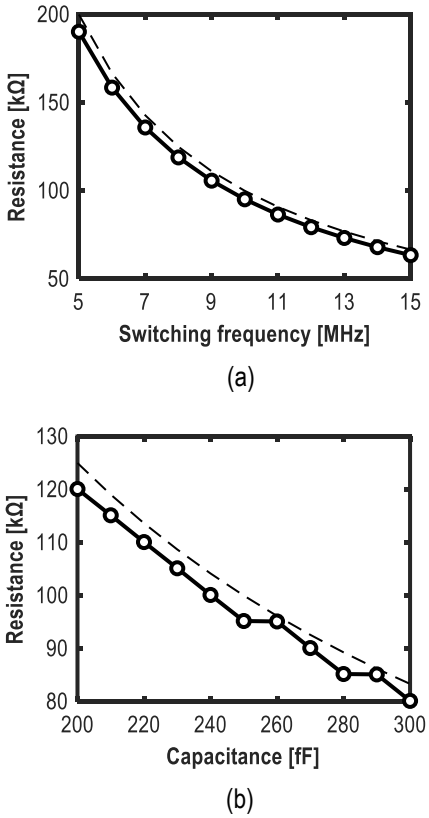

Figure 4. The simulation result of bilinear SC circuit by (a)changing switching clock frequency, and (b)changing sampling capacitance.

$$\Delta q_2 = C_{\mathrm{SC}}(v_2 - v_1) - C_{\mathrm{SC}}(v_1 - v_2) = 2C_{\mathrm{SC}}(v_2 - v_1) \quad (3)$$

respectively. The average current flow at one switching period becomes

$$I_{\mathrm{avg}} = \frac{\Delta q_1 - \Delta q_2}{T} = \frac{4C_{\mathrm{SC}}(v_1 - v_2)}{T} \quad (4)$$

where T is period of switching clock.

According to Ohm′s law, the equivalent resistance becomes

$$R_{\mathrm{eq}} = \frac{(v_1 - v_2)}{I_{\mathrm{avg}}} = \frac{T}{4C_{\mathrm{SC}}} = \frac{1}{4C_{\mathrm{SC}} \cdot f_{\mathrm{SC}}} \quad (5)$$

The theoretical analysis leading to equation (5) demonstrates a substantial efficiency advantage for the bilinear SC resistor structure: it requires four times less sampling capacitance compared to the basic SC configuration as in Figure 1 to achieve an identical equivalent resistance. This enhancement directly results in significant silicon area savings and offers the flexibility to utilize either smaller capacitor areas or slower switching frequencies for equivalent resistance generation.

To validate this relationship, simulation results for the bilinear SC resistor structure are presented in Figure 4. The two plots illustrate the simulated resistance when varying the switching frequency (with the sampling capacitance C_{SC} fixed at 250 fF) and when varying C_{SC} (with the switching frequency fixed at 10 MHz). In both cases, the simulated

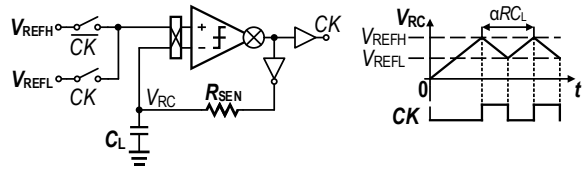

Figure 5. Structure of RC-delayed pulse generating oscillator

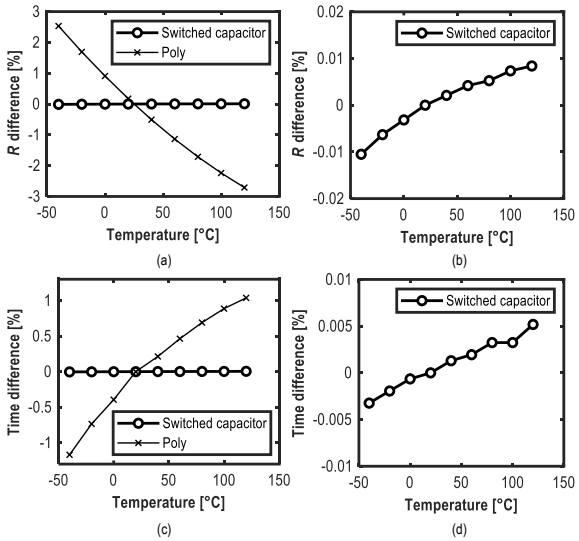

Figure 6. Simulation results of (a) resistance difference of two resistors and (b) zoomed graph of switched capacitor resistance by temperature, and (c) time difference and (d) zoomed graph of switched capacitor resistance for reaching 1024 pulse count of RC-delayed pulse.

data points rigorously follow the theoretical trend predicted by equation (5) (represented by the dashed line), confirming the robust functionality and predictive accuracy of the proposed bilinear SC equivalent resistance.

III. APPLICATION OF SWITCHED CAPACITOR RESISTOR

Figure 5 illustrates the structure of an oscillator that generates an RC-delayed pulse. Integrated temperature sensors leveraging this structure typically calculate the temperature difference by comparing a temperature-independent pulse against a temperature-dependent pulse [4]. To ensure the generation of a stable, temperature-independent reference pulse, the passive resistor within the RC timing network must itself be temperature-invariant; thus, the proposed SC equivalent resistor would serve as an excellent, non-drifting replacement. Furthermore, by utilizing a large capacitor within the RC network—a common requirement in SC architectures—designers can effectively reduce the ripple voltage introduced during the switching operation, providing a secondary advantage that reinforces the suitability of the SC resistor in this application.

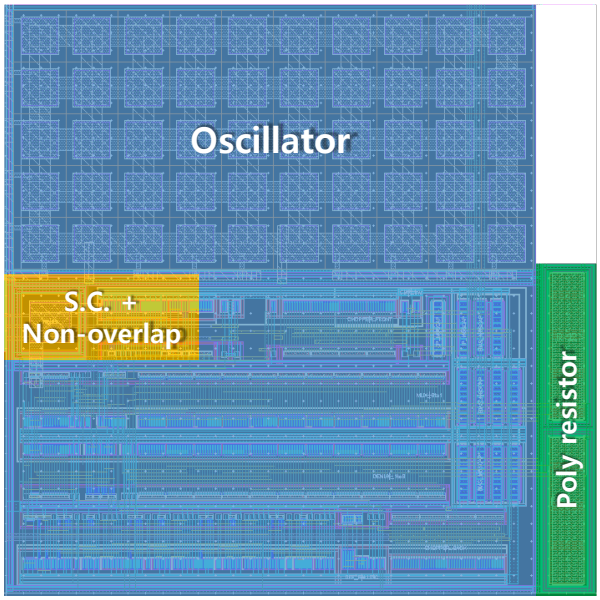

Figure 7. Chip layout of proposed SC resistor with poly resistor and RC-delayed pulse generating oscillator.

IV. RESULTS AND DISCUSSIONS

Figure 6(a) presents a comparative simulation illustrating the thermal performance of the proposed bilinear SC resistor structure against a conventional non-salicided polysilicon resistor. To implement the SC resistor, a MIM capacitor with a temperature coefficient of -29.4 ppm/℃ in the TSMC 180nm RF process was utilized, alongside an ideal reference clock for generating the switching clock. Over the wide temperature range of −40°C to 120°C, the passive polysilicon element exhibits a substantial resistance change of approximately ±3%. In stark contrast, the SC equivalent resistance demonstrates exceptional stability, registering a total variation of about 0.02% across the entire operational range, corresponding to a remarkably low temperature coefficient of 1.25 ppm/°C, as shown in Figure 6(b). This superior stability translates directly to system performance, as shown in Figure 6(c), which compares the difference in time required to count 1024 RC-delayed pulses. While the poly resistor network experiences a drift of ±1.1% over the temperature sweep, the SC-based system maintains stability with about 0.008% variation, as shown in Figure 6(d). The Beyond thermal robustness, the SC resistor offers significant area efficiency, as highlighted by the layout in Figure 7 (fabricated in the TSMC 180 nm RF process). The SC resistor, designed to yield 100 kΩ at a 10 MHz switching clock, occupies an area of 1,182 μm^2, including SC resistor itself and non-overlaping clock generator. This area is smaller compared to area 1,354 μm^2 required by the passive polysilicon resistor. However, a trade-off exists regarding power and clock idealities. Specifically, the SC resistor consumes 18.46 μW of dynamic power (including the non-

TABLE 1. Comparison with Other Temperature Independent Resistor

	This work	[5]	[6]	[7]
Process[nm]	180	180	130	40
Temperature Range[°C]	-40~125	-40~120	25~200	-25~80
TC[ppm/°C]	1.25	2.8	169	57
Area[μm^2]	1182	9198	-	750
Power[μW]	18.46	*-	*-	0.25
Dynamic adjustment	O	X	X	O

*Resistor models consisted of only passive components considered zero power consumption required for its operation

overlapping clock generation) per switching cycle, which must be considered for power-constrained applications. Additionally, in practical implementations, any temperature drift from a realistic on-chip frequency reference would introduce additional thermal variations to the SC resistor's overall temperature characteristic.

Table I presents a comprehensive performance comparison against several integrated components requiring temperature independency [5]-[7]. The proposed SC resistor exhibits significantly superior performance in temperature stability, achieving a temperature coefficient (TC) value of 1.25 ppm/°C. This level of stability is highly competitive, notably surpassing the thermal performance of prior integrated solutions. Furthermore, when compared to works that implement combinations of passive resistor, the SC resistor holds a distinct advantage in its intrinsic dynamic tunability, offering the flexibility to electronically adjust the resistance value via the switching frequency. For example, the resistance of SC resistor can be modified by using different reference clock frequency with simple frequency divider. This shows great advantage than fixed passive reference components. However it should be noticed that the switching frequency is limited to more than 10 times of system clock according to [3]. Also, since the nodes beside the SC resistor shows switching noise, the implementation of SC resistor is in fact limited to circuit where large load is present.

V. CONCLUSION

This work presents a high-stability, temperature-independent resistor utilizing the switched-capacitor (SC) structure. Leveraging the area benefits of the bilinear SC topology, the proposed design exhibits superior physical efficiency; when compared to a passive resistor counterpart fabricated in the TSMC 180 nm RF process, the SC resistor requires less silicon area. Crucially, the simulated thermal performance demonstrates a profound improvement in stability, yielding a temperature independence that is approximately 2.24 times better than that reported for leading prior integrated reference architectures.

ACKNOWLEDGMENT

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