# Wireless Power Transfer of Devices Using Non-Radiant/Radiant Structure

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*Abstract* – **This paper presents Wireless Power Transfer of Devices Using Non-Radiant/Radial Structure. Radial and non-radio-radio-type radio charging receiving station physical and layout, measurement was carried out. High-efficiency Adaptive Rectifier operating in wide receiving power range, Low-Drop-Out Voltage Regulator for rapid charging, and analog-to-digital converter for communication and power control have been developed. The core of wireless energy technology is the efficiency of RF-DC Converter. In the computer simulation results, the maximum efficiency of the radial radio charging reception was 47.19% at 0 dBm of input power and 76.23% at 11dBm. The use process is CMOS process 180nm and the chip area is 5000um X 2450um.**

*Keywords*—**Massive MIMO Wireless charging, Retroreflection beamforming, RF Energy Harvesting, Wearable device, Wireless Power Transfer**

## I. INTRODUCTION

With the recent development of the wearable market along with the fourth industrial revolution, the use of wireless power transmission has been increasing rapidly.[1] However, as ultra-close magnetic induction, magnetic induction, and co-evolutionary wireless power transmission become inconvenient, wireless charging technology is required within the user's life radius.[2] One of these alternatives is beamforming RF radio power transmission that can be transmitted at all times. Research on charging devices based on long-distance wireless power transmission is already being actively carried out with businesses at the center. A practical and new breakthrough is needed in the convergence of beamforming RF radio power transmission, which enables permanent power transmission, with existing magnetic induction and resonant wireless power transmission technologies. Due to the lack of research for power transmission to devices in mobile environments, the biggest problem of wearable device usability will be solved, contributing to the revitalization of the wearable device industry in a recession. In this paper, we aim to develop an unconstrained multi-modal energy transmission and receiving technology of the convergence of Retro-Reflective based distributed collaborative microwave energy supply technology (DC-MPT) and Non-Radiant Radio Power Transmission (NR-WPT) that can provide power remotely at all times, and a wearable device platform that can optimize power viability by utilizing it.[3] Retro-Reflective beamforming is a method of analyzing pilot signals received by each antenna and, accordingly, constructing a power beam concentrated at a specific location. DC-MPT disperses a number of transmitters that radiate Microwave, so that energy is transmitted mutually, overcoming stability of the human body and improving transmission efficiency of transmission.[4] NR-WPT has magnetic induction and magnetic resonance methods in such a way as to utilize magnetic fields formed in the local field by time-varying currents applied to transmission coils. In this study, non-radio-type radio power transmission technology, which can be wirelessly charged in a very close environment with mains power, and radial-based beamforming wireless power transmission technology, which provides energy remotely at all times with a negative power source, were studied.

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## II. DESIGN METHODOLOGY

### *A. Top Block Diagram*

The Fig. 1. shows the structure of high efficiency Rectifier for non-radiation and radial rapid radio charging. Includes high-efficiency Adaptive Rectifier operating over a wide range of received power, Low Drop-Out Voltage Regulator for rapid charging, analog-to-digital converter, and Interface for non-radio communication. Analog PLLs include Divider, CP, PFD, and FRAC-N. LDO is built into VCO, PLL and PA. In order to reduce In-rush Current, it occurred below 131mA by applying Soft-Start Scheme.

The output current can be detected by copying the current of Path MOS, and it is designed as a Current Limit circuit to prevent over-current. Analog-to-digital converter was designed with a 12bit SAR ADC structure using Dual Sampling. Convert information such as Rectifier voltage and current to Digital Code through Multi Input MUX. Set each input voltage to a range of 0-1.8V with resistance distribution inside the MUX and perform a 0.2V Boosting through the Input Offset Block for Conversion. It has a

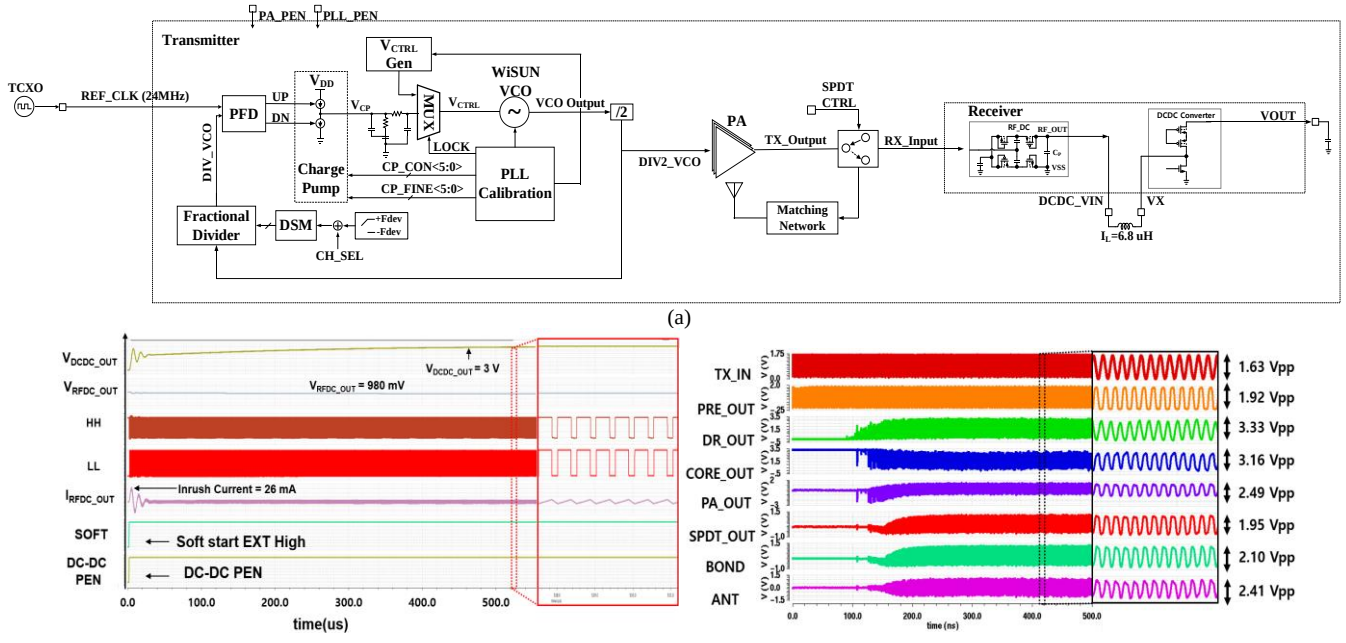
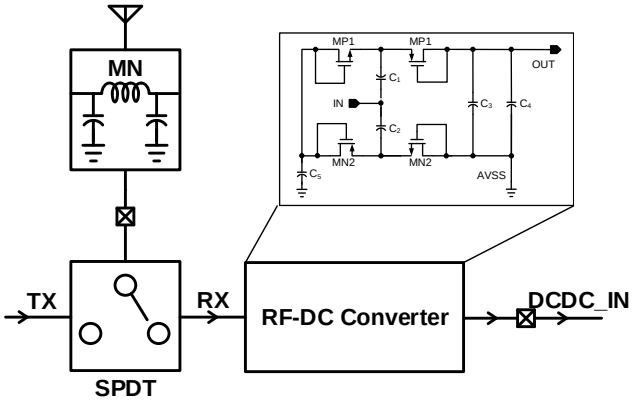


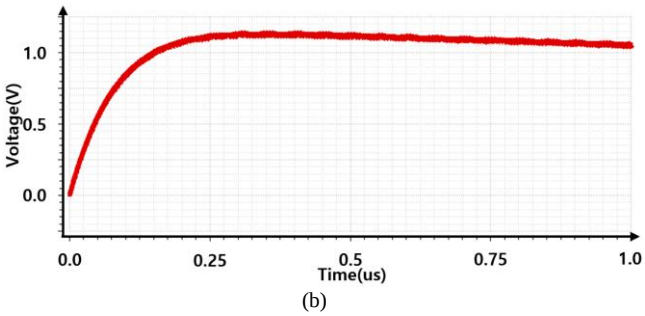

Fig. 1. Top block Diagram; (a)Top block diagram including PA, SPDT, RF-DC Converter
(b) Top Simulation result about Rx (c) Top Simulation result about Tx

sampling rate of 250 kS/s by conducting a Conversion for 60 clocks with a CLK of 15 MHz. The clocks of each bit are assigned differently so that the sampling cap and CDAC can be completely set. Non-radio charging interface has developed an interface applicable to wireless charging communication protocol. It actively adjusts the value of impedance modularization according to the receiving power to operate efficiently. Fig. 1.(b) and (c) shows Top block simulation results Rx and Tx. RF-DC Converter Input Power conducted a simulation by connecting a 1 MΩ load resistance to the DC-DC Converter at 0 dBm. After operating the initial BG/LDO, if the LDO voltage is set at 1.7V or higher, the DC-DC HH voltage is attached to High, and the output of the RF-DC Converter is increased. Fig. 1.(c) shows Top Simulation result about Tx. PA Top simulation was conducted and 11.5 dBm output was checked when the PLL output applied 1.63 Vpp to the input in the SS case.

### *B. RF-DC Converter*

The Fig. 2.(a) shows an RF-DC Converter, a radial radio-power receiver. SPDT acts as a control bit. Radial radio power receivers can handle high power over 0 dBm from low input power below 0dBm. Because receiving high power greater than 0 dBm is sufficiently large, the RF-DC Converter was configured in parallel to minimize the Production Loss. The RF-DC Converter shear Impedance matching stage minimizes the energy loss caused by the frequency being turned off, enabling maximum power transmission. The Fig. 2.(b) shows the output voltage of the RF-DC Converter at 2.4 GHz, 0 dBm. S11=-34 dB and the output voltage is 1.0V.




### *C. Step-Up DC-DC Converter*

The Fig. 3. shows a circuit diagram of the Step-Up DC-DC Converter. The input voltage is 0.5 to 3V and 3V is output. In order to reduce the component size, switching Frequency is set to 2 MHz. The DC-DC Converter output voltage is normally output at 3V by configuring Feedback Loop, and load current=3mA, the efficiency at this time

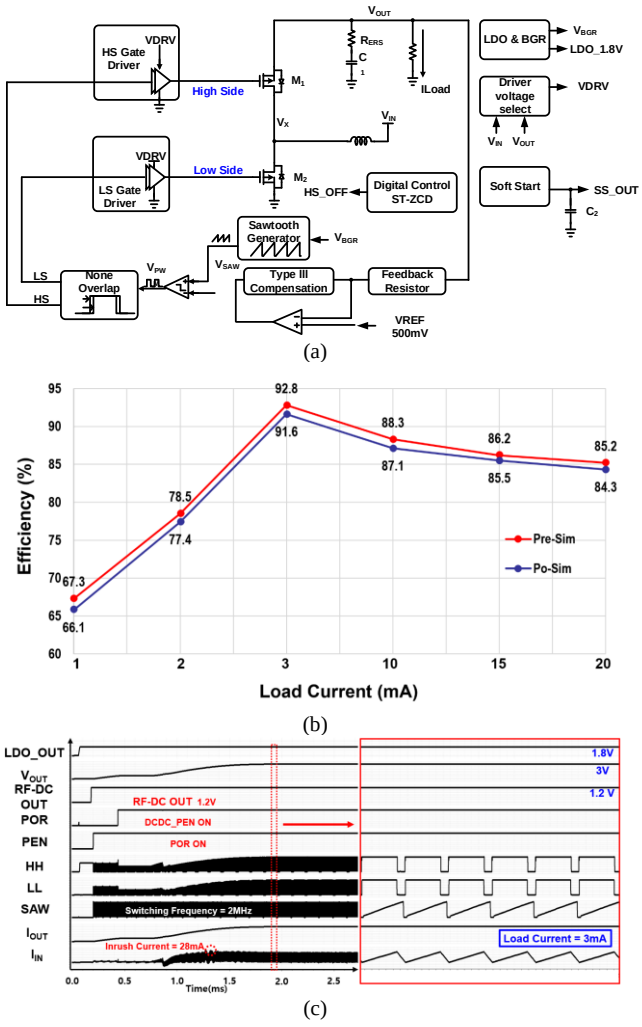



Fig. 3. Step-Up DC-DC Converter; (a) DC-DC Schematic (b) Efficiency of DC-DC Converter by Load Current (c) Top Simulation result of Step-Up DC-DC Converter

is 92.8% in Fig. 3.(b). To increase the efficiency of dc-dc converter, it is designed to operate at 3 to 10 mA as light-load. Operates by receiving 0.6 to 1V output from the RF-DC Converter as input. It has one voltage feedback loop, obtains the difference between the output voltage and the reference voltage ($V_{ref}$) through the Error Amplifier, and then re-regulates the output voltage through the Pulse Width Modulation (PWM) control.

The advantage of Voltage mode is that it has a feedback loop, which can be easily. In addition, large amplitude ramp wave form enables the use of high noise margin, which allows the system with multiple outputs to have better output regulation characteristics, but it configures feedback loops by using error amplifiers and viewing only output voltage. It has a disadvantage that the response time for line / load changes is large. In addition, buck converter adds two poles in the Power stage, so control loop must compensate by creating a low frequency domain-pole roll-off or zero of the type3 compensation. And the loop gain varies depending on the input voltage, making the composition of the reinforcement loop complex.

If the voltage is output only with the main path as in the conventional structure, the switch size of the core is so large that the resistance value of the MOS is very small, the current flowing during the initial operation must be very large, and it can cause fatal problems in circuit operation. The current is called the Inrush current, In the proposed structure, Reduced using driver Voltage Select Block. This block outputs a VDRV voltage by comparing the input voltage with the output voltage. This voltage prevents rapid current flow to the Power MOS by allowing it to operate with the gate driver's VDD. In addition, Zero Current Detector (ZCD) was used to block reverse current by low side FET, and the suggested ZCD was digitized to reduce consumption current to increase efficiency. ST-ZCD detects switching nodes without attenuation generated by the sensing circuit.

### *D. Phase-Locked Loop*

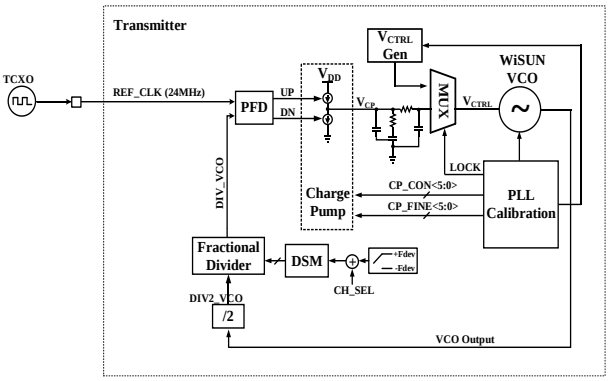



Fig. 4. Top Block Diagram of Proposed Phase-Locked Loop

Fig. 4. shows the top block diagram of proposed delta-sigma (Δ-Σ) fractional-N phase-locked loop (PLL). It is a charge pump PLL architecture, which is commonly used in communication today. The fractional divider output DIV_VCO is compared to the reference clock frequency which is 24 MHz by the phase frequency detector (PFD), which generates pulses proportional to the phase difference between the two input signals. If reference frequency lags DIV_VCO, UP pulses are generated and current is injected into the passive loop filter by the charge pump, increasing the control voltage of voltage controlled oscillator (VCO) and thus the frequency of VCO. If reference frequency leads DIV_VCO, DN pulses are generated and consequently the frequency of VCO is decreased.

The output frequency range of the proposed VCO is 2.18 GHz to 3.15 GHz in order to generate 2.4 GHz in the closed PLL loop. PLL calibration block is added for coarse frequency tuning and adjusting the charge pump current.

Using a fractional frequency divider which counts (N+k/M) voltage controlled oscillator (VCO) cycles each reference period, where N, k, M are integers and $0 \leq k < M$, can lower the quantization noise by $20 \times \log 10M$-dB.

The VCO employs the push-pull Class-C VCO. To get the maximum theoretical phase noise figure of merit of the original Class-C VCO, the circuit displays the same advantages that, in some cases, make a complementary LC-tank oscillator (employing both NMOS and PMOS

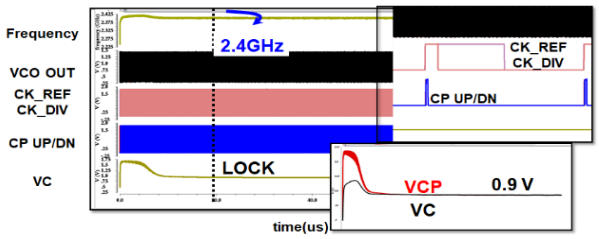



Fig. 5. Simulation Results of Proposed Phase-Locked Loop

switching transistors) preferable to a single differential pair oscillator.

To reduce the power consumption and phase noise, the unit capacitance inside the capacitor banks are minimized to its minimum value while the inductor size is high as much as possible to have maximum swing with respect to the frequency range. The cap banks are binary weighted and have linear frequency behavior.

The PLL is designed in 180 nm CMOS process with the power supply of 1.8 V Fig.5. shows the simulation results of the proposed PLL. At the top of the simulation result indicates that PLL generates target frequency 2.4 GHz. Also, the output voltage of the loop filter VC saturates to 0.9 V, half of the power supply.

## III. RESULTS AND DISCUSSIONS

This proposed circuit is required is simulated in CMOS process 180nm Process and analyzed its performance through Post-layout simulation.

Fig. 6. shows the layout of a Top layout. Size is 5000um X 2450um, and VDD is 3.3V.

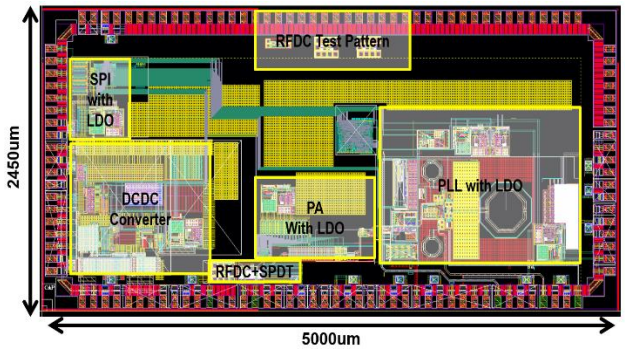



Fig. 6. Top Layout

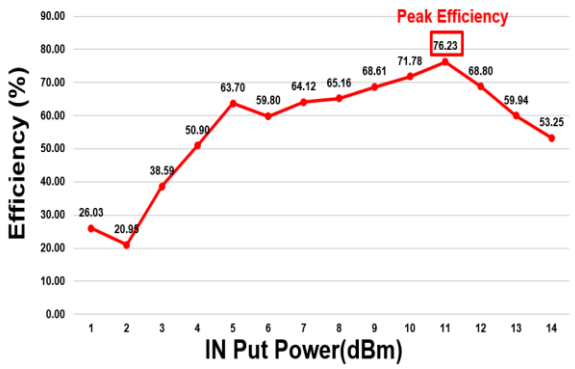
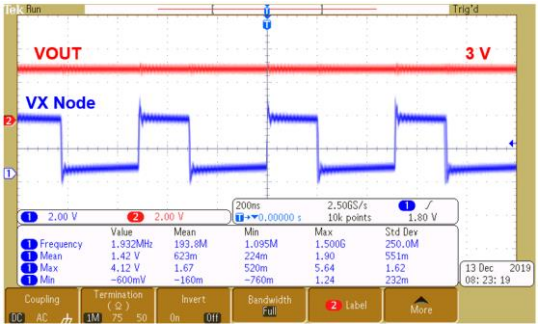


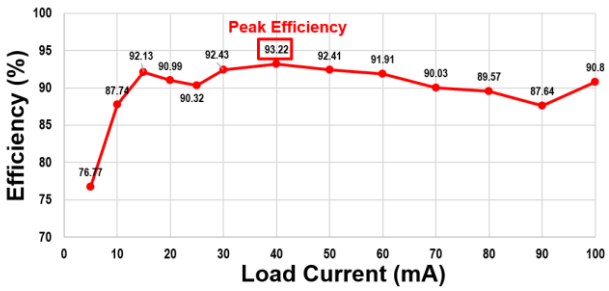

Fig. 7. 2.4GHz RF-DC Converter Efficiency

Instead of using antenna, since using RF signal generator to input the RF signal. SMA is needed and in order to input the power as much as possible. In the case of RF-DC Converter, the following equation (1) considered the pass loss condition confirmed that the highest power was produced when the 3kΩ resistance was used. The external matching component was carried out by L matching and is L=4.1nH, C=1.8pF. The maximum efficiency is 76.23% at 11dBm.

$$\eta = 10\log\left(\frac{V^2}{R}\right) + 30 \quad (1)$$



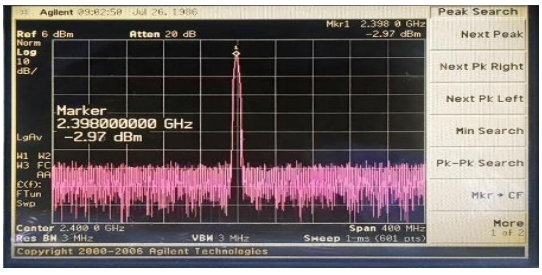

(a)



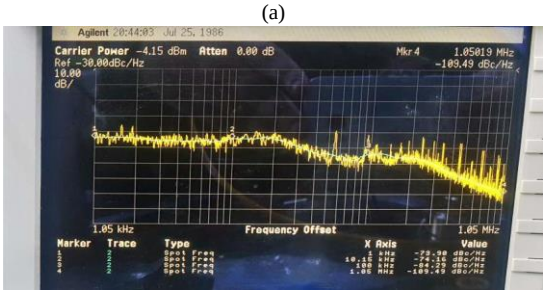

(b)

Fig. 8. DC-DC Converter measurement result; (a) Output Voltage (b) Measurement Efficiency

Fig. 8 shows dc-dc converter Measurement result. Fig. 8.(a) is when load current was 1mA, VIN=1.8V and VDD=3.3V were performed as a result of.




(a)




(b)

Fig. 9. Measurement Results of Proposed PLL; (a),(b)

Measurement results of the proposed PLL is shown in Fig .9. Fig .9.(a),(b) shows the output PLL frequency, 2.4 GHz. Figure 4. shows the measurement of the phase noise. Phase noise performance is specified in the table below.

TABLE I. Performance summary

| Parameter | [6] | [7] | [8] | This work |
|---|---|---|---|---|
| **Technology** | 130 | Off-chip | 180 | 180 |
| **Frequency** | 0.92 | 5.8 | 0.43 | 2.4 |
| **Die Area($mm^2$)** | 0.186 | N/A | 0.017 | 12.25 |
| **EH source** | RF | RF | RF | RF |
| **Sensitivity** | -16.8 | -20 | -17 | -20 |
| **Peak PCE** | 30 | 47 | 51.5 | 76.23 |

TABLE II. Cerrent Consumption

| Offset Freq (Hz) | 1 kHz | 10 kHz | 100 kHz | 1 MHz |
|---|---|---|---|---|
| **Measurement (dBc/Hz)** | -73.9 | -74 | -84.29 | -109.49 |

## IV. CONCLUSION

The biggest problem with mobile/wearable devices is charging.[5] Various methods of wireless power transmission are being proposed as measures for this purpose. Research on charging devices based on remote wireless power transmission is actively being carried out with foreign companies at the center.

In this paper, the method of radio power transmission over RF is presented. The proposed RF radio power transmission used CMOS Process 180nm process, and the chip area is 5000um x 2450um. Efficiency is paramount in RF-DC Converter. The external impedance matching group was designed to produce maximum efficiency at 2.4 GHz frequency, resulting in 76.23% efficiency at 2.4 GHz. The DC-DC Converter receives a voltage from the RF-DC Converter and converts it to 3V. There are still many problems to be solved in the proposed technique. However, it is expected that this technology will solve charging problems that occur from various devices.

## ACKNOWLEDGMENT

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## REFERENCES

[1] A. Shirane et al., “A 5.8 GHz RF-powered transceiver with a 113 μW 32-QAM transmitter employing the IF-based quadrature backscattering technique,” in Proc. IEEE Int. Solid- State Circuits Conf., Feb. 2015, pp. 248–250.

[2] Mattins. G.C, Urso. A, Mansano. A, Liu. Y. Serdijn. W. A., “Energy-Efficient Low-Power Circuit Techniques for Wireless Energy and Data Transfer in IoT Sensor Nodes”, arXiv preprint arXiv:1704.08910, 2017.

[3] Danial Khan, Seong Jin Oh, Khuram Shehzad, Muhammad Basim, Deeksha Verma, Young Gun Pu, Minjae Lee, Keum Cheol Hwang, Youngoo Yang, and Kang-Yoon. Lee, "An Efficient Reconfigurable RF-DC Converter With Wide Input Power Range for RF Energy Harvesting" IEEE Access, Vol. 8, pp.79310-79318, Apr. 2020

[4] Shinohara,N,:*Wireless Power Transfer bia Radiowaves*, Wiley, 2014.

[5] Sung Jin Kim, Dong Gyu Kim, Seong Jin Oh, Dong Soo Lee, Young Gun Pu, Keum Cheol Hwang, Youngoo Yang and Kang Yoon Lee, "A Fully Integrated Bluetooth Low-Energy Transceiver with Integrated Single Pole Double Throw and Power Management Unit for IoT Sensors," MDPI Sensors, Vol. 19, No. 10, pp. 2420-2443, May. 2019

[6] Zohaib Hameed et al. ″Hybrid Forward and Backward Threshold Compensated RF-DC Power Converter for RF Energy Harvesting″, IEEE JOURNAL ON EMERGING AND SELECTED TOPICS IN CIRCUITS AND SYSTEMS, VOL. 4, NO. 3, Sep. 2014

[7] Abdellah Taybi et al., ″Design of A New 5.8 GHz RF-DC Rectifier Structure for Wireless Power Transmission″, 2017 International Conference on Wireless Technologies, Embedded and Intelligent Systems (WITS), April, 2017

[8] M. H. Ouda, W. Khalil and K. N. Salama, "Self-Biased Differential Rectifier With Enhanced Dynamic Range for Wireless Powering," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 64, no. 5, pp.

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