Design and Optimization of Centimeter-Scale Long-Reach On-Chip Interconnect for Wafer-Level Computing

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Abstract **- This paper investigates two on-chip interconnect structures, a single-metal (Single M9) and a vertically stacked (M9/M8), for 100 Gb/s, 20mm links in Wafer-Level Computing (WLC) or Wafer-Scale Integration (WSI) systems, targeting an insertion loss below -15 dB at 25 GHz. Counterintuitively, 3D EM simulations reveal that the simpler single M9 channel is superior, achieving a -14.5 dB insertion loss, while the stacked structure exhibits a worse loss of -16.4 dB. This performance inversion is attributed to the dominance of dielectric loss over conductor loss in the stacked structure at high frequencies. System-level link simulations verify this finding, showing the single M9 channel achieves an open 100 Gb/s PAM-4 eye with a fixed FFE, a condition under which the stacked channel fails. This work highlights that high-frequency interconnect design involves a complex trade-off, demonstrating that a holistic analysis of both conductor and dielectric loss mechanisms is critical for achieving a truly optimal solution.**

Keywords**—Wafer-Level Computing (WLC), On-chip Interconnect, Signal Integrity, Insertion Loss, PAM-4, Skin Effect**

I. INTRODUCTION

Modern computing technology, driven by advancements in artificial intelligence (AI) and high-performance computing (HPC), has made high levels of computational capability indispensable. However, the slowdown of transistor scaling and the power and physical limitations of monolithic chip architecture are becoming prominent. In particular, the "Memory Wall" problem, which arises from the data movement between processors and memory, has become a critical bottleneck that hinders overall system performance.

As an innovative paradigm to overcome these limitations, Wafer-Level Computing (WLC [Fig. 1]) or Wafer-Scale Integration (WSI) technology [1]-[4], which integrates an entire wafer into a single massive processor, is gaining attention. WLC is a concept that utilizes a whole single wafer as one giant chip, employing a standard 300mm (12-inch) silicon wafer as a single computational unit. Consequently, to functionally connect the numerous distributed cores, memory, and I/O blocks across the entire wafer and to enable cohesive system operation, long-distance interconnects exceeding 2 cm are structurally required. A Wafer-Level Chip is not merely large in size; it is based on a massively parallel computing architecture that integrates hundreds of thousands to millions of cores and large-scale distributed SRAM.

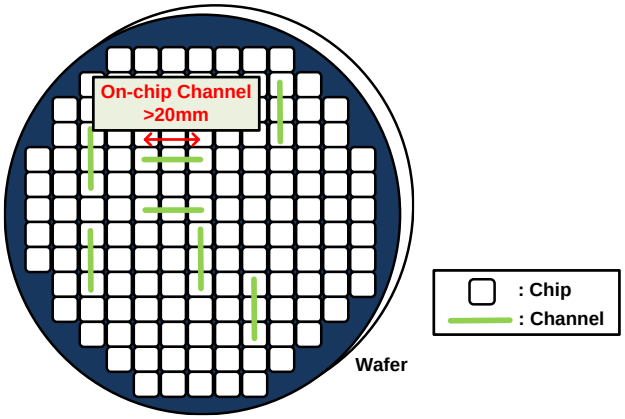

Fig. 1. Long-reach on-chip interconnects for Wafer-Level Computing (WLC) systems [1]-[4].

Therefore, these interconnects must support data rates of 100 Gb/s or higher. Traditional on-chip interconnect solutions usually deal with channel reaches of a few millimeters [5]-[11]. However, long-distance on-chip interconnect channels reaching 2 cm in length suffer from the problem of severe insertion loss (IL). This paper aims to propose the channel conditions and configuration for long-distance on-chip interconnects, which govern the performance of WLC systems, based on the 28nm CMOS process. This paper presents an in-depth comparative analysis of two contrasting channel structures in a 28nm CMOS process: a conventional single-metal layer (Single M9) structure and a vertically stacked (M9/M8) structure expected to minimize conductor resistance. While the stacked structure is intuitively predicted to be superior due to its larger cross-section, 3D electromagnetic (EM) simulations reveal a critical, counter-intuitive phenomenon: at the 25 GHz high-frequency band, the surge in conductance (G), representing dielectric loss, proves more dominant than the benefit of reduced resistance (R).

Consequently, this study establishes that for long-distance interconnect design in WSI systems, the structurally simpler single M9 channel paradoxically exhibits superior loss characteristics in the target high-frequency band. In Chapter

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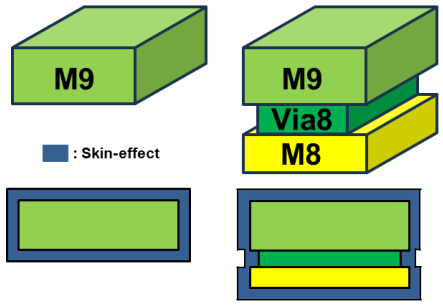
Manuscript Received Sep. 24, 2025, Revised Oct. 29, 2025, Accepted Oct. 31, 2025

II, we clarify the complex trade-off between conductor and dielectric loss and propose an optimal design methodology that satisfies both performance and power efficiency goals. Chapter III presents supporting experimental results using electromagnetic simulations. Chapter IV concludes this paper.

II. DESIGN METHODOLOGY

A. Channel Structure Selection and Comparative Analysis



(a) (b)

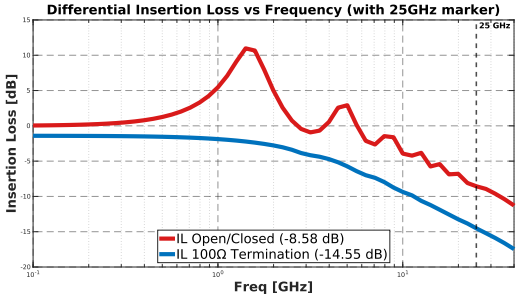
Fig. 2. Structures of the 20mm-long on-chip channel using (a) only M9 layer and (b) stacked M9/M8 layer.

In a Wafer-Level Computing (WLC) environment, a 2cm long-distance interconnect must be analyzed as a lossy transmission line rather than a simple RC circuit. In the high-frequency range, up to the 25 GHz Nyquist frequency of a 100 Gb/s PAM-4 signal, conductor loss due to resistance (R) and dielectric loss due to the conductance (G) of the insulator are equally important factors that determine channel performance. Therefore, designing a low-loss channel with an insertion loss below our target of -15 dB requires optimizing the structure to minimize both loss mechanisms. This paper analyzes the single M9 structure (a) and the stacked M9/M8 structure (b), as shown in Fig. 2.

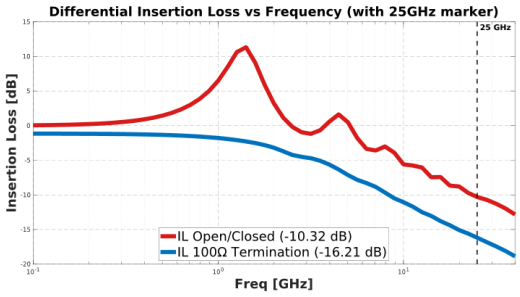
First, we analyzed the baseline performance of a 20mm differential channel using the standard design approach for on-chip interconnects: the top-most single metal layer (M9 in the 28nm process). As shown in Fig. 3(a), the insertion loss of the optimized single M9 channel is -14.5 dB at 25 GHz according to the EM simulation. This encouraging result demonstrates the viability of the channel for WLC and meets our target specification of -15 dB with a clear margin.

Next, to investigate the potential for further performance improvement, we explored an alternative structure designed to reduce conductor loss drastically. Based on the hypothesis of minimizing high-frequency resistance (R), we designed and simulated a vertically stacked M9/M8 structure, where multiple vias connect the M9 and the underlying M8 metal layers to act as a single, thicker conductor. As illustrated in Fig. 2(b), this structure was expected to reduce resistive loss by significantly increasing the effective cross-sectional area.

However, the 3D EM simulation results yield an unexpected outcome: at 25 GHz, the simulated insertion loss of the stacked M9/M8 channel is -16.2 dB, which is 2 dB worse than the single M9 channel and fails to meet the target specification of -15 dB. The root cause is that the benefit of



(a)



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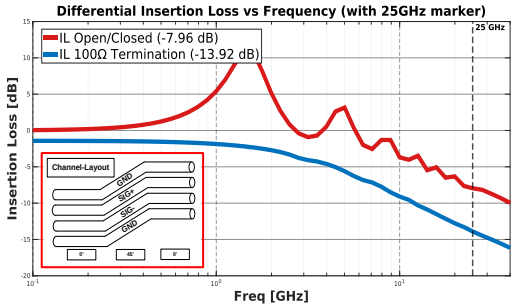


(c)

Fig. 3. Simulated insertion loss of a 20mm channel using (a) only M9 layer, (b) stacked M9/M8 layer and (c) only M9 channel with 45-degree bending.

reduced resistance (R) was outweighed by the sharp increase in capacitance (C) due to structural change. Moreover, the increased dielectric loss (G) due to taller interconnect degrades the total loss factor at high frequencies.

And, in typical Wafer-Level Chip-Scale (WLC) systems, connections to external bumps inevitably introduce local bends in the M9 metal routing due to on-chip layout constraints. These bending sections can potentially cause impedance discontinuities, leading to increased insertion loss and signal degradation. To reflect realistic routing conditions, this work analyzed a channel structure that includes a single 45-degree bend segment along an otherwise straight differential line. The simulation results showed that the channel with a 45-degree bend exhibited no significant difference in insertion loss across a wide frequency range compared to the fully straight channel.

Through this comparative analysis, we identified that for the long-distance communication environment in WLC, the structurally simpler single M9 channel is, in fact, a superior solution over the stacked structure. Therefore, the remainder of this paper will focus on the detailed geometric optimization process for impedance matching based on this single M9 channel.

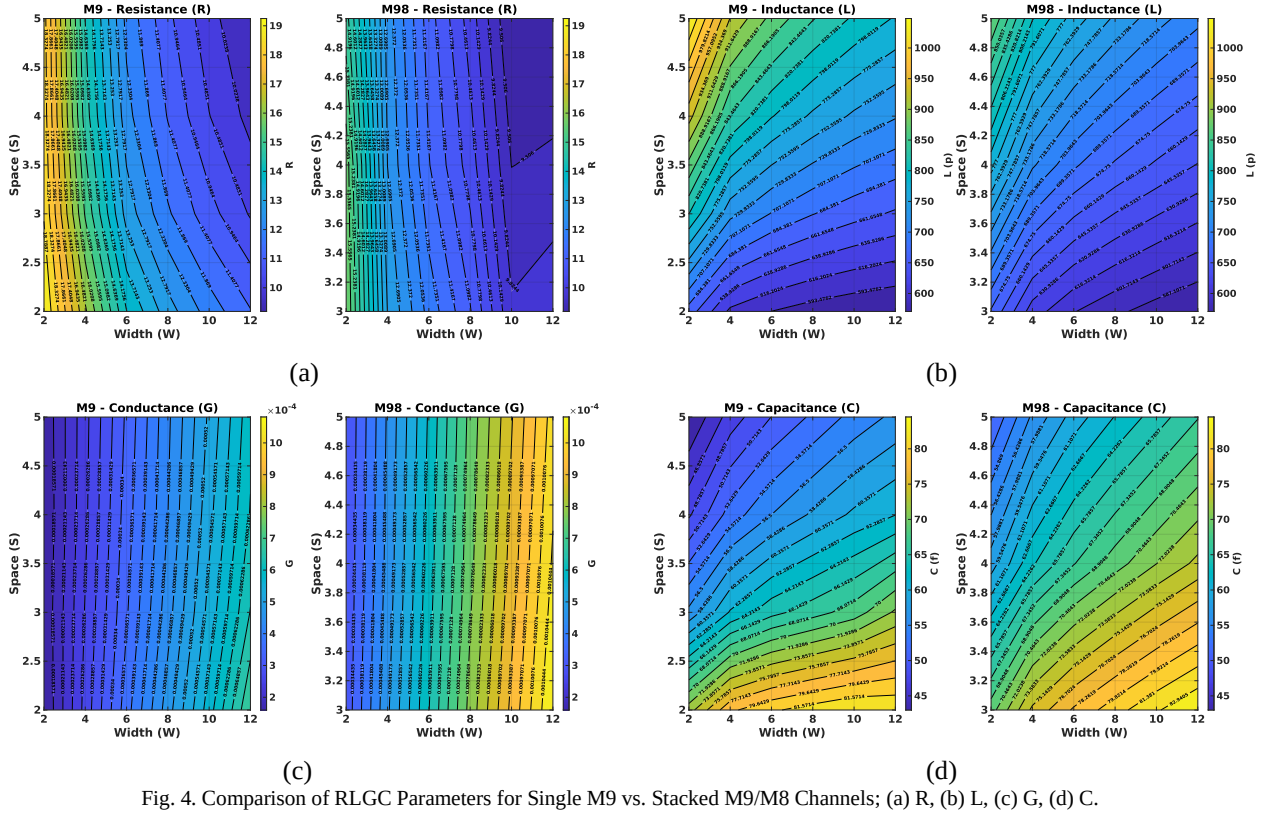


Fig. 4. Comparison of RLGC Parameters for Single M9 vs. Stacked M9/M8 Channels; (a) R, (b) L, (c) G, (d) C.

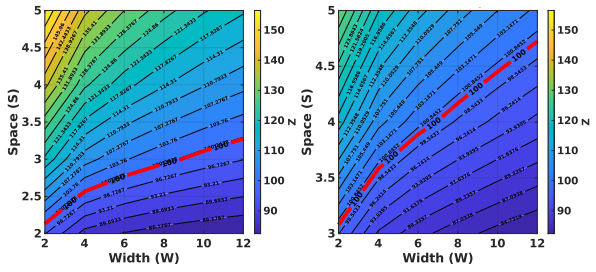


Fig. 5. 100 Ω Impedance Matching Comparison: M9 vs. M9/M8 Channels based on S and W; (a)the single M9 channel, (b) the stacked M9/M8 channel.

B. Channel RLGC and Impedance Matching Analysis

A key challenge in designing 100 Gb/s long-distance on-chip interconnects is to simultaneously achieve two goals: 100 Ω differential impedance matching and minimizing insertion loss (IL). Therefore, a model that can accurately predict changes in electrical characteristics based on the channel's geometric structure is essential.

To this end, this study extracted the RLGC parameters (Resistance, Inductance, Conductance, and Capacitance) or the metal interconnect structure of a 28nm process using EMX, which is a 2.5D electromagnetic simulation tool. Based on the extracted parameters, a compact model was built to predict the impedance according to changes in the channel's Width (W) and Spacing (S).

By utilizing this model, it was possible to perform co-optimization to quickly and accurately find the optimal structure, instead of repeating EMX simulations for the entire 20mm length.

The design strategy for the channel's Width (W) and Spacing (S) to simultaneously satisfy both impedance matching and low-loss characteristics, using the RLGC model, is as follows:

- Widening the channel width (W) is the most effective method for reducing the high-frequency resistance (R) component, which directly contributes to the improvement of Insertion Loss (IL). However, as W widens, the capacitance (C) to the ground increases, causing the problem of a lower characteristic impedance (Z).
- The spacing (S) between the differential signal lines primarily affects impedance. Narrowing S strengthens the capacitive/inductive coupling between the two signal lines, which lowers the differential impedance, while widening it increases the impedance.

Therefore, the optimization process proceeds in the following systematic order. First, to minimize insertion loss, the width (W) is set as wide as possible within the limits of the process design rules. Subsequently, to compensate for the characteristic impedance (Z) that drops below 100 Ω due to the widened W, the spacing (S) is adjusted to match the target impedance of 100 Ω by referring to the impedance graph of S vs. W shown in Fig. 5. Through this approach, the optimal values of W and S that resolve this trade-off were efficiently derived. The following explains why the M9

channel has lower Insertion Loss (IL) than the stacked M9/M8 channel, based on the parameter analysis.

- Resistance (R) analysis**:** Compared to the single M9 structure, the stacked M9/M8 structure has a larger total cross-sectional area and a more extended surface perimeter for high-frequency current flow. As a result, both low-frequency and high-frequency resistance are significantly reduced. This provides a clear advantage in terms of conductor loss.
- Capacitance (C) analysis: Conversely, capacitance increases significantly in the stacked M9/M8 structure. This occurs because the M8 layer is physically closer to the underlying metal layers and the substrate, and the larger overall 3D profile of the conductor leads to an increased fringing field.
- Conductance (G) analysis: Conductance (G), which represents dielectric loss, is directly proportional to both frequency (f) and capacitance (C), as shown by the relation $G \propto f \cdot C$. Consequently, as capacitance (C) increases significantly in the M9/M8 structure, conductance (G) also experiences a sharp, proportional increase.

The comprehensive analysis described above reveals that in the high-frequency band of 25 GHz, the benefit of reduced resistance (R) from the stacked M9/M8 structure was far outweighed by the dominant effect of dielectric loss. This loss is attributed to the amplified conductance (G), which stems from the increase in capacitance (C). As a result, while conductor loss was reduced, the more significant increase in dielectric loss ultimately worsened the total insertion loss. The findings of this analysis are summarized in Table I.

TABLE I. RLGC Parameter and Insertion Loss Analysis for Different Channel Structures

	only-M9	the stacked M9/M8	Summary of reason
R	High	Low	Resistance decreases due to increased cross-sectional area and surface perimeter.
L	Baseline	Slightly Low	Slight decrease in internal inductance due to larger conductor size.
C	Low	High	Capacitance increases due to larger conductor size and proximity to lower metal layers.
G	Low	High	Increases in direct proportion to the increase in Capacitance (C).
IL(LF)	High	Low	The effect of reduced Resistance (R) is dominant.
IL(HF)	Baseline	High	The effect of dielectric loss due to increased Conductance (G) is dominant.

C. Differential 100Ω Impedance matching

To accurately evaluate the intrinsic performance of a high-speed signal transmission channel, it is essential to eliminate the effects of signal reflection through a termination that matches the channel's characteristic impedance. Figure 3 clearly demonstrates the importance of impedance matching by comparing the insertion loss of the single M9 channel optimized in this study, with and without 100 Ω differential termination.

The red curve is the response of the unterminated channel. When the channel is not terminated, signal energy is reflected at the end of the channel instead of being absorbed. This reflected wave interferes with the incident wave, causing resonance phenomena at specific frequencies, which appear as irregular peaks in the insertion loss graph. This response is a distortion caused by reflections, not an intrinsic characteristic of the channel, and therefore cannot be used as an actual performance metric.

The blue curve is the response of the terminated channel. When the channel's input and output are terminated with its characteristic impedance of 100 Ω, signal reflections are eliminated, revealing only the pure attenuation characteristics caused by the channel's physical structure (R and G components). This blue curve shows the channel's intrinsic insertion loss, which increases smoothly and predictably with frequency. The measured value of -14.5dB at 25 GHz is the final performance metric for the optimized channel proposed in this paper.

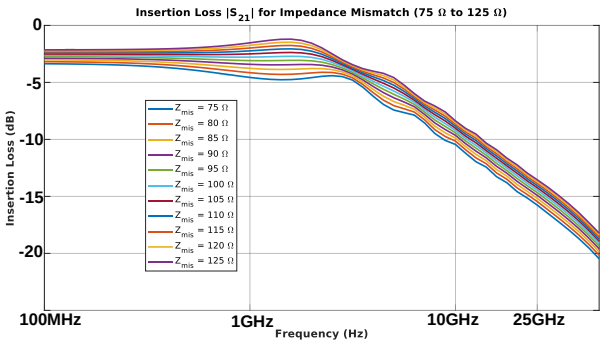


Fig. 6. Insertion Loss Caused by Impedance Mismatch from 75 Ω to 125 Ω

The purpose of the impedance optimization analysis conducted in this study is to identify the actual characteristic impedance of the WLC channel and to determine the impedance range that achieves optimal signal integrity. Figure 6 presents the differential insertion loss $Sdd21$ frequency response when the termination impedance is varied from 75 Ω to 125 Ω in 5 Ω increments. According to the differential insertion loss $Sdd21$ results in Figure 6, the optimal matching impedance of the WLC channel lies between 95 Ω and 100 Ω. Within this range, the channel exhibits the lowest loss and a flat, stable frequency response across a wide bandwidth, thereby ensuring the best signal integrity. In contrast, lower impedances such as 75 Ω cause more than 1.8 dB of additional loss, while higher impedances above 125 Ω result in irregular frequency dips. Considering that 100 Ω differential impedance is the global standard for PCB and transceiver IC designs, adopting a 100 Ω matching in the proposed WLC channel provides the most appropriate balance between optimal performance, maximum system compatibility, and practical implementation.

In conclusion, all performance evaluations of the channels presented in this paper were conducted under 100 Ω matched termination conditions to eliminate the effects of signal reflection and analyze the intrinsic loss characteristics of the channel. This approach objectively demonstrates the superiority of the proposed single M9 channel.

D. Channel Shielding

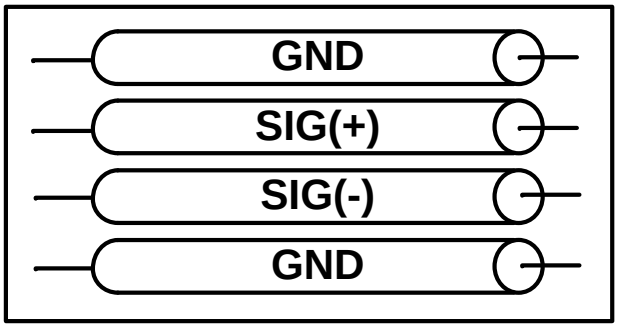
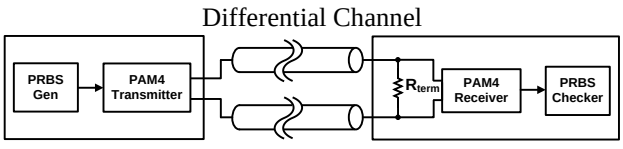


Fig. 7. Configuration of Channel Shielding

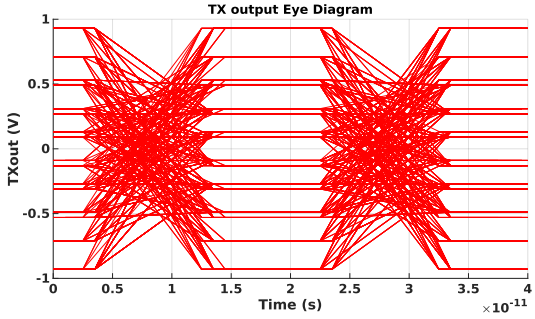
To minimize electromagnetic coupling and improve signal integrity, a ground-shielded differential channel structure was adopted. The proposed channel is implemented entirely on the M9 metal layer, consisting of a GND–SIG+–SIG—GND configuration. In this structure, the two signal traces (SIG+ and SIG–) are symmetrically placed between ground lines, forming a quasi-coplanar shield that suppresses both electric and magnetic field leakage. The ground shields serve two main purposes. First, they confine the return current within the same metal layer, effectively reducing coupling with adjacent interconnects and substrate noise. Second, they preserve the symmetry of the differential pair, thereby minimizing common-mode conversion and far-end crosstalk (FEXT). Although the single-layer shielded topology does not completely eliminate substrate coupling due to the absence of a lower ground plane, it provides a favorable trade-off between routing simplicity and signal isolation. This configuration was found to achieve stable differential impedance and improved eye-opening characteristics in transient simulations, making it suitable for short-reach wafer-level interconnect (WLC) environments.

III. EXPERIMENTAL RESULTS

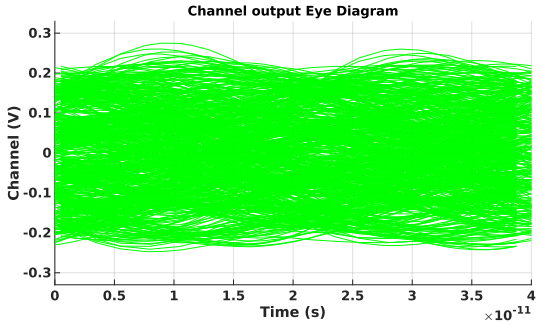


Channel Length = 20mm / R_{term} = 100Ω / RX Termination

Fig. 8. A simulation setup for 100 Gb/s PAM-4 signaling over 2cm Channel.



(a)



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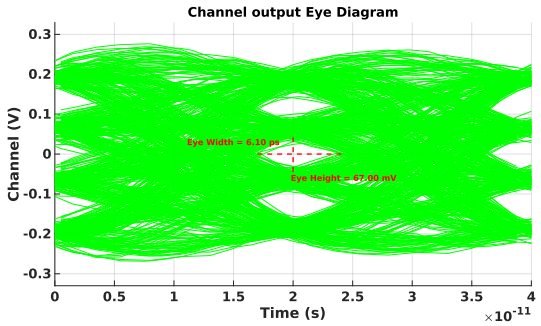

(c)

Fig. 9. Eye diagrams for the 20mm channels; (a) TX output eye (with FFE), (b) RX eye with the stacked M9/M8 channel, and (c) RX eye with M9 channel.

Previously, through frequency response (S-parameter) analysis of the channels themselves, it was determined that the optimized 'single M9 channel' exhibits superior insertion loss characteristics compared to the 'stacked M9/M8 channel' (-14.5dB vs -16.2dB). In this chapter, we perform a link simulation to verify the impact of these different channel characteristics on an actual 100 Gb/s PAM-4 data transmission system and thereby demonstrate the final system-level performance of the proposed single M9 channel. The simulation setup is as shown in Fig. 6.

A. Link Simulation Environment

A link simulation was performed to verify the system-level performance of the proposed channel structure. As shown in Fig. 7(a), at the transmitter (TX), a PAM-4 signal (25 GHz Nyquist) with a Pseudo-Random Binary Sequence (PRBS) pattern was generated for 100 Gb/s data transmission, and a Feed-Forward Equalizer (FFE) was applied to compensate for the channel's frequency response. The channel models used the respective S-parameters of the 'single M9 channel' (-14.5dB) optimized in Chapter 2 and the 'stacked M9/M8 channel' (-16.2dB) for comparative analysis.

B. Performance Verification of the Proposed Single M9 Channel

Due to its intrinsic loss and dispersion characteristics, signal recovery is impossible for a 20mm long-distance channel without an equalizer. Therefore, when an FFE was applied at the transmitter for pre-compensation of channel distortion, it was confirmed that the three eyes of the PAM-4 signal open clearly at the receiver, as shown in Fig. 7(c). The simulation results secured an eye width of

approximately 6.1 ps and an eye height of 67 mV, demonstrating at a system level that the proposed single M9 channel is fully capable of receiving 100 Gb/s data.

C. Comparative Analysis with the M9/M8 Stacked Channel

To demonstrate the practical superiority of the proposed single M9 channel, a direct performance comparison was made with the M9/M8 stacked channel, which had been considered as an alternative. To clearly highlight the difference in the intrinsic characteristics of the two channels, a fixed FFE setting that successfully recovered the signal for the single M9 channel was applied identically to both channels, and the signal quality at the receiver was analyzed. In contrast to the M9 channel, Fig. 7(b) shows the result for the M9/M8 stacked channel. As this channel has a relatively high insertion loss (-16.2dB at 25 GHz), the same FFE setting was insufficient to overcome the signal distortion. Consequently, the eye diagram remained severely distorted and in a closed state, confirming that data recovery was impossible.

This comparative result clearly demonstrates that the proposed single M9 channel has superior intrinsic characteristics compared to the M9/M8 stacked structure, allowing it to achieve the target 100 Gb/s data rate with simpler or lower-power equalization techniques. This signifies that the design can make a crucial contribution to improving the power efficiency of the entire system, a key objective of Wafer-Level Computing.

D. Impulse Response with M9 20mm Channel

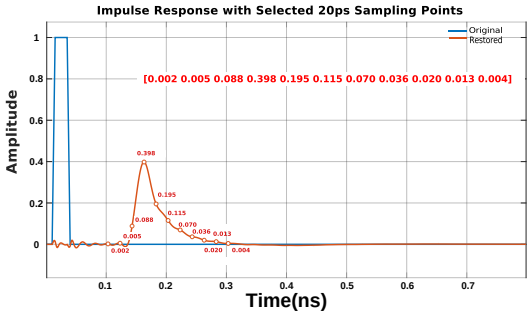

Fig. 10. Impulse Response with M9 channel.

To analyze the dynamic characteristics of the WLC channel in the time domain and provide practical insights for Tx/Rx designers, an impulse response h(t) analysis was conducted, and the results are presented in Figure 10. In the time domain, this channel can be characterized as an 11-tap finite impulse response with tap coefficient shown in the top-right corner of Fig. 10. When a unit impulse (1 V) was applied, the output signal exhibited a maximum amplitude of approximately 0.401 V, indicating an attenuation of about −7.96 dB after transmission through the channel. The propagation delay was measured to be approximately 147.5 ps, quantitatively representing the electrical length of the channel. A key feature of the impulse response is the long residual tail that persists for roughly 500 ps after the main tap, indicating the presence of significant inter-symbol interference (ISI) during high-speed operation. This observation demonstrates that the WLC channel inherently induces ISI, and therefore, Tx/Rx designers should consider implementing multi-tap decision feedback equalizers (DFE) or feed-forward equalizers (FFE). By compensating for the 500 ps ISI tail based on its amplitude and shape, such equalization schemes can effectively mitigate ISI and improve the overall bit error rate (BER) performance of the system.

E. Comparison with Prior Art

To show how well our proposed channel performs, we compared our results with one recently published study [5]. The details are summarized in Table II. The most significant differences are the channel length and data rate. The channel proposed in this study is designed for a long-distance environment of 20mm, which is 10 times longer than the 2mm channel in the reference work [5]. This better reflects the practical signal transmission environment required in Wafer-Scale Integration. Furthermore, this work targets 100 Gb/s transmission, corresponding to a 25 GHz Nyquist frequency, whereas the work in [5] has a Nyquist frequency of 14GHz. This indicates that our study addresses a channel under significantly more challenging and higher-speed conditions.

The total insertion loss of -14.5dB may seem numerically higher than the -8.5dB reported in [5]; however, this is a natural consequence of the channel being 10 times longer. To accurately compare the efficiency of the channels, the loss per unit length was calculated. The channel in this study exhibits a superior low-loss characteristic of -0.725 dB/mm. In contrast, the channel in [5] has a loss of -4.25 dB/mm, which is significantly higher per unit length. This is a key result that proves the proposed single M9 channel optimization method is highly efficient and superior for long-distance transmission.

TABLE II. On-Chip Channel Comparison Table

	This Work	ISSCC' 2025 [5]
Length	20mm	2mm
Nyquist	25 GHz	14 GHz
Insertion loss	-14.5dB	-8.5dB
Loss per unit length	-0.725dB/mm	-4.25dB/mm
Signaling	Differential	Single-ended

IV. CONCLUSION

This paper investigates and proposes an optimal channel structure for implementing a 100 Gb/s, 20mm long-distance on-chip interconnect required for Wafer-Level Computing (WLC) environments. To support the large-scale parallel processing of WLC systems, a long-distance signal path capable of low-power, high-speed operation is essential. For this study, we set a target specification of an insertion loss below -15dB at the 25 GHz Nyquist frequency.

Initially, following conventional wisdom, a vertically stacked structure combining the M9 and M8 metal layers

was considered a strong candidate to reduce conductor resistance (R). However, through in-depth analysis using 3D EM simulations and RLGC modeling, we discovered a key physical phenomenon in the high-frequency band of 25 GHz that contradicted expectations. While the stacked structure succeeded in reducing resistance, the increased capacitance (C) due to the structural change amplified the conductance (G), which represents dielectric loss, thereby worsening the overall insertion loss to -16.2dB. In contrast, a single M9 channel with an optimized geometric structure demonstrated a performance of -14.5dB insertion loss, confirming that it comfortably meets the target specification.

This finding suggests that in long-distance, high-speed interconnect design, simply reducing resistance is not the sole solution. Instead, it is crucial to accurately understand the complex trade-off between conductor loss (R) and dielectric loss (G) within the target frequency band.

In conclusion, this study highlights the importance of selecting a suitable structure considering high-frequency characteristics in designing long-distance on-chip interconnects for Wafer-Scale Integration (WSI), and demonstrates the practicality and superiority of an optimized single-metal-layer channel. For future work, the accuracy of the model could be further enhanced by fabricating a test chip and applying the proposed channel structure.

ACKNOWLEDGMENT

We thank IDEC for chip fabrication and CAD support.

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