A Design Technique for Highly Parallel Pseudo-Random Ternary Sequences Generators

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***Abstract* - This paper introduces a design technique and an optimized architecture for pseudo-random trit sequence (PRTS) generation and checking, aimed at high-speed serial communication systems such as PAM-3 transceivers. Unlike PRBS generators that rely on modulo-2 arithmetic, PRTS generation requires modulo-3 operations, which introduce additional design complexity. To address this, we propose a transition matrix-based framework for parallel PRTS generation, enabling efficient high-throughput sequence construction while remaining compatible with standard CMOS design methodologies. The circuits are designed in a 28-nm CMOS process using a standard-cell design flow. The generator achieves 72Gb/s operation at 1.89mW with an area of 0.00045 mm², while the checker consumes 1.64mW and occupies only 0.00218 μm². The proposed solution provides nearly a twofold improvement in both area and power efficiency when compared with a previous work.**

***Keywords*— Pseudo-random trit sequence (PRTS), Pseudo-random bit sequence (PRBS), Pseudo-random sequences, Built-in-self-test (BIST), Three-level pulse amplitude modulation (PAM3), Transceivers**

I. INTRODUCTION

Pseudo-random bit sequences (PRBS) have been widely employed in various system applications, such as high-speed serial link testing. With the recent advances in artificial intelligence, computing demand has significantly increased, and consequently, these sequences are required to operate at extremely high speeds. Testing links with an external bit error rate tester (BERT), however, can be impractical due to the prohibitively high cost. In contrast, when PRBS is deployed within a system, chips can be easily operated even in an automatic test equipment (ATE) environment, which improves production efficiency [1]-[12]. Fig. 1 depicts integrating both a PRBS generator and a PRBS checker enables the construction of a built-in self-test (BIST) structure, allowing straightforward verification of proper chip functionality.

Conventionally, PRBS has been used in systems employing binary or four-level modulation schemes, such as NRZ and PAM-4 [1]-[13]. A PRBS sequence of length $2^n - 1$ is typically generated using a linear feedback shift register (LFSR) with register length n and an appropriate feedback function. However, implementing a serial LFSR-based generator at very high speeds poses significant challenges due to strict timing and power constraints inherent in its serial nature. To address these limitations, prior papers have reported approaches using multiple parallel LFSRs with constant phase shifts, or LFSRs with complex phase-shifting logic [1]-[4]. Nevertheless, in such designs, the number of XOR gates and D flip-flops increases exponentially with sequence length, leading to disadvantages in both area and power consumption.

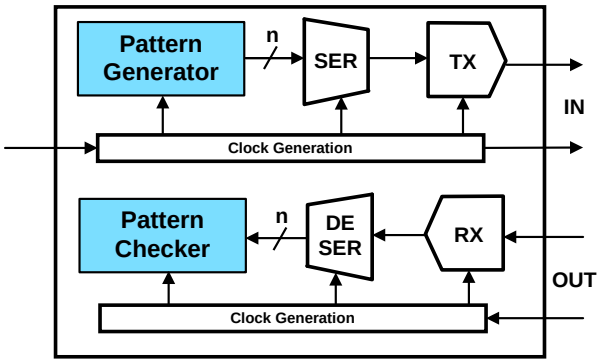

Fig. 1. Architecture of a high-speed transceiver

Another effective solution is the transition matrix-based parallelization method [5], [6], [9], [10], which computes a transition matrix T_m and implements the state transitions using XOR operations. A clear comparison of the costs among different architectures has been reported in [3]. Although the transition matrix approach is indeed an efficient method for PRBS generation, applying the same principle to PRTS generation is not optimal. This is because PRTS generation inherently involves modulo-3 operations, which lead to increased circuit complexity.

In this work, we propose an optimized parallel PRTS generator architecture by transforming a serial PRTS into its parallel counterpart. Compared with previous on-chip implementations of PRTS generators for PAM3 signaling [14], the proposed approach achieves significantly higher efficiency and faster operation. Moreover, it is fully compatible with CMOS technology and conventional digital design flows, making it a highly practical solution.

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II. TRANSITION MATRIX-BASED PARALLEL PSEUDO-RANDOM SEQUENCE GENERATION

Linear Feedback Shift Registers (LFSRs) are widely used to generate pseudo-random sequences, where the stored bits are sequentially shifted and updated according to a feedback function. While this serial implementation offers simplicity and intuitive operation, scaling it to very high data rates often requires RF-oriented circuit techniques like Current Mode Logic (CML) [5],[6],[11].

Such solutions, however, inevitably increase circuit complexity and implementation cost, which limits their practicality in scenarios demanding straightforward design and seamless compatibility with standard CMOS digital flows.

A. Transition Matrix Representation

Parallel pseudo-random sequence generation has been preferred as a practical solution that can be efficiently integrated within standard CMOS digital design methodologies. Among various approaches, the transition matrix-based method has been widely employed due to its simplicity and scalability [5], [6], [9], [10]. In this technique, the evolution of an LFSR is represented using matrix operations, which enables parallel sequence generation through systematic mathematical formulation.

If the data stored in the DFFs is represented in array form as $S_k = [S_{-1}, S_{-2}, \dots, S_{-n}]^T$, then the state transition can be described by a transition matrix T, which relates the next state S_{k+1} to the current state S_k.

$S_k = [S_{n-1}, S_{n-2}, S_{n-3}, \dots, S_{-1}, S_{-0}]^T$,

$S_{k+1} = T \cdot S_k = [S_n, S_{n-1}, S_{n-2}, \dots, S_{-2}, S_{-1}]^T$.

The simplest method to derive T is by mapping it directly from a serial PRBS generator implemented with an LFSR in Fig. 2 .

For example T and T_p for PRBS $2^7 - 1$ with m = 4 are shown in Fig. 3 (a) the serial PRBS generator for a $2^7 - 1$ sequence and its corresponding transition matrix are shown. In this example, the first row of T is obtained from the XOR feedback defined by the characteristic polynomial $1 + x^6 + x^7$. The remaining rows of T form an identity matrix, with an additional column of zeros appended, representing the shift connection between each DFF.

Fig. 3(b) shows the transition matrix T^4 in its exponentiated form. While this matrix is structurally more complicated than the original transition matrix T, it provides an efficient means of computation that enables the evaluation of four LFSR state transitions in a single step, thus streamlining the process of parallel pseudo-random sequence generation. The design results in a circuit comprising four XOR gates with a maximum fan-out of 2.

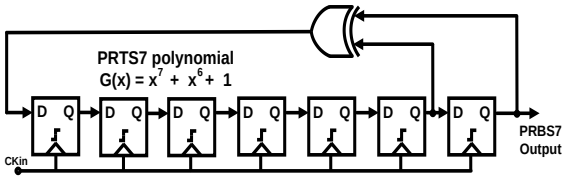

Fig. 2. Architecture of PRBS-7 generator using LFSR.

$$T = \begin{bmatrix} 0&0&0&0&0&1&1 \\ 1&0&0&0&0&0&0 \\ 0&1&0&0&0&0&0 \\ 0&0&1&0&0&0&0 \\ 0&0&0&1&0&0&0 \\ 0&0&0&0&1&0&0 \\ 0&0&0&0&0&1&0 \end{bmatrix} \quad T_p = \begin{bmatrix} 0&0&1&1&0&0&0 \\ 0&0&0&1&1&0&0 \\ 0&0&0&0&1&1&0 \\ 0&0&0&0&0&1&1 \\ 1&0&0&0&0&0&0 \\ 0&1&0&0&0&0&0 \\ 0&0&1&0&0&0&0 \end{bmatrix}$$

(a) (b)

Fig. 3. Transition matrix representation of PRBS-7: (a) basic transition. matrix T, (b) exponentiated transition matrix T^4 for parallel sequence

B. Extension of Transition matrix to PRTS

Pseudo-Random Trit Sequences (PRTS) refer to ternary sequences in which each symbol is selected from the set {0,1,2}. In principle, they can be viewed as the ternary counterpart of the widely used Pseudo-Random Binary Sequences (PRBS). Just as PRBS sequences are uniquely defined by a characteristic polynomial and are most commonly implemented using a base-2 linear feedback shift register (LFSR), PRTS sequences are instead determined by a characteristic polynomial in the ternary domain and are typically realized through a base-3 LFSR structure.

The essential difference between PRBS and PRTS arises from the type of arithmetic required during the generation process. PRBS generation involves modulo-2 operations, which restrict the sequence values to binary symbols. In contrast, PRTS generation requires modulo-3 computations, thereby expanding the symbol set to ternary values and introducing additional complexity into the implementation.

As an illustrative example, Fig. 4(b) presents an LFSR-based PRTS-15 generator with m = 16, which is derived from the characteristic polynomial $2x^{15} + x^{10} + 1$. Specifically, Fig. 4(c) shows the transition matrix that is systematically constructed by analyzing the state transitions of the PRTS-15 LFSR. This matrix-based representation provides a convenient mathematical framework for describing how the internal states evolve over time and for enabling the parallel generation of ternary pseudo-random sequences.

In the same way as parallel PRBS generation, the transition matrix T can be exponentiated to form T_p. However, unlike PRBS, which relies on modulo

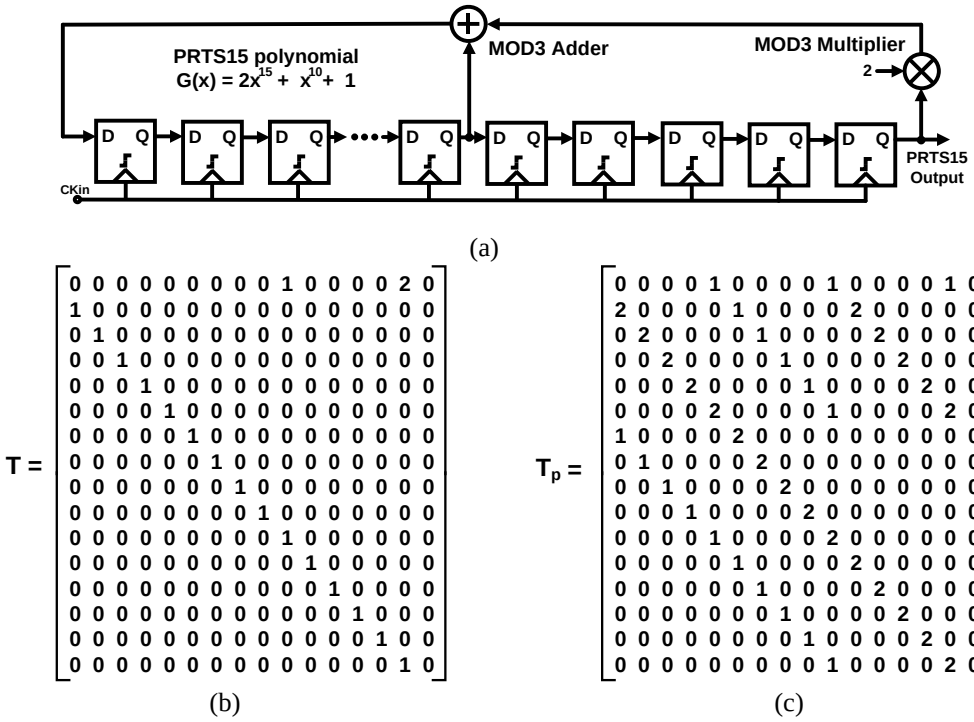

Fig 4. Transition matrix representation of PRTS15 (a) Architecture of PRTS-15 generator using LFSR. (b) Basic transition matrix (c) Exponentiated transition matrix T_p for parallel sequence generation

arithmetic where overlapping terms cancel each other out PRTS employs modulo-3 arithmetic.

This matrix can be implemented to a simple circuit and is shown in Fig. 5. The circuit incorporates 16 MOD3s and has maximum fan-out of only 4. Each modulo-3 operation is realized in logic through a combination of multipliers and adders corresponding to each matrix element. The proposed method operates correctly for arbitrary values of m and is not restricted to ternary systems. Thanks to this flexibility and efficiency, the approach serves as a highly effective solution for designing high-speed and low-complexity random sequence generators.

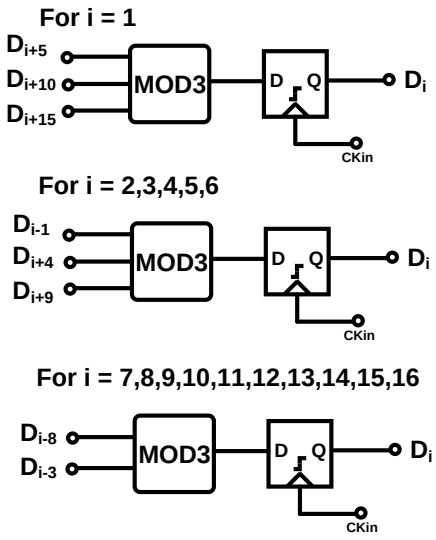

Fig. 5. Resulting circuit translated from T_p

III. MODULO 3

In the design of a PRTS generator, the modulo-3 operation constitutes a critical component. Among the various building blocks, the modulo-3 unit frequently emerges as the logical speed bottleneck and accounts for the highest power consumption. Consequently, optimizing this block is of paramount importance for achieving both high performance and energy efficiency.

The proposed modulo-3 architecture processes n input signals and, at the final stage, retains only the combination logic corresponding to values 1 and 2. The output is then derived through a table-driven approach, which simplifies the computation and reduces hardware complexity. The result can be conveniently obtained by interchanging the most significant bit (MSB) and the least significant bit (LSB) of the input. Specifically, the mapping is expressed as Dout[0]=I[1], Dout[1]=I[0]

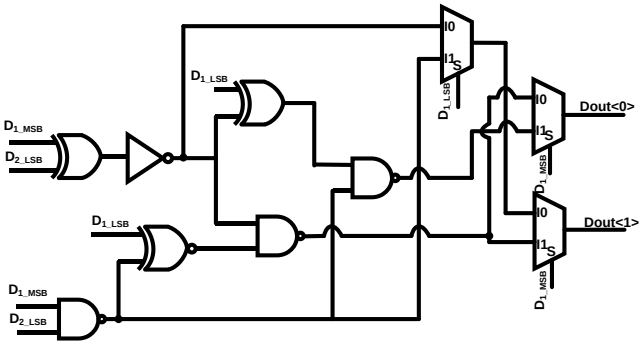

Fig. 6. CMOS modulo3 circuit

IV. PRTS CHECKER

Pattern checkers are essential for verifying the integrity of received data. The Pseudo-Random Trit Sequence (PRTS) checker is constructed using the same logic as the generator and is employed to measure the Bit-Error Rate (BER) process as illustrated in Fig. 8. The checker ensures that the received sequences conform to the characteristic polynomial defined by the generator.

Since the PRTS generator produces deterministic sequences, the subsequent pattern can be precisely predicted from the current state by applying the transition matrix calculation logic. The expected pattern is then compared with the received data.

V. EXPERIMENTAL RESULTS

Parallel PRTS generators for generating patterns of $2x^{15} + x^{10} + 1$ is designed separately using standard cell design flow in a 28-nm CMOS process as illustrated in Fig. 7. Fig. 7(a) shows a conventional on-chip PRTS generator composed of a PRBS generator and an encoder [14]. Since two binary sequence generators and an encoder are required to produce a PAM3 sequence, it occupies a relatively large chip area. In contrast, Fig. 7(b) generates a single parallel trit sequence without using an encoder, resulting in a significantly smaller area.

The procedure that reduces the number of DFF is applied. The proposed PRTS generator consumes 1.89mW when operating at 3Gs/s, occupying 0.00045 um^2 . Maximum simulated data rate is 132Gb/s when the 16-bit parallel PRTS generator runs at 5.5GHz. The power consumption of each method was measured through post-layout simulations under a 0.9 V supply voltage and 3 GHz operation, while maintaining the same bit rate across all implementations. All power values were obtained from post-layout simulations including parasitic extraction under typical PVT conditions (TT, 27°C). The reported power represents the average dynamic power of the circuit, excluding clock buffers and test interfaces. The power consumption increases linearly with the output bit rate, implying that dynamic power is the dominant component in the proposed design.

The proposed PRTS checker corresponding to the PRTS generator is designed to evaluate the bit error rate. The checker occupies an area of only 0.00218 μm² as illustrated in Fig. 8. The checker consumes 1.64mW when operating at 3Gs/s. Although many recent works have reported PAM3 transceiver designs, the implementation details of their PRTS generators have not been disclosed [15],[16]. Therefore, comparison is made with the prior work [14], in which design details are available, showing that the proposed method achieves approximately two-fold improvement in both area and power efficiency.

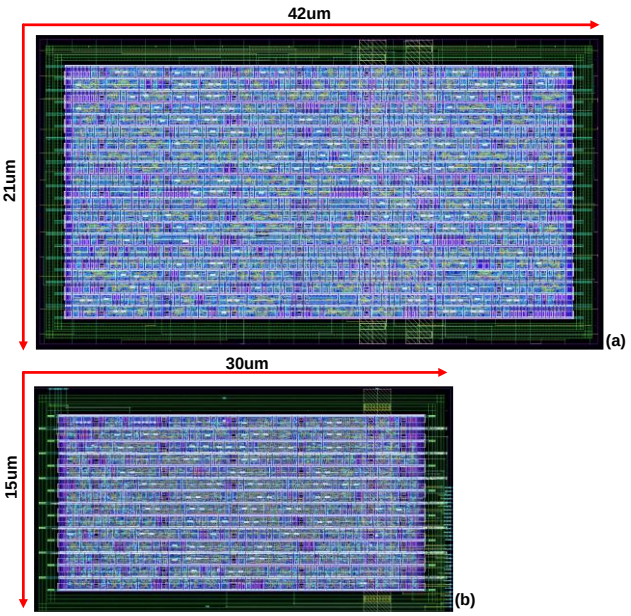

Fig. 7. Comparison layout of PRTS (a) PRTS generator w/encoder (b) proposed PRTS generator

TABLE I. Performance Summary and Comparison Table

	This work	JSSCC 2021 [14]
Method	Transition matrix	PRBS + Encoder
Process (nm)	28	28
Supply (V)	0.9	0.9
Number of Bits	16	16
Area(um^2)	0.00045	0.00088
Power (mw)	1.64 @3GHz	3.18 @3GHz
Max. Data Rate (Gb/s)	132 ($= 5.5G \times 16 \times 1.5$)	96 ($= 4G \times 16 \times 1.5$)

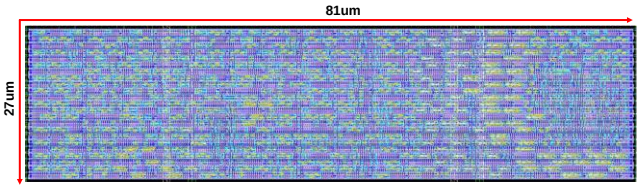

Fig. 8. PRTS checker

VI. CONCLUSION

To the best of our knowledge, this work reports the first fully realized hardware implementation of a pseudo-random Trit sequence (PRTS) generator, specifically optimized for high-speed serial interconnects. The proposed method introduces a transition matrix-driven parallel PRTS generation scheme for ternary logic systems. Furthermore, lightweight modulo-3 arithmetic blocks, including a table-based multiplexer, are incorporated to minimize complexity. Implemented in a 28-nm CMOS technology, the PRTS generator achieves a power consumption of 1.68mW at 0.9

V. These results confirm both the scalability and practicality of the proposed design, providing a strong basis for the development of future high-speed transceivers employing PAM-3 modulation.

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