A CMOS LiDAR Sensor Using Time-to-Voltage Converter for Elder-Care Applications

Somi Park, Sunkyung Lee, Bobin Seo, and Sung Min Park[a]
Division of Electronic & Semiconductor Engineering, Ewha Womans University, Seoul, Republic of Korea 03760
E-mail: 1118som@ewhain.net, snklee20@ewha.ac.kr, qhqls28@ewha.ac.kr, smpark@ewha.ac.kr

***Abstract* - This paper presents an optoelectronic readout integrated circuit (ORIC) fabricated in 180-nm CMOS technology, tailored for high-resolution, short-range LiDAR sensing applications. The ORIC pixel integrates an on-chip P^+/Nwell/Deep N-well avalanche photodiode and a CMOS transimpedance-limiting amplifier employing active feedback for low-noise performance. Then, a time-to-voltage (T2V) conversion scheme is adopted to enable precise signal quantization with minimal walk error, which is followed by a voltage-domain successive approximation register (SAR) analog-to-digital converter (ADC). This architecture is suggested to replace conventional time-to-digital converters (TDCs), thereby significantly reducing system complexity while maintaining wide dynamic range and high scalability. Post-layout simulations indicate an input dynamic range of 47.4 dB that corresponds to the detectable photocurrent levels ranging from 15 μA_{pp} to 3.5 mA_{pp}. This can be translated to a measurable distance of 31 centimeters to 4.76 meters under typical operating conditions. To the best of the authors' knowledge, this is the first attempt to substitute a TDC with a T2V-SAR ADC pipeline for LiDAR sensors, offering a compact, low-power, and scalable solution for emerging applications such as ambient-assisted living and elderly monitoring systems.**

Keywords: APD, CTLA, LiDAR, Optoelectronic, T2V, SAR ADC.

I. INTRODUCTION

With the rapid increase in the aging population, falls among elderly people have become a critical public health concern. According to the Centers for Disease Control and Prevention (CDC), one of four adults aged over 65 experiences a fall in each year, thus resulting in approximately 36 million incidents. Of these incidents, 8 million lead to severe injuries. Fall-related fatalities occur every 20 minutes, imposing a significant burden on healthcare systems and caregivers. By 2030, the elderly population is projected to reach 73 million, further intensifying medical expenditures and long-term care demands. Consequently, real-time fall detection systems are urgently required, particularly those utilizing low-power, cost-effective sensors to improve elderly safety while reducing societal costs.

Light Detection and Ranging (LiDAR) technology has emerged as a vital enabler for short-range applications, including indoor navigation, fall detection, and monitoring systems [1]–[5]. These cases demand compact, energy-efficient, and economically viable solutions, rendering LiDAR sensors indispensable for contemporary real-time detection platforms. In contrast to conventional RGB cameras that raise privacy concerns, LiDAR sensors acquire only depth information, hence making them highly suitable for non-invasive fall detection and elderly monitoring.

Most LiDAR sensor systems operate on the pulsed time-of-flight (ToF) principle, where a transmitter (Tx) emits light pulses and a receiver (Rx) detects the reflected signals. The time-interval between the START and STOP pulses is utilized to determine the distance to targets. To achieve accurate motion tracking and reliable fall detection, LiDAR receivers must handle a wide range of signal intensities while ensuring stable performance under various indoor conditions. Recently, CMOS-based optoelectronic receivers have been suggested to enable low-cost multi-channel LiDAR integration with on-chip avalanche photodiodes (APDs), enhancing system compactness and cost efficiency [6]–[10]. It is well known that conventional receivers with off-chip APDs face limitations to manage wide dynamic range signals, often leading to distortion or saturation.

This paper proposes a CMOS-integrated optoelectronic readout integrated circuit (ORIC) featuring a novel time-domain signal processing chain comprising a time-to-voltage (T2V) converter followed by a successive approximation register (SAR) analog-to-digital converter (ADC), thereby eliminating the need for complex time-to-digital converter (TDC) circuitry.

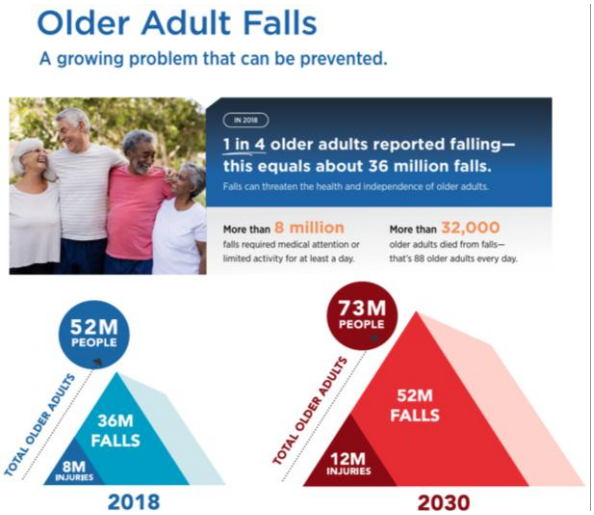

Fig. 1. Statistics of falling accidents (CDC, U.S., 2018).

a. Corresponding author; smpark@ewha.ac.kr

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The T2V converter integrates a Schmitt trigger, a capacitive charging circuit, and a peak-detect-and-hold (PDH) circuit to convert ToF delays into analog voltage levels. This approach enables wide dynamic range operations and robust detection under strong signal conditions. The SAR ADC provides high-resolution digital conversion with no need for extensive calibration algorithms. By combining T2V and SAR ADC techniques, the proposed LiDAR system achieves improved timing accuracy, making it highly suitable for short-range low-cost low-power elder-care LiDAR applications. A CMOS transimpedance-limiting amplifier (CTLA) is incorporated as the front-end circuit to ensure low-power operations. Particularly, this work focuses on the optimization of the CTLA-assisted T2V conversion to enhance time-to-voltage linearity and thereby achieve high-precision digital timing measurements.

II. DESIGN METHODS

A. CTLA and Schmitt Trigger

A low-noise CMOS transimpedance-limiting amplifier (CTLA) is presented to enhance the dynamic range of LiDAR receiver systems. It is well established that conventional shunt-feedback transimpedance amplifiers (SF-TIAs) are constrained by intrinsic gain-bandwidth tradeoffs and limited dynamic range, often necessitating the deployment of multi-stage limiting amplifiers [11]–[13]. However, this approach results in elevated power consumption and increased circuit complexity. To alleviate these limitations, the proposed design adopts a dual-feedback architecture that integrates both passive and active feedback paths, inherently enabling limiting behavior. The proposed architecture mitigates signal distortion effectively for input photocurrents exceeding 100 μA_{pp} without relying on a power-intensive limiting amplifier, thereby improving the overall energy efficiency [6].

Fig. 2 illustrates the block diagram of the proposed CTLA, which comprises an active-feedback TIA and a dual-feedback TIA (DF-TIA). The active-feedback TIA employs a variable feedback-resistor (R_{F2}) controlled by an NMOS switch that dynamically compensates for the increasing input currents, thereby extending the linear operating range. The DF-TIA is realized by using a three-stage inverter-based topology, incorporating a primary feedback resistor (R_{F1}) and a local feedback resistor (R_{F3}).

For small input currents, the input impedance and transimpedance gain are given by,

$$R_{in} = \frac{R_{F1}}{1+A_1},\ Z_T = -R_{F1}\left(\frac{A_1}{1+A_1}\right) \quad (1)$$

, where A_1 is the voltage gain of the DF-TIA.

When the NMOS switch is turned on, the effective feedback resistance is reduced to $R_F = R_{F1} \| R_{F2}$ and the input impedance and transimpedance gain are given by,

$$R_{in} = \frac{(R_{F1}||R_{F2})}{1+\alpha A_1} \quad (2)$$

$$Z_T = -(R_{F1}||R_{F2})\left(\frac{A_1}{1+\alpha A_1}\right)$$

, where $\alpha \cong 1-(g_{m7}+g_{m8})R_F$ and g_{m7} & g_{m8} denote the transconductance of the NMOS and PMOS in the feedback inverter, respectively.

This configuration achieves a ~4 dB enhancement in transimpedance gain when compared to a conventional SF-TIA, while preserving pulse integrity during amplification. Furthermore, an inverter-based output buffer (I-OB) is integrated to achieve 50-Ω impedance matching and to suppress the capacitive loading effects, therefore ensuring robust high-speed signal delivery.

Fig. 3 shows the simulated pulse response under varying input current conditions, which validates the performance of the CTLA. The CTLA reliably operates over an input current range of 1 μA_{pp} to 1.5 mA_{pp}. In addition, the Schmitt trigger maintains robust discrimination between logic '0' and '1' even for larger input currents, so that the effective dynamic range is extended up to 3.5 mA_{pp}. It achieves a transimpedance gain of 70.5 dBΩ, a -3 dB bandwidth of 1.21 GHz, the input-referred noise current density of 4.3 pA/√Hz, and a power consumption of 23.6 mW under a 1.8-V supply.

The pulse amplitude exhibits almost linear behavior for the input currents below 100 μA_{pp}, while saturation occurs beyond this threshold. This demonstrates the circuit's built-in limiting functionality so as to establish the proposed CTLA as a highly efficient analog front-end solution for short-range LiDAR applications by overcoming the limitations of a traditional SF-TIA architecture.

Fig. 4 presents the schematic diagram of the Schmitt trigger which consists of only three PMOS and three NMOS transistors, forming a compact and efficient implementation. Despite its simplicity and the use of minimally sized transistors, the circuit functions effectively as a regenerative latch.

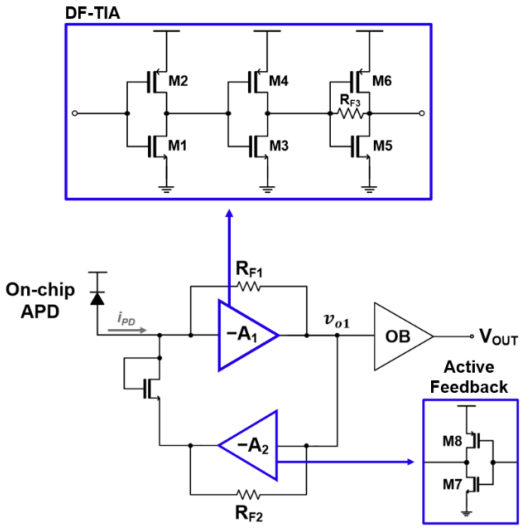

Fig. 2. Schematic diagram of the CTLA circuit.

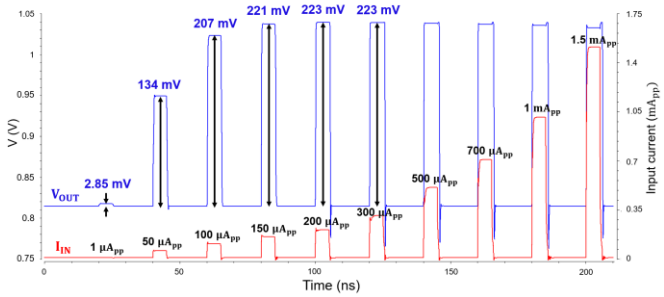

Fig. 3. Post-layout simulated pulse response of the CTLA.

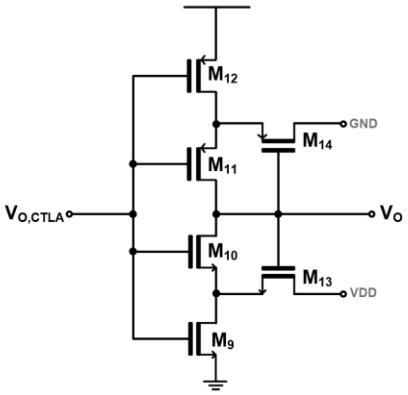

Fig. 4. Schematic diagram of the CMOS Schmitt trigger.

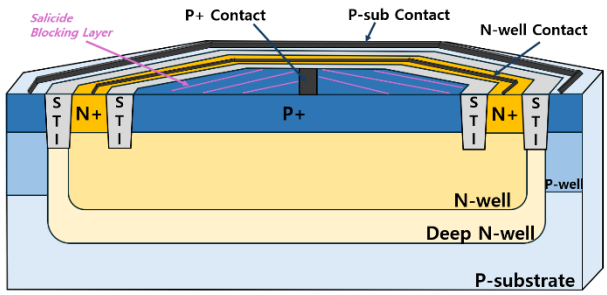

Fig. 5. Cross-sectional view of a P^+/NW/DNW APD.

Upon receiving an input signal (i.e., the CTLA output), the operation of transistors M_9–M_{12} depends on the input logic level. When either M_{13} or M_{14} is activated, these devices act as switching elements, restoring the signal to a full-swing logic '0' or '1'. The combined CTLA and Schmitt trigger accommodates the input dynamic range of 15 μA_{pp} to 3.5 mA_{pp}, ensuring that the subsequent stage receives well-defined binary signals.

B. On-Chip P^+/NW/DNW APD

Fig. 5 illustrates the cross-sectional structure of the monolithically integrated CMOS P^+/N-Well/Deep N-Well (P^+/NW/DNW) avalanche photodiode (APD), where avalanche multiplication is initiated by hole-generation at the P^+/N-Well junction [7]. This configuration effectively suppresses diffusion-induced currents from the P-substrate, resulting in enhanced responsivity and broad bandwidth. To mitigate the edge breakdown and ensure uniform electric field distribution at the junction periphery, shallow trench isolations (STIs) are employed, thereby extending beyond the depth of the P^+/N-Well junction and functioning as a guard ring. This technique, however, might introduce a design tradeoff with a reduced APD responsivity.

To alleviate this degradation, the DNW is incorporated to limit hole diffusion into the P-substrate, therefore improving sensitivity to near-infrared (NIR) wavelengths. Moreover, the potential barrier formed between the DNW and the P-substrate effectively blocks the photocurrent generation within the substrate region. For optical access, the P^+ source and drain regions are covered with a salicide-blocking layer, while the P^+ contacts remain exposed to prevent the increased contact resistance due to the silicide formation process [8]. Besides, the area of the P^+ node must be carefully optimized because an excessively large diffusion area can adversely affect the device responsivity [9].

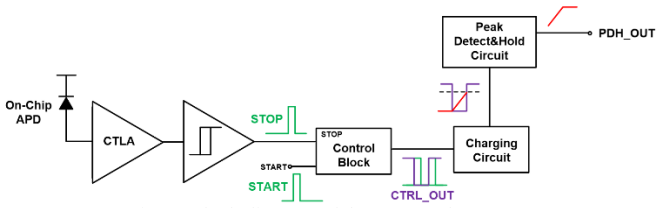

Fig. 6. Block diagram of the proposed ORIC.

C. Optoelectronic Readout Integrated Circuit (ORIC)

The CTLA integrated with an on-chip APD is utilized as the front-end circuitry for the T2V converter. Fig. 6 shows the block diagram of a single receiver cell, which comprises a CTLA and a T2V conversion stage [10]. The operational flow of the single-cell T2V circuit is as follows. Initially, the on-chip APD generates a photocurrent, which is then converted into a voltage signal by the CTLA. This voltage output is subsequently processed by a Schmitt trigger, which produces a well-defined digital pulse with distinct logic '0' and '1' levels.

Compared to conventional latch circuits, the Schmitt trigger offers a lower power consumption and a smaller footprint due to its compact MOSFET-based implementation. The output of the Schmitt trigger is utilized as the STOP signal for the T2V block, whereas the START signal is derived from the Tx reference. A control block detects the rising edges of both START and STOP pulses to produce the CTRL_OUT signal that remains low during the time-interval between the START and STOP events and remains high otherwise.

An integrator-based charging circuit is employed to perform charge accumulation exclusively during the low phase of CTRL_OUT signals. The resulting output voltage corresponds to the duration of the time interval, thereby enabling accurate time-domain measurements.

The output of the charging circuit is routed to a peak detect and hold (PDH) stage, which captures and stabilizes the peak voltage for improved temporal accuracy and readout reliability.

D. CADC (Combined TDC)

Fig. 7 illustrates the block diagram of the complete ORIC, which comprises a CTLA, a Schmitt trigger, a T2V converter, and a SAR ADC. In this configuration, the output signal of the Schmitt trigger serves as the STOP pulse, while the START signal is routed through the T2V converter to define the time-interval. The output of the T2V converter is applied to the input of the SAR ADC's comparator, where it is compared against the successive reference voltages to perform analog-to-digital conversion and hence to yield the corresponding binary codes. This complete converter architecture (CADC) facilitates high-resolution, low-power time measurements, hence rendering it highly suitable for LiDAR sensors and other precision timing applications. Fig. 8 displays the layout of the ORIC with the core occupying an area of 143 × 117 μm^2.

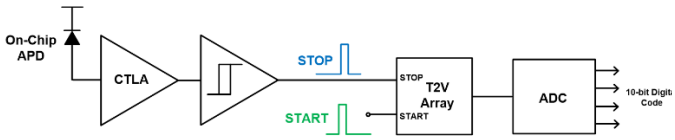

Fig. 7. Block diagram of the proposed CADC system.

III. POST-LAYOUT SIMULATION RESULTS

Fig. 9 presents the post-layout simulation results of the proposed ORIC, which verifies the effective conversion of time-intervals between the START and STOP pulses into the corresponding voltage levels. It reliably processes the input photocurrents ranging from 15 μA_{pp} to 3.5 mA_{pp}, where the maximum input current of 3.5 mA_{pp} corresponds to the minimum detectable range of 31 cm.

Fig. 10 shows that a subset of digital outputs (B0–B3) is obtained through the T2V converter when a 5-ns interval is applied between the START and STOP pulses.

Fig. 11 depicts the final 10-bit digital output (B0-B9) when the START-STOP interval is 5 ns. The distinction between logic '1' and '0' is clearly maintained.

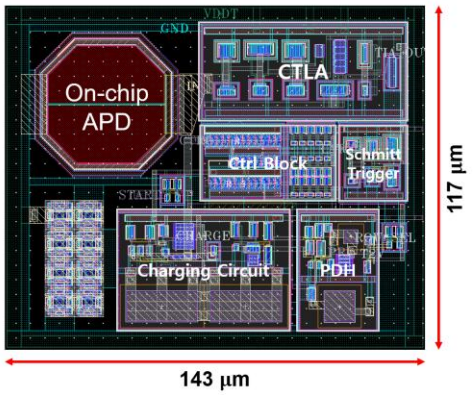

Fig. 8. Layout of the proposed ORIC.

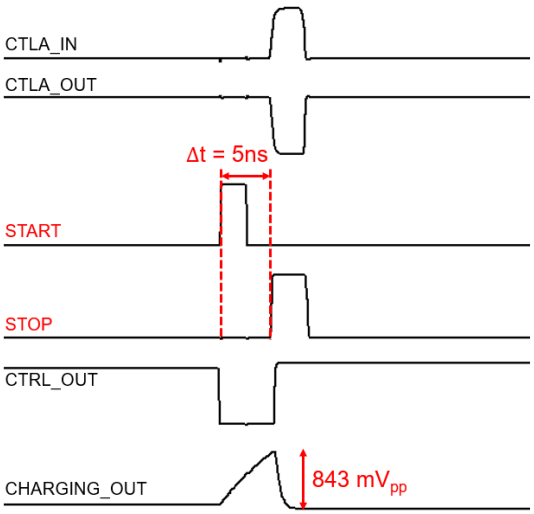

Fig. 9. Post-layout simulations of the ORIC with a 5-ns time-interval between the start and stop pulses.

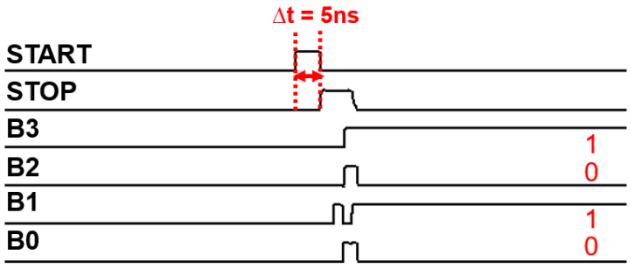

Fig. 10. Simulated final outputs of the proposed T2V converter with a 5-ns time-interval between the start and stop pulses.

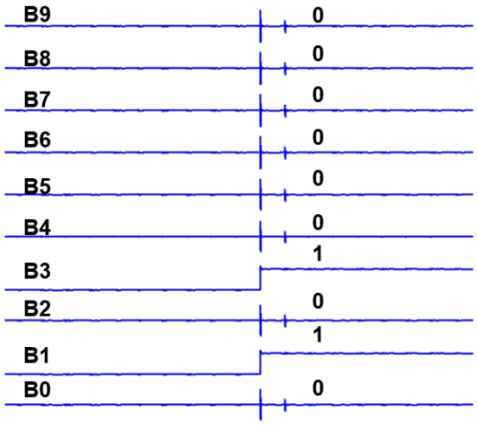

Fig. 11. Simulated 10-bit outputs of the proposed ORIC with a 5-ns time-interval between the start and stop pulses.

IV. CONCLUSIONS

This paper presents an ORIC implemented in a 180-nm CMOS process for real-time elder-care LiDAR sensors, employing a T2V converter and a SAR ADC. The ORIC integrates a P^+/NW/DNW APD and a CTLA, supporting a dynamic range of 47.4 dB that corresponds to the detection range from 31 cm to 4.76 meters. It enables efficient conversion of time intervals into 10-bit binary digital codes, and hence provides a low-power, cost-effective solution for short-range applications including medical monitoring, indoor localization, and robotic vision.

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Somi Park received the B.S. degree in electronic and electrical engineering from Ewha Womans University, Korea, in 2024. She is currently pursuing the MSc degree at the same university. Her current research interests include silicon photonics, CMOS optoelectronic integrated circuits, architectures for short-range optical application systems, and sensor interface IC designs.

Sunkyung Lee received the B.S. degree in electronic engineering from Hoseo University, Korea, in 2024. She is currently pursuing the MSc degree at Ewha Womans University. Her current research interests include silicon photonics, CMOS optoelectronic integrated circuits, architectures for short-range optical application systems, and sensor interface IC designs.

Bobin Seo received the B.S. degree in electronic and electrical engineering from Ewha Womans University, Korea, in 2024. She is currently pursuing the MSc degree at the same university. Her current research interests include silicon photonics, CMOS optoelectronic integrated circuits, architectures for short-range optical application systems, and sensor interface IC designs.

Sung Min Park received the B.S. degree in electrical and electronic engineering from KAIST, Korea, in 1993. He received the M.S. degree in electrical engineering from University College London, U.K., in 1994, and the Ph.D. degree in electrical and electronic engineering from Imperial College London, U.K., in May 2000. In 2004, he joined the faculty of the Department of Electronics Engineering at Ewha Womans University, Seoul, Korea, where he is currently a professor. His research interests include high-speed analog/digital integrated circuit designs for the applications of optical interconnects, silicon photonics, and RF communications.