Design of a 6-bit Broadband Differential Digital Attenuator Using a Hybrid Topology for DC–13 GHz Systems

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***Abstract* - This paper presents the design and implementation of a 6-bit differential digital step attenuator targeting broadband transmitter applications across the DC–13 GHz range. The circuit is fabricated using a 0.13-μm SiGe BiCMOS process and achieves high-resolution attenuation with minimal insertion loss variation across 64 discrete control states. A hybrid topology is employed to optimize performance across all attenuation bits: bridged-T-type topologies are used for the 16 dB and 8 dB bits to ensure flat insertion loss in high-attenuation states; π-type topologies are adopted for the 4 dB and 2 dB bits to achieve compact layout and balanced signal paths; and MOSFET-based resistive shunt switches are utilized for the 1 dB and 0.5 dB bits, enabling fine resolution without discrete resistors. The attenuator operates in fully differential mode to match system-level signal interfaces. Simulation results confirm an RMS amplitude error below 1 dB and an RMS phase error under 16° across the DC–13 GHz frequency range. Embedded matching inductors are used to compensate for the parasitic capacitance of MOSFET switches, enhancing return loss performance. The average input and output return losses are –21.84 dB and –15.11 dB, respectively. The total chip area including pads is 1030 × 510 μm².**

***Keywords*— Attenuator, bridged-T type topology, π-type topology.**

I. INTRODUCTION

Providing high-speed and reliable internet connectivity to remote and underserved regions-such as deserts, oceans, and mountainous terrains-remains a critical global challenge [1]. Terrestrial communication infrastructures, including fiber optics and cellular base stations, are often economically or technically infeasible in such locations due to logistical constraints and limited population density [2]. To address this issue, Low Earth Orbit (LEO) satellite constellations have emerged as a promising solution.

Projects such as Starlink aim to eliminate coverage blind spots by deploying thousands of LEO operating at altitudes of 500 to 2,000 kilometers [3], forming a dynamic mesh network that delivers low-latency, high-bandwidth global internet access [4]. Communication between user terminals and satellites is typically established using radio frequency (RF) links operating in the Ku-band, with uplink frequencies around 14.0–14.5 GHz and downlink frequencies around 10.7–12.7 GHz, depending on regional spectrum regulations [5], [6]. A central challenge in LEO satellite systems is maintaining efficient and reliable directional communication despite the high relative motion between satellites and ground terminals. To address this, beamforming techniques are employed, enabling electronic steering of antenna beams to dynamically track moving satellites without relying on mechanical rotation [7], [8]. This not only enhances link reliability but also improves spectral efficiency by reducing interference and enabling spatial reuse [9].

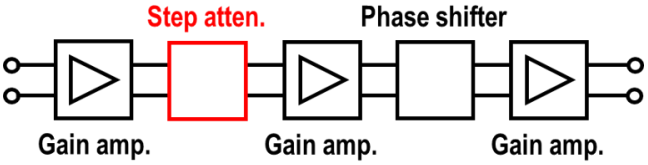

Fig. 1. System-level placement of the proposed differential step attenuator in a transmitter chain.

In addition, to cope with variations in received signal power due to distance, weather conditions, and antenna pointing accuracy, step attenuators are incorporated into the RF front-end [10]. These components play a vital role in optimizing system dynamic range, ensuring signals remain within the linear region of the receiver chain and preserving signal integrity under fluctuating link conditions [11], [12]. As shown in Fig. 1, the proposed differential step attenuator is placed within a representative transmitter chain, providing digitally controlled attenuation at the system level.

In this context, this paper presents a 6-bit broadband differential digital step attenuator operating from DC to 13 GHz for RF front-end applications. A hybrid topology is adopted to achieve wideband operation and attenuation control. The 16 dB and 8 dB stages use bridged-T structures to minimize insertion loss at high attenuation levels [10], [11]. The 4 dB and 2 dB stages employ π-networks to reduce layout area and maintain symmetry [12], while the 1 dB and 0.5 dB stages use MOSFET-based shunt switches for fine resolution without resistors [13]. Embedded inductors are included to compensate for parasitic effects and improve return loss over the target bandwidth [14]. Simulation results show low RMS amplitude error and consistent step response, demonstrating the design's suitability for broadband satellite and phased-array systems.

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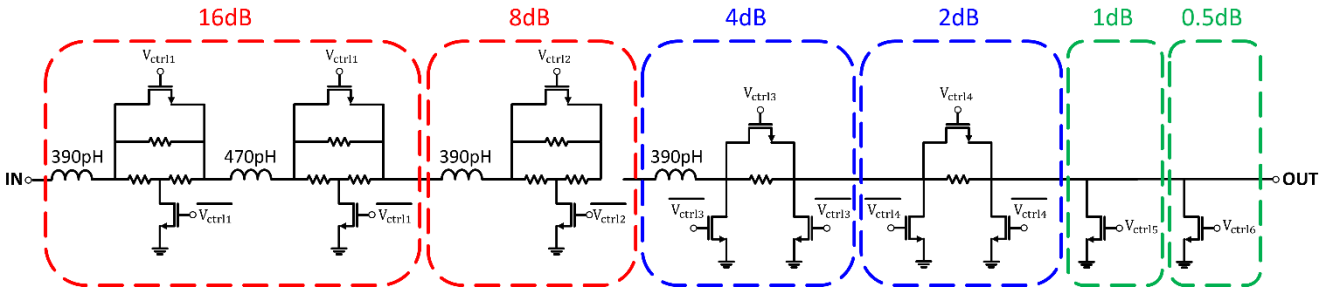

Fig. 2. 6-bit step attenuator schematic.

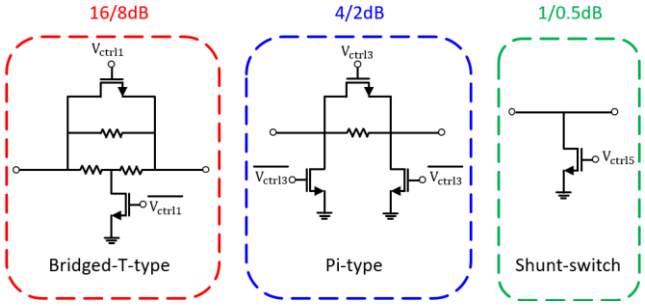

Fig. 3. Schematic diagrams of bridged-T-type (16, 8 dB), π-type (4, 2 dB), and MOSFET-based resistive shunt (1, 0.5 dB) attenuation cells.

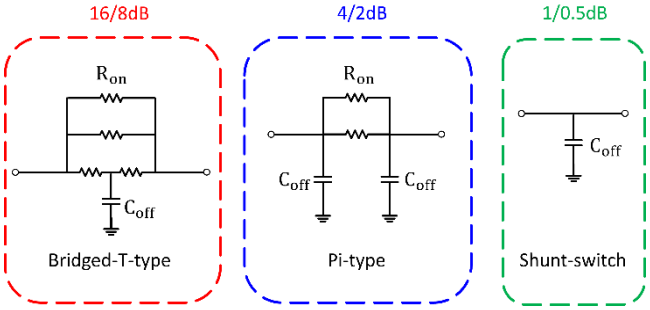

Fig. 4. Equivalent reference-state model showing a conducting series switch R_{on} and a non-conducting shunt switch C_{off}.

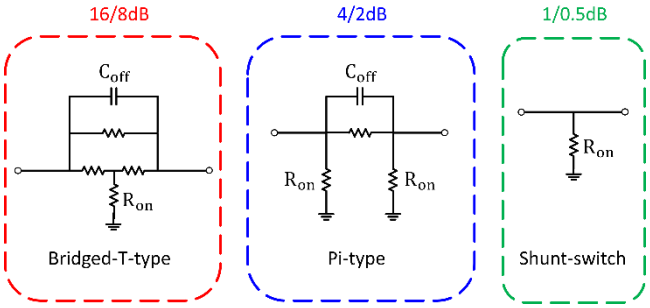

Fig. 5. Equivalent attenuation state model showing a non-conducting series switch C_{off} and a conducting shunt switch R_{on} forming the attenuated path.

II. DESIGN METHODOLOGY

A. Hybrid Topology Design

The attenuator consists of six cascaded control bits with attenuation steps of 0.5, 1, 2, 4, 8, and 16 dB. An overview of the 6-bit step-attenuator architecture and the ordering of the control bits is shown in Fig. 2. To ensure optimal performance over the entire dynamic range and bandwidth, a hybrid topology is adopted in which each bit is implemented with a different circuit structure tailored to its attenuation level. Representative schematics of the attenuation cells bridged-T for the 16 dB and 8 dB bits, π-type for the 4 dB and 2 dB bits, and a MOSFET-based shunt switch for the 1 dB and 0.5 dB bits are provided in Fig. 3. The 8 dB bit is realized using a bridged-T topology consisting of three 100 Ω resistors, one series MOSFET switch, and one shunt MOSFET switch. The 16 dB stage is constructed by cascading two identical 8 dB bridged-T cells, resulting in a total of four switches and six resistors. These bridged-T cells are chosen for high attenuation stages due to their inherently flat insertion loss characteristics and relatively stable impedance matching across frequency. The 4 dB and 2 dB stages are implemented using π-type topologies, employing 60 Ω and 22 Ω resistors, respectively. These configurations offer compact layout and symmetric signal paths, making them suitable for intermediate attenuation levels where trade-offs between area, performance, and balance are important. The 1 dB and

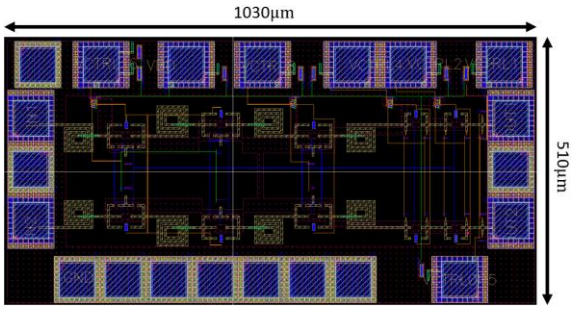

Fig. 6. Cascaded block diagram of the 6-bit hybrid differential attenuator.

TABLE I. Component Values for 6-Bit Attenuator

Attenuator	Type	Series resistance	Shunt MOS (width)
0.5dB	Shunt switches	X	2μm
1dB	Shunt switches	X	4μm
2dB	π	60 Ω	2μm
4dB	π	60 Ω	3μm
8dB	Bridged-T	100 Ω	24μm
16dB	Bridged-T	100 Ω	24μm

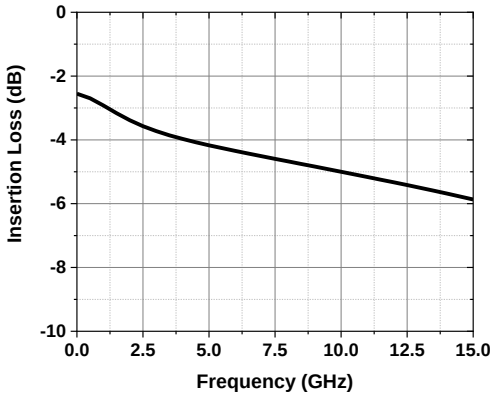

Fig. 7. Simulated insertion loss.

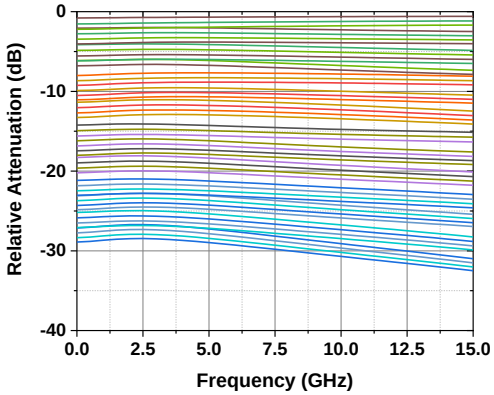

Fig. 8. Simulated relative attenuation of 64 different states.

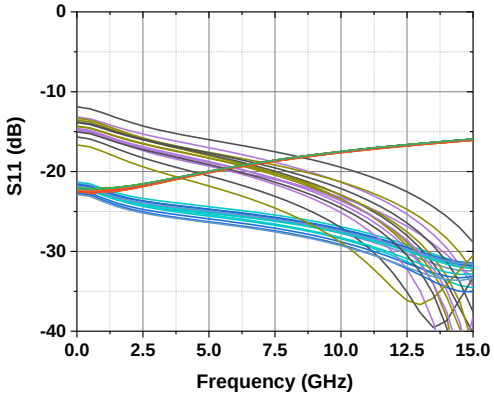

Fig. 9. Simulated input return loss.

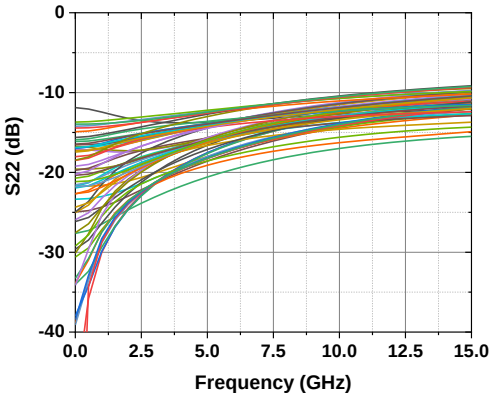

Fig. 10. Simulated output return loss.

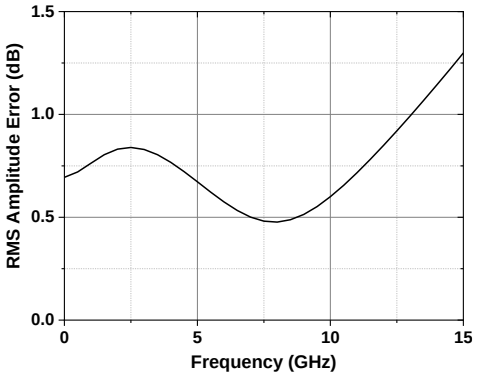

Fig. 11. Simulated rms amplitude error.

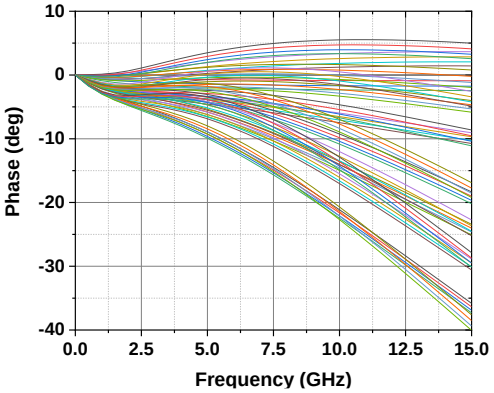

Fig. 12. Simulated phase of 64 different states.

0.5 dB stages are designed using single MOSFET-based resistive shunt switches, which rely on the intrinsic on-state resistance (Ron) of the MOSFET to achieve fine attenuation steps without the use of discrete resistors. All attenuation cells are implemented in a fully differential configuration to support high-speed RF operation, improve common-mode rejection, and ensure compatibility with differential transmitter architectures.

B. Reference and Attenuation States

Each attenuation cell operates in one of two modes-reference or attenuation-based on the digital control input. In the reference state, the series-connected switch is turned on, presenting a low-resistance R_{on} path for the input signal, while the shunt-connected switch is turned off, contributing only its parasitic capacitance C_{off}. This configuration allows the signal to pass with minimal attenuation and defines the reference level of the signal chain, as illustrated in the equivalent reference-state models shown in Fig. 4, where the signal path is dominated by R_{on} and the shunt path presents only C_{off}. In the attenuation state, the series-connected switch is turned off and the shunt-connected switch is turned on. As a result, the main signal path is blocked by the off-state capacitance C_{off}, and the signal is diverted through the conducting shunt path, where R_{on} provides the attenuation. The attenuation level depends on

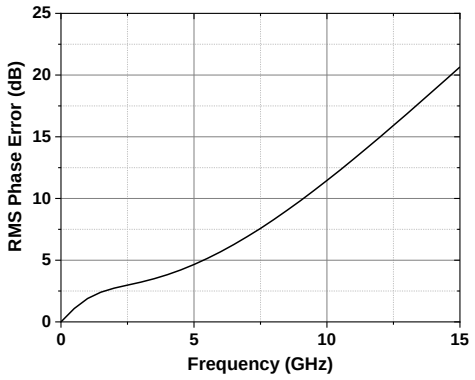

Fig. 13. Simulated rms phase error.

TABLE II.
Comparison Table of the Digital Step Attenuators

Ref.	[15]	[16]	[17]	This work
Process	0.25μm SiGe BiCMOS	0.25μm GaN	0.25μm GaAs pHEMT	0.13μm SiGe BiCMOS
Frequency (GHz)	0.1-4.5	DC-12	0.05-6	DC-13
Number of Bits/ Attenuation Range (dB)	6/31.5	4/30	5/31.5	6/31.5
Insertion Loss (dB)	< 5.4	< 8.3	< 2.3	< 5.5
Return Loss (dB)	>12	>12	> 15	> 10
RMS Amp. Error (dB)	< 0.95	< 1	< 0.8	< 1
Structure	Switched T/Pi	Switched T	Switched T	Switched T/Pi
Chip Area (mm^2)	1.4 x 0.6	2.45 x 1.7	2 x 1	1.03 x 0.5

the bit weight and the topology employed in the cell, as modeled in Fig. 5.

C. Cascaded Implementation

The six attenuation bits-0.5 dB, 1 dB, 2 dB, 4 dB, 8 dB, and 16 dB are cascaded from the most to least significant bit to form a 64-state digital attenuator. Cascading from the most to least significant bit ensures monotonic behavior and minimizes signal distortion across transitions between states. A hybrid topology is adopted to optimize overall performance and chip area: bridged-T structures are employed for the 16 dB and 8 dB bits due to their flat insertion loss characteristics at high attenuation levels; π-type networks are applied to the 4 dB and 2 dB bits, offering compact layout and balanced impedance; and resistive shunt switches are used for the 1 dB and 0.5 dB bits, enabling fine resolution without discrete resistors. The detailed configuration, including the circuit topology, series resistance, and shunt switch MOSFET width for each bit, is summarized in Table I.

To compensate for parasitic capacitance and ensure good impedance matching across the 0–13 GHz frequency band, a total of four series inductors-390 pH, 470 pH, 390 pH, and 390 pHare strategically and symmetrically inserted between and around the bridged-T-type stages. These inductors significantly enhance broadband impedance performance and overall signal integrity.

All RF ports are implemented with a ground-signal-ground (GSG) pad configuration to facilitate on-wafer probing. The physical layout is carefully optimized for structural symmetry and differential balance using full-wave electromagnetic (EM) simulation tools, minimizing layout-induced parasitic effect and phase imbalance. Structural symmetry is essential for maintaining consistent performance across all control codes. The complete chip, including all bonding pads, occupies an area of 1030 × 510 μm². The final layout view is shown in Fig. 6.

III. RESULTS AND DISCUSSIONS

The proposed 6-bit differential digital attenuator was simulated across the 0–13 GHz frequency band to evaluate its broadband performance. Fig. 7 shows the simulated insertion loss, and Fig 8 illustrates the relative attenuation across all 64 digital states from 0 to 31.5 dB in 0.5 dB steps. The attenuator maintains consistent step resolution with minimal deviation, confirming accurate attenuation control across the full dynamic range.

The return loss performance was also assessed. As shown in Fig. 9 and Fig. 10, the input and output return losses (S_{11} and S_{22}) remain better than –10 dB across the entire frequency band. The average input return loss is measured at –21.84 dB, and the output return loss averages –15.11 dB, indicating good impedance matching at both ports even without the need for external matching networks.

To quantify amplitude flatness, the RMS amplitude error across all 64 states was extracted and is shown in Fig. 11. The RMS amplitude error remains below 1 dB across the 0–13 GHz band, demonstrating excellent linearity and flatness over the entire operating frequency range.

Phase characteristics were also analyzed to verify the suitability of the attenuator for phase-sensitive applications such as beamforming. Fig. 12 shows the simulated phase response for all 64 attenuation states, revealing predictable phase variation as attenuation increases. The extracted RMS phase error across the full band is plotted in Fig. 13, which shows that the error remains below 16° up to 13 GHz. These results confirm that the proposed design maintains consistent phase behavior across different states, making it well-suited for broadband phased-array systems. Table II shows the comparison table of digital step attenuators. Our proposed work shows comparable performance compared to other reported work.

IV. CONCLUSION

A 6-bit differential digital attenuator suitable for broadband transmitter systems up to 13 GHz has been presented. The proposed design utilizes a hybrid topology combining bridged-T, π-type, and MOSFET-based resistive switch structures to optimize performance across the full attenuation range. High-attenuation bits adopt bridged-T configurations to ensure flat insertion loss, while low-attenuation bits employ MOSFET-based shunt switches for compact implementation and fine resolution. The attenuator

is implemented in a 0.13-µm SiGe BiCMOS process and occupies a compact chip area of 1030 × 510 μm^2. Post-layout simulations demonstrate precise 0.5 dB step resolution across 64 control states with an insertion loss variation of less than 1 dB. Input and output return losses average –21.84 dB and –15.11 dB, respectively, without requiring external matching networks. The RMS amplitude error remains below 1 dB across the 0–13 GHz operating range, confirming stable and broadband performance. These results validate the proposed attenuator as a highly integrated solution for wideband phased-array systems and reconfigurable front-end architectures that demand both resolution and spectral flatness.

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