A High-Efficiency Hybrid Buck-Boost Photovoltaic Energy Harvester with Adaptive Fractional Open-Circuit Voltage Maximum-Power-Point-Tracking Control

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***Abstract*-This paper presents an energy-efficient photovoltaic energy harvesting system achieving an ultra-wide input power (P_{IN}) range by optimizing both maximum-power-point-tracking efficiency (η_{MPPT}) and power-conversion efficiency (η_{CONV}). An MPPT based on an adaptive fractional open-circuit voltage method is proposed to tune the fraction *k* based on P_{IN} with only little power overhead, unlike other complex and power-hungry hybrid MPPTs. Also, the harvester maintains high η_{CONV} at low P_{IN} levels thanks to its modified hybrid topology that operates as a buck-boost converter with three different control techniques. The proposed zero-current detection circuit reduces the control bit size and response time because it actively changes the tuning resolution according to P_{IN}. The proposed system achieves η_{MPPT} >98% across a 10,000× P_{IN} dynamic range, and the achieved η_{CONV} is greater than 81% across the whole range with a peak efficiency of 96.5%. Compared to other previous state-of-the-art works, this design provides the highest peak η_{CONV} as well as the widest P_{IN} ranges, over which it achieves >98% η_{MPPT} and >80% η_{CONV}.**

***Keywords*—Photovoltaic energy harvesting (PV EH), maximum power point tracking (MPPT), adaptive fractional open-circuit voltage (FOCV), hybrid converter, zero current detection (ZCD).**

I. INTRODUCTION

Demand for modern mobile devices has grown rapidly to fulfill human daily lives and activities. Most of these devices are battery-powered, and battery life has always been a big challenge. Photovoltaic (PV) energy harvesting (EH) has been widely used to extend the battery usage time [1]. However, the power harvested from the PV panels greatly depends on the ambient irradiance. Because mobile devices require to operate both outdoors and indoors, the exposed irradiance of PV panels has a large variation (Fig. 1(a)). Due to such irradiance-level variations, the available power from a PV panel with a size of a touchscreen can vary from hundreds of μW to a W [2].

Fig. 1(b) shows a block diagram of conventional PV EH systems. The energy is harvested from a PV panel and delivered to an energy storage device, such as a battery. For this EH process, a DC-DC converter is used in between to control the operating point of the PV panel and maximize the harvested energy. The maximum possible amount of energy can be harvested from the PV panel by employing a maximum-power-point-tracking (MPPT) method. The end-to-end efficiency can be calculated as the product of the maximum-power-point-tracking efficiency (η_{MPPT}) and power-conversion efficiency (η_{CONV}). However, this maximum power point (MPP) varies over the wide power range of the PV panel [2]. Thus, the MPP should be adaptively found and followed continuously over a wide range to maximize η_{MPPT} and η_{CONV} concurrently.

There are various types of MPPT methods including fractional open-circuit voltage (FOCV), hill climbing, perturb/observe (P&O), and global search. However, most of the integrated energy harvesters use only one MPPT method for wide irradiance levels [2]. As shown in Fig. 1(c, middle), those energy harvesters with power computation-based MPPT schemes [3], [4] are susceptible to errors not only in the current sensing but also in the computation by multiplication circuitry, thereby degrading the MPPT efficiency, especially, under low input power levels. Since conventional FOCV methods [1], [5] offer high MPPT efficiency across a very narrow power range only due to their limited fractional-constant accuracy. The hybrid MPPT method [2] can improve η_{MPPT} but at the cost of complexity and power consumption. Also, η_{MPPT} at both ends of the P_{IN} range is still very low. To address these issues, we propose an adaptive FOCV MPPT method (Fig. 1(c, middle)) that tunes the fraction *k* depending on the measured open-circuit voltage (V_{OC}) output of the PV panel.

The main power loss (P_{LOSS}) in a DC-DC converter consists of conduction loss (P_{COND}), switching loss (P_{SW}), and quiescent loss (P_Q) [6]. As shown in Fig. 1(c, bottom), under high P_{IN} conditions, the conventional PV EH designs [1] - [4] have limited η_{CONV} because of the significantly high P_{COND} incurred by large DCR of the inductor (R_{DCR}) [7]. The previous harvesters [2], [5] have low η_{CONV} under low P_{IN} levels due to high P_{SW} and P_Q caused by using the same size of the power switches and a single switching technique. To overcome these challenges, we propose to use a new hybrid buck-boost topology modified from [7]-[8]. Here a pulse width modulation (PWM) [2] is adopted in the buck mode, while in the boost mode, a pulse skipping modulation (PSM) [9] is implemented in conjunction with a pulse frequency modulation (PFM) [9] and a switch size modulation (SSM) [10]. Thanks to all of these, the proposed work can provide high η_{CONV} across an ultra-wide P_{IN} range.

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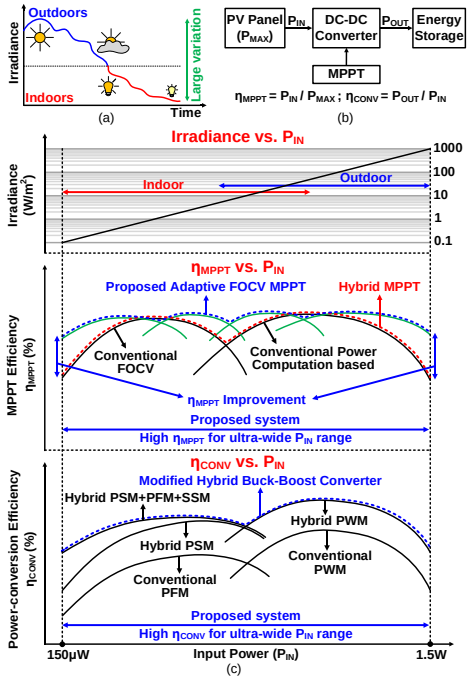


Fig. 1. (a) Irradiance variation profile of a PV panel. (b) Conventional PV energy harvesting system. (c) Comparison of the proposed and conventional energy harvesters in terms of the MPPT efficiency and power-conversion efficiency.

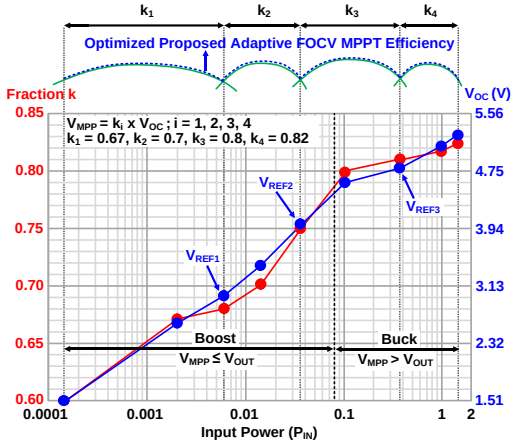


Fig. 2. Measured PV panel characteristics

II. PROPOSED PHOTOVOLTAIC ENERGY HARVESTER

The measured characteristics of the PV panel we used are shown in Fig. 2. The PV panel is built from three 8.9 cm × 5.5 cm monocrystalline PV modules connected in parallel. The measurements are performed under both indoor and outdoor environments that can provide P_{IN} from 150 μW to 1.5 W for the PV EH system. The blue line shows V_{OC} over P_{IN}, and V_{OC} varies from 1.5 V to 5.2 V for the range 150 μW to 1.5 W. The red line shows the fraction *k* over the variation of P_{IN}, and *k* changes from 0.60 to 0.83 over the range.

Fig. 3 shows the proposed PV EH system consisting of a PV panel, a battery, and the proposed hybrid buck-boost converter with an adaptive FOCV MPPT block and a controller. The converter is composed of three 5-V power switches (S_1, which is separated to S_{1_1} and S_{1_2} for SSM, S_2, and S_3) employing the body-switching (BS) technique [8], a flying capacitor (C_F), and

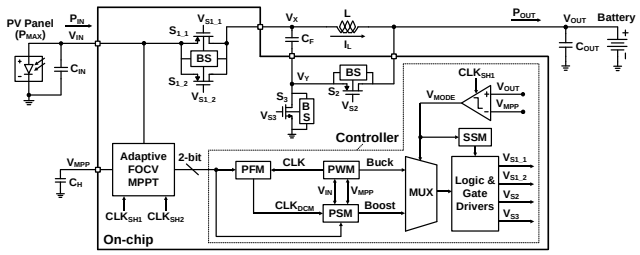


Fig. 3. Proposed photovoltaic energy harvesting IC.

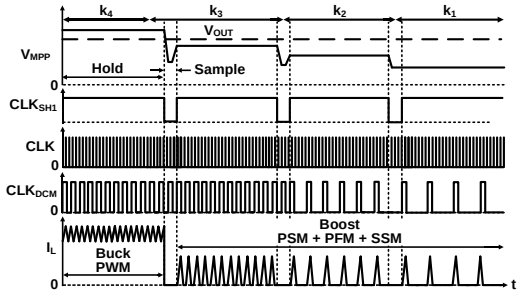


Fig. 4. System operation scheme when the irradiance decreases.

an inductor (L). The MPPT block samples the MPPT voltage (V_{MPP}) and compares it with V_{OUT} to concurrently carry out EH and the mode detection. As illustrated in Fig. 4, when $V_{MPP} \leq V_{OUT}$, the system operates in the boost mode. Otherwise, it operates in the buck mode. A dynamic comparator operated with a low-frequency clock (CLK_{SH1}) is used to detect the mode with only a little power. A 2b output from the MPPT block is used for the PSM and PFM controls. Fig. 4 depicts the system operation scheme for a case when the irradiance decreases. The sample and hold clock (CLK_{SH1}) for the MPPT and the switching clock (CLK) for the PWM control are fixed at 1/12 Hz and 1 MHz, respectively. The irradiance level is monitored periodically at CLK_{SH1}, and based on the level, CLK_{DCM} and the control mode in the boost mode are controlled to minimize P_{LOSS} at low P_{IN} levels.

III. CIRCUIT IMPLEMENTATIONS

A. *Proposed Adaptive FOCV MPPT*

Fig. 5 shows the proposed adaptive FOCV MPPT block. An irradiance detector converts V_{OC} into a 2b digital signal (B_1, B_0) that represents 4 P_{IN} regions. For each region, an optimized k is decided and used, as indicated in Fig. 2. To find the optimized k, k of the PV panel is swept to maximize the lowest η_{MPPT} in all P_{IN} ranges. During the sample period (S_H: on), the 2b digital signal (B_1, B_0) is reset to 0, V_{IN} rises towards V_{OC}, and its initial fraction V_{MPP} (= $k_1 \times V_{OC}$) is sampled on C_H. At the CLK_{SH2} rising edge, the irradiance detector compares V_{IN} with V_{REF1}, V_{REF2}, and V_{REF3} to detect the P_{IN} level. In Fig. 2, the V_{REF} values are defined from the open-circuit voltage (V_{OC}) at the crossing point of the four MPPT efficiency plots for k_1, k_2, k_3, and k_4. Then, V_{MPP} is changed to the corrected V_{MPP} (= $k_i \times V_{OC}$). During the hold period (S_H: off), the corrected V_{MPP} is held on C_H while the converter harvests the energy.

The voltage dividers for creating the fractions of V_{OC} and the reference voltages of the irradiance detector are implemented using diode-connected low-threshold-voltage 5-V PMOS

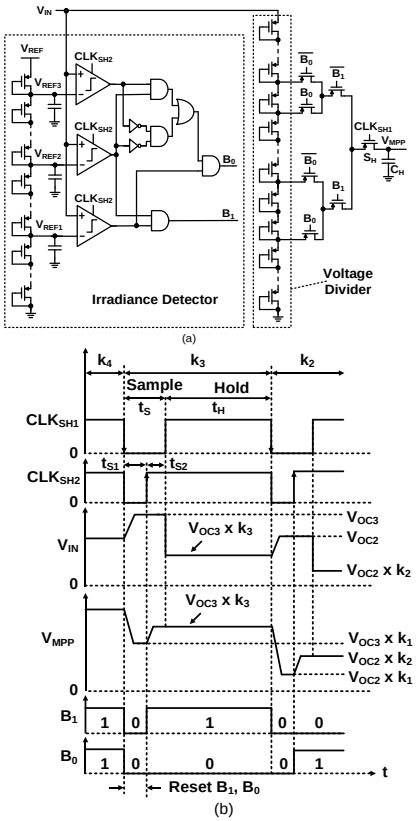


Fig. 5. Proposed adaptive FOCV MPPT block: (a) circuit diagram and (b) waveforms of the main signals.

transistors, as shown in Fig. 5(a). In the irradiance detector, dynamic comparators [11] are adopted to reduce power consumption as it does not consume quiescent power, unlike analog continuous-time comparators. The total sample time t_S (= 0.4 seconds) is chosen in consideration of the power consumed by the voltage divider, that is the main power consumption of the MPPT circuit. The sample time t_{S1} (= 0.2 second) and t_{S2} (= 0.2 second) are decided considering the time for V_{MPP} to rise or fall to the proper values over all P_{IN} ranges. Because the accuracy of V_{MPP} directly affects η_{MPPT}, the hold time t_H (= 11.6 seconds) is designed considering V_{MPP} deviations caused by the leakage from C_H (= 10 nF).

B. Proposed Hybrid Buck-Boost Converter and Control Circuits

Fig. 6 shows the buck mode operation. During Φ_1 (S_{1_1}, S_2: on; S_{1_2}, S_3: off), the inductor current (I_L) ramps up, C_F is charged to $V_{IN} - V_{OUT}$, and V_{OUT} is supplied by the dual paths of I_L and the current of C_F (I_C). During Φ_2 (S_3: on; S_{1_1}, S_{1_2}, S_2: off), L and C_F are connected in series, and I_C is set to $-I_L$ since I_L acts like a current source, supplying V_{OUT}. In comparison to the conventional designs, the dual path topology greatly reduces P_{COND} in the inductor, thus improving η_{CONV} [7]. The boost mode operation is shown in Fig. 7. During Φ_1 (S_2: on; S_{1_1}, S_{1_2}, S_3: off), C_F behaves like a voltage source building up I_L. During Φ_2 (S_{1_1}, S_{1_2}, S_3: on; S_2: off), I_L supplies V_{OUT} and decreases because V_{OUT} is larger than V_{IN}. At the same time, C_F is charged to V_{IN}. During Φ_3 (S_{1_1}, S_{1_2}, S_2, S_3: off), the converter is idle, and the voltage on C_F is held at around V_{IN}. Because this topology needs fewer power switches than conventional buck-

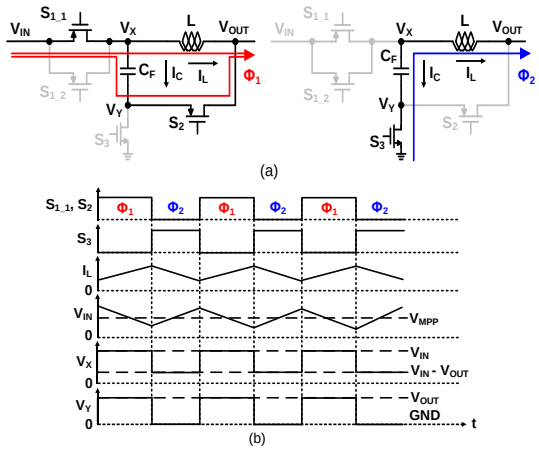


Fig. 6. Buck mode operation: (a) circuit diagram and (b) waveforms of the main signals.

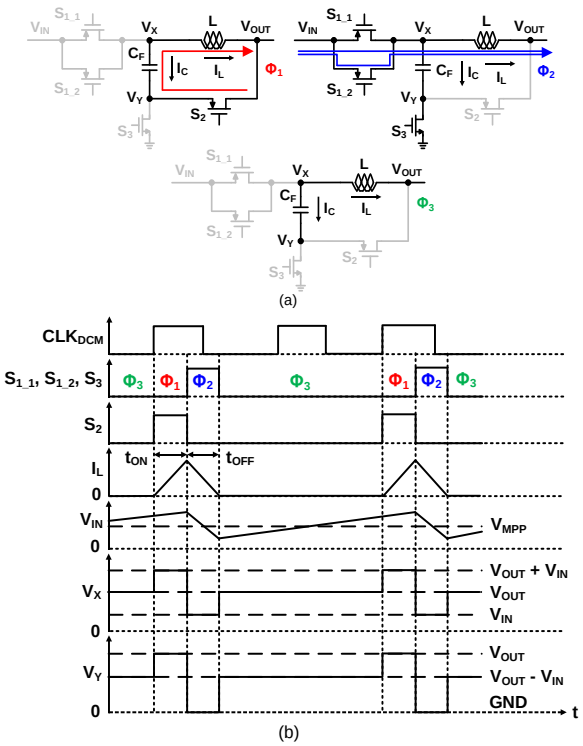


Fig. 7. Boost mode operation: (a) circuit diagram and (b) waveforms of the main signals.

boost converters and only one switch exists in the main current path, it can achieve lower power loss and smaller chip size [8].

The control circuit of the hybrid buck-boost converter is depicted in Fig. 8. In the buck mode, the PWM controller with a type III compensator is adopted to operate the system in continuous conduction mode (CCM). During this mode, the input voltage V_{IN} is regulated by the PWM controller to ramp down to match V_{MPP} at high P_{IN}. In the boost mode, the PSM controller operates the system in discontinuous conduction mode (DCM). The PSM controller regulates V_{IN} to V_{MPP} as follows. During the hold period of CLK_{SH1} (T_H in Fig. 5(b)), the converter harvests the energy from the PV panel, as mentioned in Section III-A. The operation diagram of the converter operating in the boost mode is shown in Fig. 7(b). At the rising edges of the PSM clock (CLK_{DCM}), if $V_{IN} > V_{MPP}$, the converter starts to harvest energy from the PV panel. During this period,

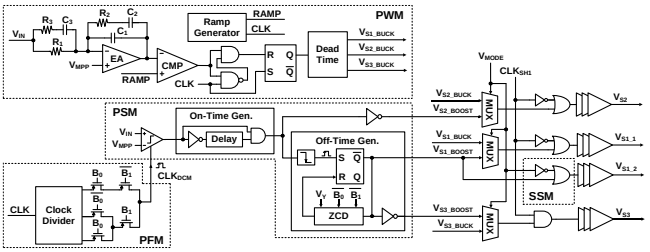
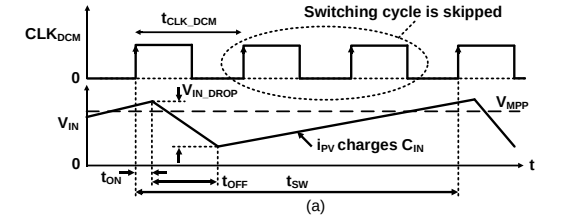


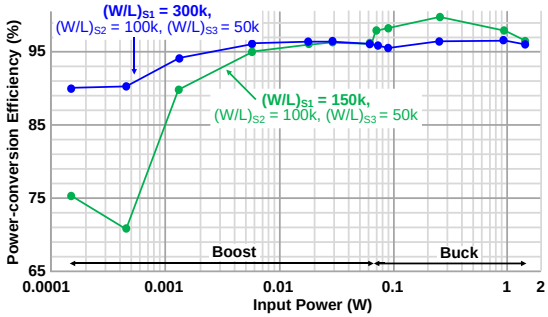
Fig. 8. The control circuits of the hybrid buck-boost converter.



(a)

P_{IN} region	k_1 = 0.67	k_2 = 0.7	k_3 = 0.8
V_{MPP}	1.03V – 2.04V	2.10V – 2.80V	3.20V – 3.5V
t_{SW}	90µs – 320µs	50µs – 90µs	130µs – 220µs

(b)



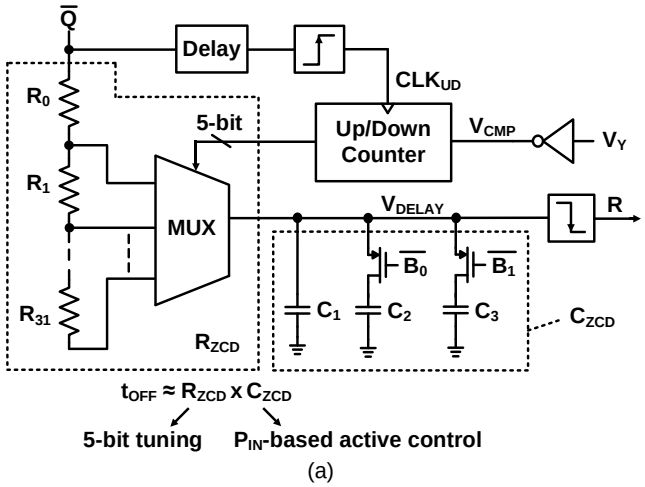
(c)

Fig. 9. (a) Example voltage waveform of V_{IN} with CLK_{DCM} when using the PSM. (b) Simulated switching period without the PFM for three different P_{IN} regions. (c) Power-conversion efficiency improvement by the switch size modulation.

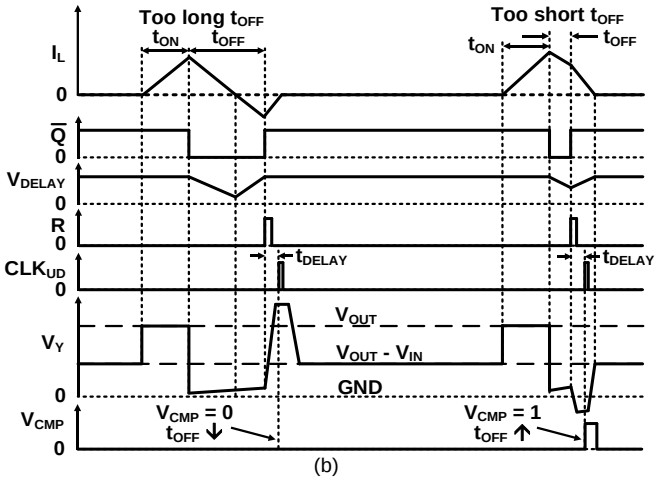
P_{IN} region	k_1 = 0.67	k_2 = 0.7	k_3 = 0.8
V_{MPP}	1.03V – 2.04V	2.10V – 2.80V	3.20V – 3.5V
t_{OFF}	0.41µs – 1.39µs	1.43µs – 3.80µs	6.50µs – 100µs

Fig. 10. Simulated t_{OFF} for different P_{IN} regions.

the on-time generator is triggered to pull V_{S2} low for a fixed on-time period t_{ON} of 1 µs, turning on the power switch S_2. After t_{ON}, V_{S2} is pulled high, turning off S_2. At the same time, the rising edge of V_{S2} triggers the off-time generator [12] to pull V_{S1_1} and V_{S1_2} low for turning on S_{1_1} and S_{1_2}, and it also pulls V_{S3} high for turning on S_3. Three switches S_{1_1}, S_{1_2}, and S_3 are on for an off-time period t_{OFF} until I_L goes to 0, which is detected by the zero-current detector (ZCD). The PFM controller changes CLK_{DCM} based on the P_{IN} region to minimize the controller's quiescent power. CLK_{DCM} is generated from CLK



(a)



(b)

Fig. 11. Adaptive digital ZCD. (a) Circuit. (b) Waveform.

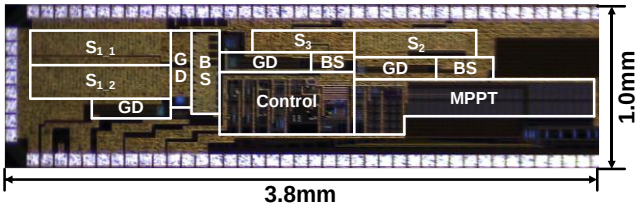


Fig. 12. Die micrograph.

by using clock dividers. The SSM controller activates S_{1_2} to increase the size of S_1 in the boost mode.

Fig. 9 shows the η_{CONV} improvement in the boost mode by using the proposed control techniques. Fig. 9(a) illustrates an example voltage waveform of V_{IN} with CLK_{DCM} when using PSM. To reduce the switching loss, the PSM control skips the switching cycle for two CLK_{DCM} pulses where V_{IN} is lower than V_{MPP}. Although the pulses are skipped, the bandgap reference and the voltage comparator still consume power. To avoid this power loss, PFM can be additionally used [9]. The switching period (t_{SW}) is the sum of t_{OFF} and the time for the current from the PV panel (i_{PV}) to charge the input capacitor C_{IN}. Fig. 9(b) shows simulated variation of

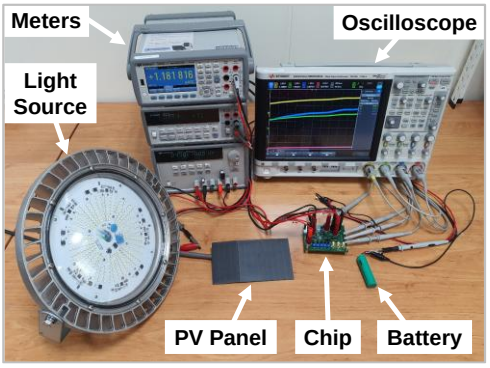


Fig. 13. Measurement setup.

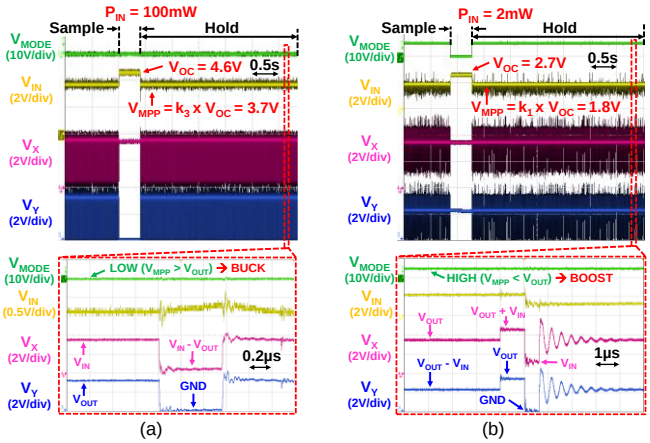


Fig. 14. Measured waveforms of the overall system operation (a) in the buck mode and (b) in the boost mode.

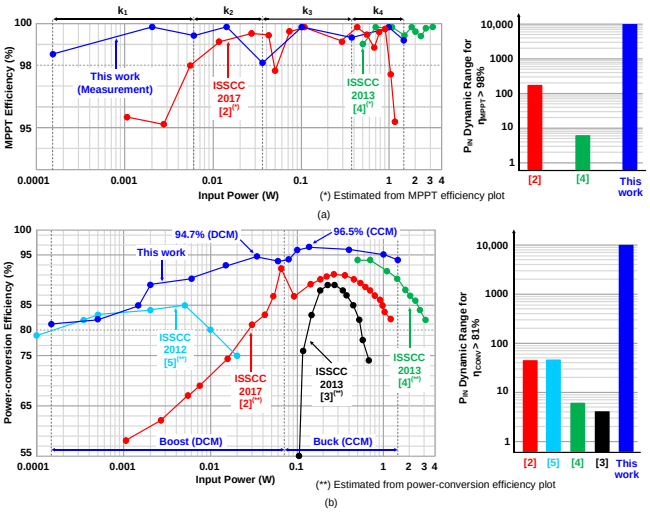


Fig. 15. Measured (a) MPPT and (b) Power-conversion efficiency in comparison with state-of-the-art works.

t_{SW} by P_{IN} when a fixed t_{CLK_DCM} (= 10 μs) is used. In this design, CLK_{DCM} is generated from CLK: $t_{CLK\_DCM} = 2^n \times t_{CLK} = 2^n$ μs. In addition, the period of CLK_{DCM} (t_{CLK_DCM}) has to be smaller than t_{SW} to ensure that V_{IN} can be regulated to V_{MPP}. Therefore, t_{CLK_DCM} for k_1, k_2, and k_3 regions are chosen as 64 μs, 32 μs, and 128 μs, respectively.

Since the charged voltage on C_F (V_{C_F}) ramps up I_L during Φ_2, the peak inductor current (I_{L_PK}) can be expressed as follows:

$$I_{L\_PK} = V_{C\_F} \frac{t_{ON}}{L} \quad (1)$$

In the implemented design, a constant on-time (t_{ON} = 1μs) is used and L is fixed. Thus, I_{L_PK} only varies with V_{C_F}, which is the subtraction of V_{IN} from the voltage drop due to the ON-resistance of S_1. When the size of S_1 increases, the voltage drop decreases, hence increasing V_{C_F} as well as I_{L_PK}. An increase in I_{L_PK} will result in more energy being transferred to the battery improving the efficiency because the energy caused by nonideal ZCD is reduced [9]. The simulated η_{CONV} with a change in the size of S_1 is shown in Fig. 9(c). The power-conversion efficiency is significantly improved at low P_{IN} levels with a larger size of S_1 while being degraded at high P_{IN} levels.

C. *Proposed Adaptive Digital ZCD*

An overly long off-time causes power loss due to the reversed inductor current while an overly short off-time dissipates power in the conduction of the body diode and the reverse recovery of the body diode. Thus, an overly long or overly short off-time is likely to result in extra power loss, significantly degrading the power conversion efficiency [13]. Therefore, an accurate ZCD is required to operate the system efficiently, in particular, at low P_{IN} levels. The conversion ratio of the hybrid boost mode is the same as that of a simple boost converter [8]. Hence, the off-time can be approximately calculated by the inductor volt-second rule [14] as follows:

$$t_{OFF} = t_{ON} \frac{V_{IN}}{V_{OUT} - V_{IN}} \quad (2)$$

In Eq. (2), t_{ON} and V_{OUT} are fixed, and the off-time t_{OFF} can vary from hundreds of ns to 100μs depending on V_{IN}, as indicated in Fig. 10. Note that, t_{OFF} also varies with C_{IN} due to the change of V_{IN} deviation from V_{MPP}. Conventional digital ZCDs with a tunable delay resistor and a fixed delay capacitor [15] that are only applied for a small t_{OFF} range typically need a large control bit size of over 10 and a long time to reach near-zero I_L in this wide
range of t_{OFF}. To address this issue, we propose an adaptive digital ZCD, of which circuit diagram is shown in Fig. 11. The proposed ZCD detects whether t_{OFF} is overly long or overly short by comparing V_Y with GND at the end of each off-time period. The comparator output is converted to 5b control by an Up/Down counter. Then, t_{OFF} is tuned adaptively by only 5b control of the resistor array (R_{ZCD}) at every switching cycle to toggle around the ideal value. The capacitor array (C_{ZCD}) is adaptively changed based on the P_{IN} region to adjust t_{OFF} tuning resolution at the beginning of the sample period. As a result, the settling time of the near-zero inductor current is reduced.

IV. Measurement Results

The IC has been fabricated in a 180 nm CMOS process. The die micrograph of the prototype chip is depicted in Fig. 12. The total chip area is 3.8 mm^2. Fig. 13 shows the measurement setup comprising L = 10μH, C_{IN} = C_{OUT} = C_F = 10 μF, a 3.5-V 1-cell LiPo battery, and a 1.5-W PV panel. This same setup is also used for the measurements of Fig. 2. The light source for the indoor measurements is a 200-W LED. Fig. 14(a) shows the waveforms at the buck mode measured outdoors at V_{OC} = 4.6 V.

In the hold period, the harvester stays in the CCM with the PWM control to regulate V_{IN} to V_{MPP} (= 3.7 V) under the input power of 100 mW. The waveforms at the boost mode measured indoors at V_{OC} = 2.7 V (P_{IN} = 2 mW) are depicted in Fig. 14(b). A proper DCM operation with the PSM control is demonstrated since the resonance exists at the switching node voltages after all the power switches are turned off to enter the idle phase. The operation mode is changed based on V_{MODE}, which is the comparison result between V_{MPP} and V_{OUT}.

Figs. 12(a) and (b) show measured MPPT efficiency η_{MPPT} and power-conversion efficiency η_{CONV} of the proposed PV EH system across a 10,000× P_{IN} dynamic range from 150 μW to 1.5 W, respectively. As shown in Fig. 15(a), the energy harvester achieves >98% η_{MPPT} across the entire 10,000× P_{IN} dynamic range with a peak MPPT efficiency of 99.9%. Fig. 15(b) shows that the hybrid buck-boost converter achieves a peak power-conversion efficiency of 96.5% and maintains an efficiency of more than 81% across the entire P_{IN} ranges.

V. Conclusion

A PV EH system that achieves high MPPT efficiency and high power-conversion efficiency in an ultra-wide dynamic input power range is presented. The proposed MPPT circuit improves the efficiency while consuming a low power of 78 nA. The proposed hybrid buck-boost converter uses only three power switches, achieving high efficiency with small chip area. The IC integrates all the functional blocks in a 3.8 mm × 1 mm die area in a 180nm CMOS process. The proposed EH system is verified by the measurement with a 1.5-W PV panel and a 3.5-V rechargeable battery, providing an energy-effective solution for portable applications.

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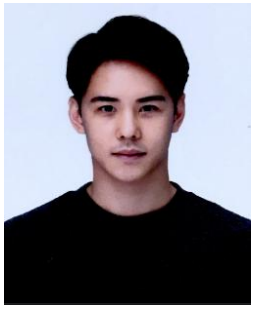

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