Dynamic Performance Enhancement of a Current-Steering DAC Using Tree-Structured Routing and Power Mesh-Based SI/PI Optimization

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***Abstract* - As broadband communication systems demand increasingly higher data rates, the role of High-speed DACs has become essential. Time-Interleaved DAC (TI-DAC) architectures are widely employed to achieve higher sampling speeds by operating multiple sub-DAC channels in parallel. However, employing two sub-channels in a Time-Interleaved structure increases array area and exacerbates power integrity challenges, which can further degrade dynamic performance typically measured by SFDR. Moreover, the physical layout of each sub-DAC includes over 126-unit cells, and non-uniform routing paths between these cells can lead to dynamic mismatch in current summation, resulting in SFDR degradation. Layout-level optimization and PDN enhancement are applied, improving the SFDR from 41.5dB to 52.5dB.**

***Keywords*— Current-Steering DAC, Time-Interleaved DAC, Spurious Free Dynamic Range**

I. INTRODUCTION

To address the speed and power efficiency limitations of conventional Current-Steering DACs (CS-DACs), the Time-Interleaved DAC (TI-DAC) architecture has been widely adopted [1],[2],[3]. As illustrated in Fig.1, the operating principle of a TI-DAC involves multiple sub-DACs arranged in parallel. Each sub-DAC processes input data based on a clock of a different phase. The outputs from these channels are then sequentially selected and combined into a single signal by an analog multiplexer [4]. This Interleaving achieves high speed using slower, power-efficient units.

Despite its advantages, this parallel structure introduces significant design challenges. The increased layout area can compromise the Power Delivery Network (PDN) [5], leading to power integrity issues like IR drop and ground bounce that degrade linearity. Furthermore, mismatches in the physical path lengths from each sub-DAC to the common output node create timing skews [6], resulting in signal distortion [7] at high frequencies.

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Manuscript Received Aug. 20, 2025, Revised Nov. 22, 2025, Accepted Nov. 30, 2025

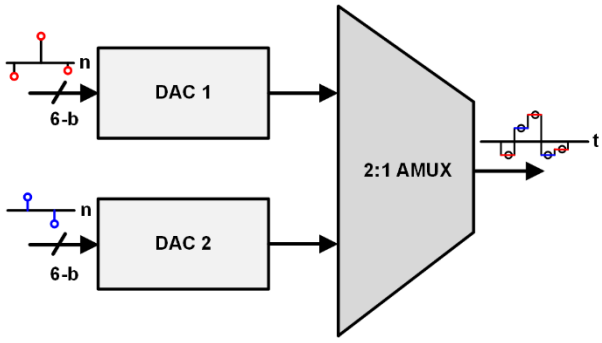

Fig. 1. Operating principle of a Time-Interleaved DAC.

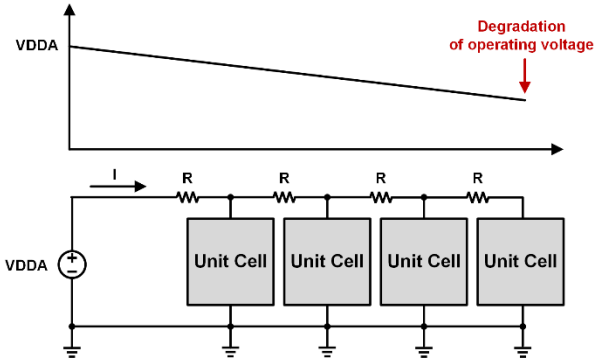

Fig. 2. Supply voltage drops due to power line resistance.

II. EXPERIMENTS

A. Problems with the existing Power Delivery Network

Fig. 2 shows the voltage drop in VDD caused by the series resistance of metal lines when power and ground mesh structures are not implemented. As current flows from the power pad to each unit cell, the cumulative IR drop along the horizontal and vertical metal traces cause a gradual voltage loss. Similarly, on the ground side, the return current path also experiences resistance-induced potential rise, effectively reducing the local voltage difference between VDD and VSS at each unit cell. By modeling this behavior using Ohm's Law (V = IR), with the distributed resistance of the power lines and the cumulative current drawn by each cell considered, the maximum difference in operating

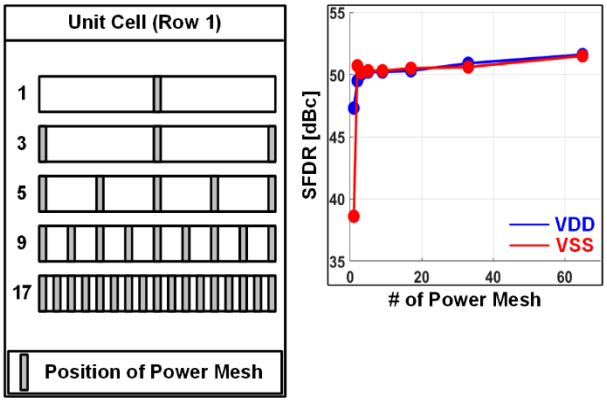

Fig. 3. SFDR dependence on power mesh points.

voltage between the leftmost and rightmost unit cells in the array was found to be 92mV, which is reduced to 26mV with the proposed routing.

Due to the configuration in which VDD and VSS are supplied from the top-left pad, the operating voltage gradually decreases depending on the physical location of each unit cell. When considering the effect of voltage drop due to resistance and distance along the power lines, a maximum deviation in unit current of 8.4 μA is observed. This spatial voltage imbalance leads to non-uniform current outputs across the array, ultimately degrading overall linearity and dynamic performance. Therefore, an optimized power distribution network is essential to ensure consistent bias conditions for all unit cells.

B. Power Network Design and Verification

Fig. 3 illustrates the results from an optimization study of power mesh points, which was conducted on a single horizontal row of the unit cell array using upper-level metals. To enhance the Power Delivery Network (PDN) and lower the series resistance of the power lines, horizontal mesh connections were introduced with seven different configurations, corresponding to 1, 3, 5, 9, and 17 points. The SFDR was measured for each case to quantify the impact on output distortion. The findings demonstrate a clear trend where a finer mesh granularity improves SFDR. Notably, distortion artifacts were substantially mitigated when the number of mesh points was approximately one-quarter of the total cells, which corresponds to the 17-point configuration for the 65-cell row.

The improvement in unit current uniformity across the 2D cell array, following the application of the optimized power mesh. In the original design, the nominal unit current of 31μA varied by as much as 8.4μA due to uneven voltage distribution dependent on the distance from the power pad. Conversely, after strengthening the PDN with the denser mesh structure, this maximum deviation was drastically lowered to just 1.8μA. This significant reduction in current deviation validates the effectiveness of the optimized power mesh in mitigating spatial voltage gradients and ensuring uniform supply conditions throughout the array. Consequently, the operating current of a unit cell becomes far less dependent on its physical position within the layout. This improvement directly contributes to enhanced linearity.

C. Signal Network Design and Verification

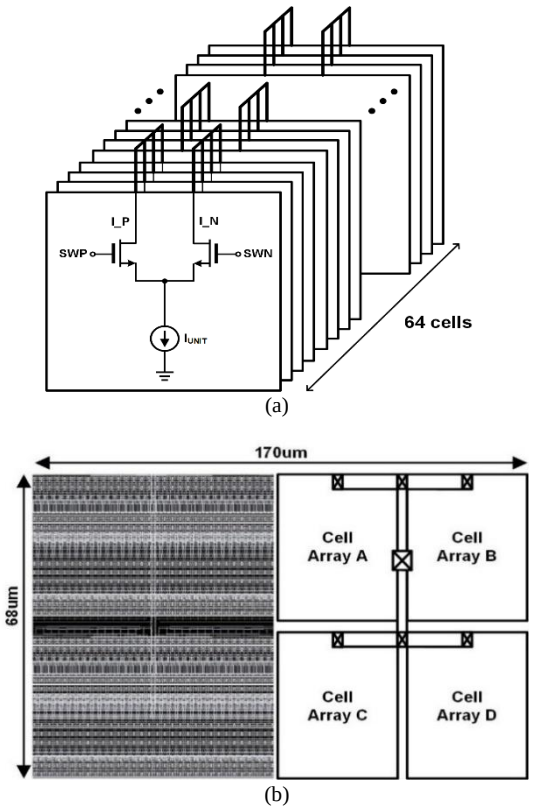

Fig.4. Tree-structured current summation: (a) Horizontal Routing (b) Vertical Routing

Fig. 4. (a) introduces the proposed routing architecture, which is based on a tree-like structure for current summation. In this scheme, the output currents from every four neighboring unit cells are first combined at a local node implemented with the lower metal layers. This initial stage of local current aggregation is designed to minimize parasitic effects by shortening the routing paths from each cell, which in turn reduces IR drop and mitigates layout-dependent mismatches. The collective result is a significant improvement in the signal integrity and overall robustness of DAC's output network. This robust foundation is then scaled up through subsequent hierarchical layers.

The subsequent routing of these aggregated currents through a hierarchy of nodes using upper metal layers is depicted in Fig. 4. (b). This hierarchical methodology is recursively applied until the current from all groups converges at the final differential output terminals, I_P and I_N. The key advantage of this design is the maintenance of electrical and physical uniformity for the signal path from every unit cell to the final output. This uniformity is crucial for minimizing parasitic mismatches that arise from variations in routing length, thereby ensuring stable current delivery. The left panel of Fig. 4. (b) displays the physical layout of the unit cell array, whereas the right panel provides a conceptual view of how the horizontally summed currents are aggregated vertically via the higher metal layers. This layered summation process effectively demonstrates the

structure's capacity to realize symmetrical current routing and balanced signal distribution across the entire DAC.

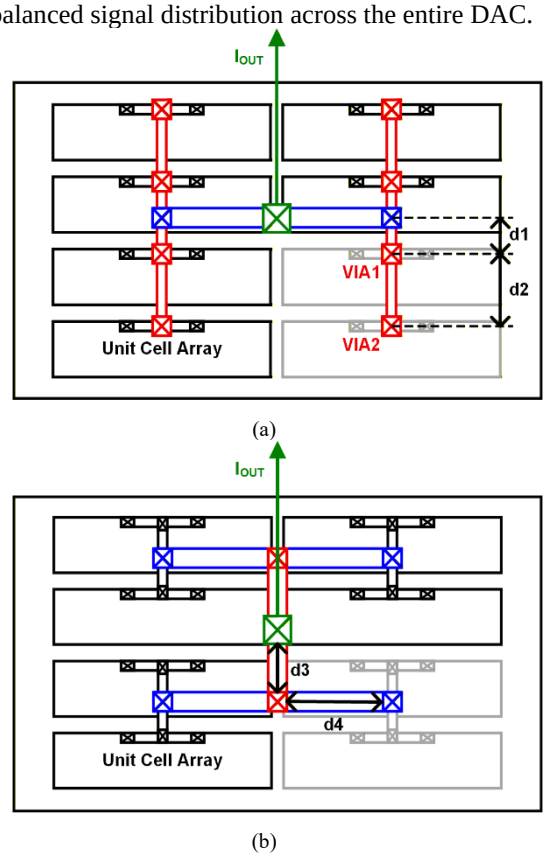

Fig.5. Current path routing structure of the sub-DAC (a) Conventional routing and (b) Layout-optimized tree-structured routing

Fig. 5 illustrates the difference between the conventional current path routing and the proposed tree-structured routing. In the conventional scheme, P/G, Data, CLK, and IOUT lines are routed to minimize the number of crossing points between metal layers, which was previously adopted as a practical layout approach. However, this method inherently produces unequal routing distances from each unit cell to the final output node. For example, the path length to VIA1 corresponds to single routing segment d1, whereas the path to VIA2 accumulates additional horizontal and vertical distances d1 + d2. Such distance dependent variations introduce parasitic resistance and capacitance mismatches among unit cells, which are further amplified in a TI-DAC due to interleaving. As a result, the timing and current summation mismatch lead to degraded SFDR in the conventional routing structure.

Fig.5.(b) illustrates the detailed signal routing organization of the optimized layout, where the proposed tree-structured routing applies a hierarchical summation network that equalizes the electrical distance from every unit cell to the final output. By grouping local currents (e.g. d3 + d4) and routing them upward through symmetric aggregation nodes, the distance from any cell to the blue marked via at the top-level output becomes identical. This layout ensures consistent parasitic loading, uniform propagation delay, and balanced current delivery across the array. Consequently, the tree-based routing significantly reduces layout-induced mismatches and enables substantial SFDR improvement in the TI-DAC.

D. Overall Architecture

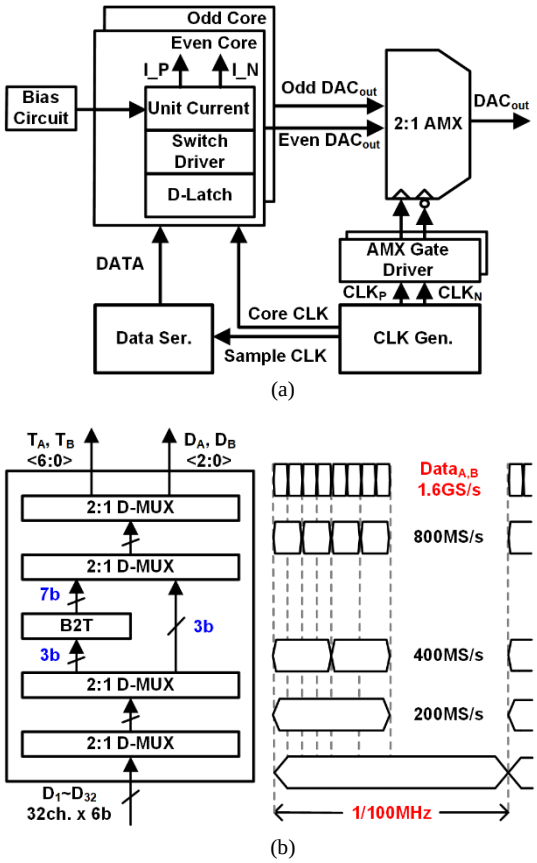

Fig.6. TI-DAC Block Diagram (a) Overall Architecture (b) Data Serializer

The overall architecture of the time-interleaved DAC (TI-DAC), as depicted in Fig. 6. (a), consists of two sub-DACs. By Time-Interleaving these two channels, each operating at 1.6GS/s, the system achieves a final effective sampling rate of 3.2GS/s. For data encoding, a Segmented architecture is utilized, where the 3 most significant bits (MSBs) are thermometer-coded and the 3 least significant bits (LSBs) are binary-coded. This hybrid approach is effective at minimizing switching timing mismatches between unit cells, leading to enhanced linearity during high-speed operation. Specifically, using a thermometer code for the MSBs significantly reduces glitches that occur during major code transitions. Meanwhile, the binary code for the LSBs allows for a more compact and area-efficient layout. This strategic balance between performance and size makes the segmented architecture highly suitable for high-speed, high-resolution applications.

Fig. 6. (b) shows the block diagram of the data serializer used in the proposed design. The structure receives 6-bit parallel input data at 100MS/s across 32 channels (D_1–D_{32}), and sequentially serializes the data through four stages of 2:1 Digital multiplexers. This process generates binary and thermometer codes at a final data rate of 1.6GS/s. At each stage, the serializer selects one of two input paths using a

high-speed clock, thereby halving the number of parallel data streams. By repeating this process in a cascaded manner, the original 32 inputs are sequentially merged into a single high-rate output stream.

III. RESULTS AND DISCUSSIONS

A. post-layout simulation results

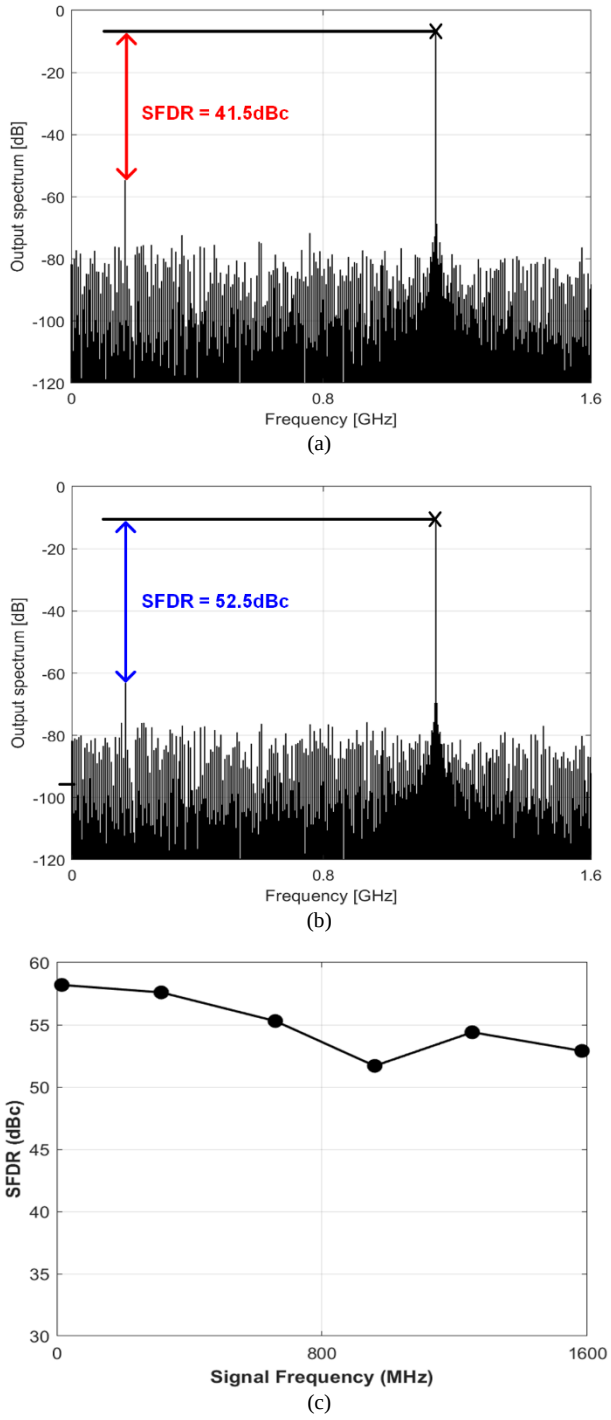

Fig. 7. Post-Layout simulation Results of the TI-DAC (a) With Conventional routing structure (b) With Tree-Based structure and Power/Ground Mesh applied (c) According to Input Frequency

Fig.7 shows the post-layout simulation output of the TI-DAC analyzed using FFT within the first Nyquist zone. The FFT results in Fig.7.(a) to Fig.7.(c) are based on a fundamental input frequency of fin = 1.1GHz and a sampling rate of Fs = 3.2GS/s.

Fig. 7.(a) shows the simulation results when conventional, non-symmetrical routing structures are applied. The output spectrum reveals significant distortion stemming from two primary sources. First, due to current mismatch among unit cells caused by asymmetrical current summation paths and non-uniform voltage drop, spurious tones are clearly observed near 165MHz, resulting in a degraded SFDR of 41.5dB.

Fig.7.(b) presents the FFT result when both the power and ground mesh structure and the tree-based output and clock routing are simultaneously applied. Compared to the results in Fig.7.(a), this configuration effectively mitigates layout-induced mismatches across unit cells. By reinforcing the power delivery network and ensuring symmetric signal paths through hierarchical routing, both current uniformity and clock timing alignment are significantly improved. As a result, the SFDR is enhanced from 41.5dB to 52.5dB, demonstrating a substantial improvement in dynamic performance.

Fig.7.(c) shows the SFDR results of the layout-optimized TI-DAC tested at different input frequencies. SFDR higher than 50dB is achieved within the Nyquist frequency range.

B. Performance Comparison Table

TABLE I. Comparison with State-of-the-Art DACs

Specification	This Work	[1]	[8]	[9]	[10]
Technology (nm)	28	28	16	28	16
Sampling Rate (GS/s)	3.2	11	14	18	28
Resolution (bit)	6	9	8	8	8
SFDR (dB) @Low,fin	58	62	45	52	46
SFDR (dB) @Nyquist	53	52	34	43	37
Supply (V)	0.8/1.6	1	0.8	1/1.5	0.8
Topology	CS[(a)]	CS	SC[(b)]	CS	SC

(a) CS: Current-Steering DAC
(b) SC: Switched-Capacitor DAC
* Low, fin represents Input frequency below 2% of the sampling rate

IV. CONCLUSION

This work presents the design of a 6-bit, 3.2GS/s Time-Interleaved Current-Steering DAC in a 28nm CMOS process. To enhance performance at high speeds, the layout incorporates a tree-structured routing for both output and clock signals, which mitigates current mismatch and signal distortion. Additionally, a mesh-based power and ground grid was implemented to ensure uniform current delivery by minimizing voltage variations across the unit cell array. These layout-level techniques demonstrate that careful physical design can substantially enhance SFDR within a conventional TI CS-DAC framework, making the proposed design suitable for high-speed communication systems.

ACKNOWLEDGEMENT

This research was supported by the "Regional Innovation System & Education (RISE)" through the Seoul RISE Center, funded by the Ministry of Education (MOE) and the Seoul Metropolitan Government. (2025-RISE-01-017-04). The EDA tool was supported by the IC Design Education Center(IDEC), Korea.

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