A 4 - 8GHz Analog Duty Cycle Corrector with 30-70% Correction Range for High-Speed Serial Interface

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***Abstract* - This paper presents the analog duty cycle corrector (DCC) for high-speed and accurate duty cycle correction. To enable high-speed and accurate duty cycle correction, the proposed design utilizes an integrator to extract error information as a DC voltage, while a set generator is introduced to significantly reduce lock time during initial setup time. The proposed circuit was designed using a 65-nm CMOS process. The proposed circuit supports input duty cycles ranging from 30% to 70% across a clock frequency range of 4 - 8 GHz and corrects them to 50% with an accuracy of ±0.5%. The active area of the design is 0.0053mm^2, with a power consumption is 4.42 mW at 8 GHz.**

***Keywords*—Analog Duty Cycle Corrector, Integrator, Set generator.**

I. INTRODUCTION

As the operating frequency and integration density of modern semiconductor systems continue to rise, precise clock timing becomes increasingly critical. Such as, half-rate and quad-rate systems, which are commonly used to support higher data throughput, employ dual-edge clocking, where the duty cycle directly impacts phase alignment and timing margin. But duty cycle distortion is introduced by process, voltage, and temperature (PVT) variations. These variations occur as the clock propagates through on-chip components such as phase-locked loop (PLL), delay-locked loop (DLL), and serial clock buffers. This effect becomes increasingly pronounced at higher frequencies and lower supply voltages. In such systems, even slight deviations from the ideal 50% duty cycle can severely degrade bit error rates. Therefore, ensuring accurate DCC is essential in synchronous systems such as double data rate (DDR) and SDRAM memory interfaces, high-speed transceivers [1]. Conventional DCC architecture can be classified into open-loop and closed-loop approaches. Open-loop DCC offer low complexity and fast locking behavior due to the absence of a negative feedback loop. However, they suffer from limited accuracy [2].

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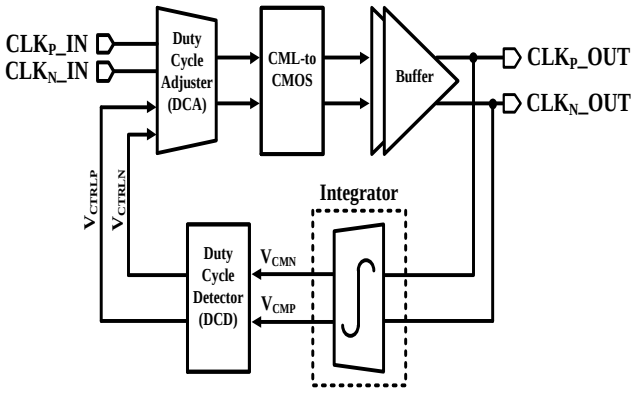


Fig. 1. Block diagram of proposed DCC

Closed-loop DCC, on the other hand, employ negative feedback mechanisms to track and correct duty cycle errors continuously, providing superior accuracy and robustness, though often at the cost of longer convergence time [3]. To address the trade-offs between accuracy, power, and lock time, digital DCC architectures have gained popularity in advanced technology nodes due to their compatibility with low-voltage operation, reduced static power, and ease of programmability. Techniques such as SAR-based calibration and digital finite-state machines (FSM) have been widely explored [4]-[5]. Nevertheless, digital DCC often suffers from limitations in resolution n and linearity, mismatches due to quantization error and non-ideal digital detection circuits. To improve correction accuracy, some hybrid DCC architectures integrate analog comparators with digital SAR control [6]. While such approaches provide better linearity and correction range, they often require additional analog circuit tuning, which can be sensitive to PVT conditions and may complicate integration. In this work, we proposed a closed-loop analog DCC architecture that achieves ±0.5% duty cycle accuracy and 11ns lock time, supporting 30–70% input duty cycles across a 4–8 GHz frequency range.

The remainder of this paper is organized as follows. Section II describes the architecture of the proposed DCC, including the integrator with a set generator. Section III discusses the post-simulation results of the DCC. Finally, Section IV concludes the paper.

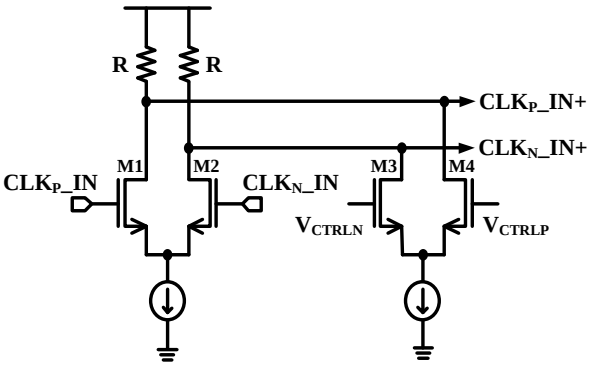


Fig. 2. Schematic of the DCA based on a CML structure.

II. PROPOSED DUTY CYCLE CORRECTOR

Fig. 1 illustrates the proposed DCC architecture. The differential input clock is corrected by the duty cycle adjuster (DCA), which adjusts the duty cycle by combining the input clock with control voltages (V_{CTRLN}/V_{CTRLP}). To enhance the operating speed of the circuit, an integrator incorporating a charge-pump (CP) based set generator is implemented. The output voltage of the integrator is fed into the duty cycle detector (DCD), which generates the corresponding control voltages for feedback correction.

A. Duty Cycle Adjuster (DCA)

Fig. 2 shows the schematic of the DCA. The DCA operates based on a current-mode logic (CML) structure, enabling high-frequency operation over a wide frequency range. M1 and M2 receive the differential input clock signals (CLK_P_IN/CLK_N_IN), while the control voltages (V_{CTRLN}/V_{CTRLP}) generated by the DCD are applied to modulate the current through M3 and M4. This modulation alters the common-mode (CM) level of the output signals, which in turn affects the transition time, thereby adjusting the duty cycle of the differential input clock.

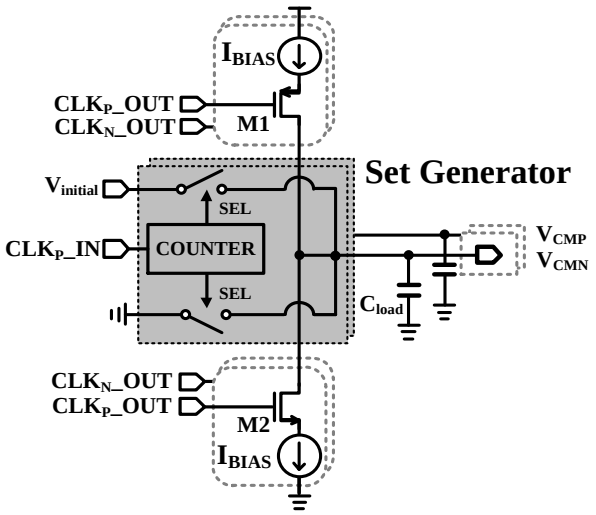
B. Integrator

Fig. 3(a) illustrates the proposed integrator, which is designed based on a CP structure to support high-speed operation. The differential output clock is fed back into the integrator, where the same clock signal is applied to M1 and M2. This configuration enables the extraction of a DC voltage that corresponds to the duty cycle error of the opposite-phase clock. For instance, if the feedback differential clock exhibits a duty cycle error of 70% (CLK_P_OUT) and 30% (CLK_N_OUT), the integrator receiving CLK_P_OUT as input generates an output voltage V_{CMN} such that the average current charging the output capacitor (C_{load}) through M1 is 0.3 × I_{BIAS}, while 0.7 × I_{BIAS}

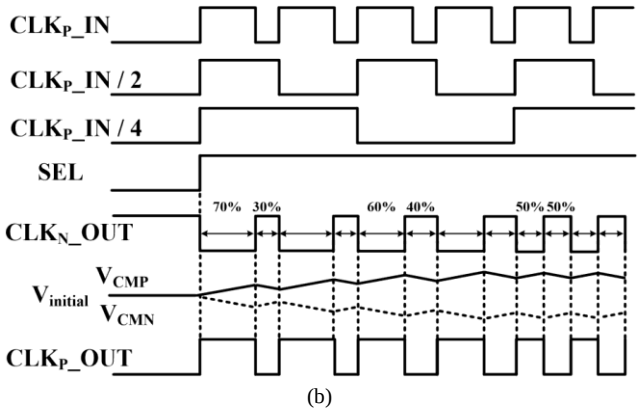
$CLK_P\_OUT(duty\ cycle\ 70\%)$

$$V_{CMN} = V_{initial} + \frac{1}{C_{load}} \int (I_{BIAS} \times (0.3 - 0.7))\, dt \quad (1)$$

is discharged through M2. This relationship forms the basis



(a)

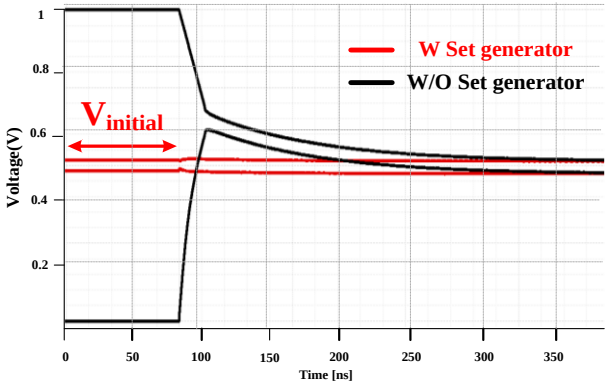


(b)

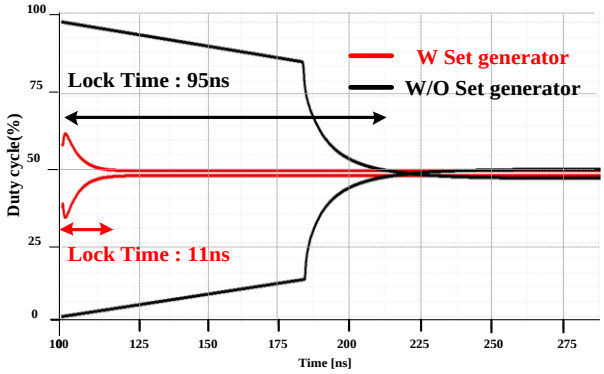
Fig. 3. (a) Proposed integrator with embedded set generator for fast locking. (b) Timing diagram of the integrator showing the effect of initialization on VCMN and VCMP.

of the integrator behavior as described in Equation (1). Consequently, the integrator generates a DC voltage V_{CMN} that reflects the duty cycle error of CLK_N_OUT. Similarly, when CLK_N_OUT is applied to the integrator input, a charging current of 0.7 × I_{BIAS} and a discharging current of 0.3 × I_{BIAS} are produced. This results in the generation of V_{CMP}, a DC voltage corresponding to the duty cycle error of CLK_P_OUT. This relationship is the vice versa of that described in Equation (1).

When the DCC is locked and both CLK_P_OUT and CLK_N_OUT achieve a 50% duty cycle, the charging and discharging currents to C_{load} become equal. As a result, the output voltage maintains the value that has been integrated previously by the duty cycle error. However, during the initialization phase of clock generation circuits such as PLL, the differential input clocks are typically held at fixed logic levels (0 and 1). This condition prevents immediate extraction of the duty cycle error, thereby introducing a significant delay. Under such conditions, the output of the integrator also remains fixed at 0 or 1 during the initial phase, which adversely affects the overall lock time of the DCC. To address this issue, a set generator is embedded within the



(a)



(b)

Fig. 4. (a) Output voltages V_{CMN} and V_{CMP} of the integrator during initialization. (b) Duty cycle of the differential output clock showing the effect of the set generator on lock time.

integrator, as shown in Fig. 3(a). It receives one of the differential clock inputs and performs a 3-bit counter operation. Until the input clock exits its initialization state, the set generator applies a predefined initial voltage ($V_{initial}$) to both V_{CMN} and V_{CMP}. Once the initialization phase is complete and the SEL signal from the counter transitions to 1, as shown in Fig. 3(b), the $V_{initial}$ is released, and the integrator begins to generate V_{CMN} and V_{CMP} voltages that reflect the duty cycle error of the differential clock.

III. SIMULATION RESULTS

The proposed DCC was designed using a 65 nm CMOS process with a 1 V supply voltage. It operates over a frequency range of 4 – 8 GHz and supports duty cycle correction for input clocks with duty cycles ranging from 30% to 70%. The power consumption is 4.42 mW when the differential input clock at 8 GHz with a 30%-70% duty cycle. Fig. 4(a) shows the output voltages V_{CMN} and V_{CMP} of the proposed integrator that includes the set generator. During the first 100 ns, the differential input clock remains in an initialization state, keeping V_{CMN} and V_{CMP} fixed at 0 and 1, respectively. However, by applying a predefined $V_{initial}$ through the set generator during this phase, the DCC lock time is reduced from 95 ns to 11 ns, as shown in Fig. 4(b). Fig. 5 presents the simulation results for duty cycle

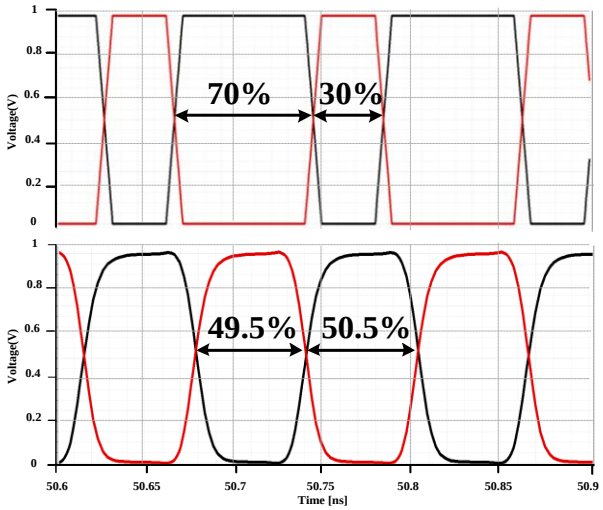


Fig. 5. Post simulation results of the DCC output duty cycle for differential input clocks with 30% and 70% duty cycles at 8GHz.

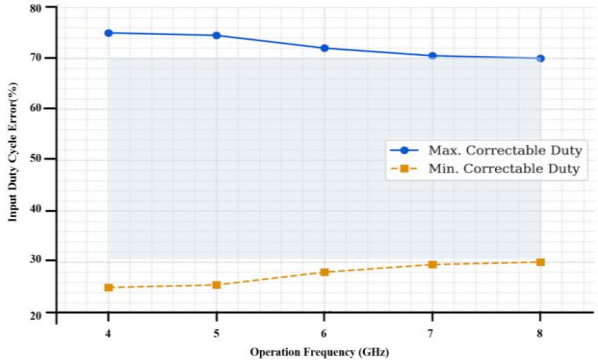


Fig. 6. Min/Max duty cycle error correction range depending on operation frequency.

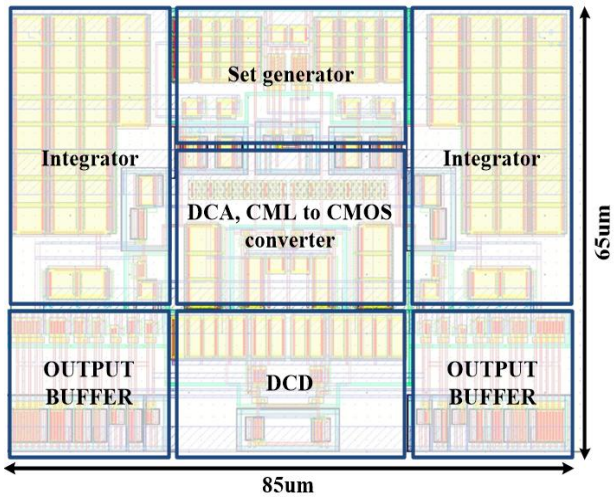


Fig. 7. Proposed DCC layout.

correction when the differential input clock, operating at 8 GHz, has a duty cycle of 30%-70%. As shown in Fig. 6, it supports duty cycle correction for input clocks with duty cycles ranging from 30% to 70%, ensuring the output is corrected to 50 ± 0.5%. Table I shows the performance of the proposed DCC and provides a comparison with prior works. Though the analog DCC in the proposed method results in higher power consumption and a narrower

Table I. Performance Summary and Comparison with Other Recent Duty Cycle Corrector

	[6]	[7]	[8]	This Work
Types	Analog feedback	Analog feedback	Analog feedback	Analog feedback
Process	55nm	35nm	65nm	65nm
Supply(V)	1.2	1.2	1	1
Power consumption(mW)	3.6@3GHz	1.1@600MHz	0.32@5GHz	4.42@8GHz
Operation frequency	1GHz-5GHz	3MHz-600MHz	500MHz-5GHz	4GHz-8GHz
Correction Range	20% - 80%	30% - 70%	20% - 80%	30% - 70%
Duty accuracy(%)	<±0.5%	<±1%	<±0.7%	<±0.5%

correction range compared to the previous method [8] but achieves higher duty cycle accuracy at high speeds compared to [6]-[8] by employing an integrator with a set generator.

IV. CONCLUSION

In this work, analog feedback-based DCC is presented, supporting a wide correction range of 30%–70% over a clock frequency range of 4–8 GHz. The internal blocks of the DCC include a DCA, a CML-to-CMOS converter, buffer stages, an integrator, and a DCD. Fig. 7. presents the layout architecture of the proposed DCC. To ensure high-speed and accurate operation, the duty cycle error of the differential input clock is converted into a DC voltage using the proposed integrator. However, during the initialization phase of clock generation circuits such as PLL, the integrator output may become latched to 0 or 1 due to fixed input levels, which significantly affects the DCC lock time. To mitigate this issue, a set generator is integrated within the proposed integrator. This block maintains a predefined initial voltage during the input clock initialization period, reducing the lock time from 95ns to 11ns.

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