Dual-Core High-Swing Class-C VCO design

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***Abstract* - We utilize the idea of reducing phase noise (PN) by combining multiple oscillators. The dual core LC-tank oscillator is based on a high-swing class-C topology and realized in 65-nm CMOS process. As a result of simulation, it is tunable within 1.12-1.25 GHz, while drawing 1.7 mA from a 1.2 V power supply. Phase noise and figure-of-merit (FOM) are −135.0 dBc/Hz and 194 dB at 1MHz, respectively, from a 1.12 GHz carrier frequency.**

***Keywords*—Figure of merit (FoM), low-noise oscillators, phase noise, voltage-controlled oscillators**

I. INTRODUCTION

Voltage controlled oscillators (VCO's) are an essential part of phase-locked loops which are the most common frequency synthesizer. Random fluctuations in the output frequency of VCO's, expressed by phase noise, have a direct impact on timing accuracy where phase alignment is required and cause the signal-to-noise ratio (SNR) issues. In other words, RF oscillators must meet stringent phase noise requirements.

Extensive efforts [1] − [6] have been made to improve the phase noise in CMOS oscillators while maintaining a good figure of merit (FoM), i.e., normalized PN per 1 mW of power consumption

$$FoM = PN + 20log_{10}\left(\frac{f_0}{\Delta f}\right) - 10log_{10}\left(\frac{P_{DC}}{1mW}\right) \quad (2)$$

where f_0 is the oscillating frequency, Δf is the frequency offset from f_0, and P_{DC} is the power consumption. From the previous works, the only realistic way to improve phase noise performance is to increase the power consumption P_{DC} while maintaining a good FoM [7]. This appears to invariably lead to an increase in the oscillation amplitude Vosc of the resonating LC-tank according to (based on (2) in [3])

$$V_{OSC} = \sqrt{P_{DC} \bullet \alpha_I \bullet \alpha_V \bullet Q \bullet \omega_0 L} \quad (3)$$

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where α_I and α_V are the current and voltage conversion efficiencies, Q is the tank′s quality factor, and L is the tank inductance. α_I and α_V are largely fixed by the chosen oscillator topology.

For an optimal power consumption efficiency (i.e., FoM), Q should be kept as high as possible. Trying to increase P_{DC} to further improve phase noise will increase V_{OSC} and eventually lead to serious device stability issues [3]. Hence, based on (3), a reasonable strategy in delivering more effective PDC would be decreasing L while keeping V_{OSC} at its maximum tolerated level. As pointed out later in Section II, there are technological limitations on how low L can go. To conclude, each CMOS process seems to have a technological limit to the phase noise of a given oscillator topology (i.e., α_I and α_V).

We propose to break that limit by a dual-core oscillator topology [8] and then demonstrate it in Samsung 65nm CMOS process. Section II provides background on various techniques to improve PN. Section III details more on the multi-core oscillators. Section IV describes the simulation results of multi-core oscillator design and conclusion in Section V.

II. PHASE NOISE REDUCTION TECHIQUES

A. Parameter Optimization

In 1966, Lesson presented an empirically derived PN (L) model of oscillators [9]

$$L(\Delta\omega) = 10log_{10}\left(F\frac{4kTR_P}{V_{OSC}^2}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right) \quad (4)$$

where k is Boltzmann′s constant, T is the absolute temperature, R_P is an equivalent parallel tank resistance, and F is a noise factor of the active device.

Leeson′s equation shows the dependency of PN on Q. In bulk CMOS process, the inductor's Q-factor is limited to around 30 in the best case with ultra thick metal option. Furthermore, oscillators should cover a certain tuning range (> 10%) to account for variations in process, voltage and temperature (PVT). Such tuning is typically done with switched capacitors or varactors, which also have a limited Q-factor. In addition, there is a trade-off between Q factor and the tuning range of these tuning capacitors. As a result, there is not much margin left on the Q of the tank to further improve the PN in scaled CMOS.

Furthermore, due to advances in the CMOS technology, the supply voltage, VDD is systematically reduced. Maximum practical voltage swing V_{OSC} in the oscillator gets saturated to less than twice VDD. Hence, the voltage scaling will directly lead to the PN degradation according to (4). Moreover, FoM of the oscillator is also dependent on the voltage conversion efficiency, $\alpha_V = V_{OSC}$/VDD, which tends to be degraded due to supply scaling. It has been shown that [8]

$$FoM = \frac{4Q^2 \cdot \alpha_I}{F \cdot 4kT} \times \frac{V_{OSC}}{V_{DD}} \times 10^{-3} \quad (5)$$

where α_I is the current conversion efficiency (conversion ratio of the bias current into the fundamental current harmonic).

An important parameter is an inductance value, L, of the LC-tank. Equation (5) is written such that FoM does not depend directly on L. However, L affects the equivalent parallel resistance of the tank as R_P=$L\omega Q$. By decreasing L and, consequently, R_P (while managing to keep Q constant), PN can be reduced, as per (4). However, the bias current should be increased to keep the maximum oscillation amplitude while maintaining FoM.

To reduce the PN as much as possible, one might choose a high-Q inductor at first and then try to reduce the radius or the number of turns to lower the inductance. Multi-turn inductors may have a slightly higher quality factor, but by choosing a single-turn inductor, a much lower inductance value can be obtained. Reducing the radius of the inductor lowers the inductance. However, after a certain point, the quality factor starts dropping dramatically as series resistance losses start to dominate. By trading off between a low L and high Q, we can find the optimum point from which further increasing the inductance would worsen the PN, but lowering the inductance would drop Q and thus worsen FoM and perhaps even phase noise. At that point, the oscillator could have the lowest possible phase noise in a given process technology with a good FoM. In other words, to improve the phase noise of the oscillator, the term R_P/Q^2 = Lω/Q from (4) needs to be reduced. This ratio cannot keep on decreasing indefinitely since at certain point Q drops more than L. Moreover, there are also limitations on how small an inductor can be before the inductor is limited by vias and other routing parasitics.

B. High-Swing Class-C Topology

Based on Leeson′s equation, another parameter that can be utilized to improve PN is F (i.e., amplifier′s noise factor). There are a number of efforts to reduce F by shaping the tank voltage and reducing the effective noise of active devices [1]–[3], [5].

A class-C oscillator was first introduced in [5] and, according to [10], its ENF is very competitive. As noted above, the phase noise improves with increasing the oscillation amplitude, which here would mean lowering the gate bias voltage, V_{bias}. Unfortunately, the original class-C oscillator limits the fixed V_{bias} from being set low enough, otherwise the oscillation may not start up. In [11], a high-swing class-C (HSCC) oscillator was introduced, which removed the tail current transistor of the original class-C oscillator [5]. Instead, an automatic amplitude control was introduced to stabilize the oscillation amplitude. In this work, instead of the transformer used in [11], we choose a simple RC bias circuit. The oscillator schematic is shown in Fig. 1. The currents of the core transistors are mirrored and compared to the reference bias current I_{REF} and after integrated, the resulting control voltage V_{ctrl} is applied to the cross-coupled $M_{1,2}$transistor gates. At start-up, since there is no current through the oscillator, V_{ctrl} node rises to V_{th}+V_{od}. As the waveforms demonstrate in Fig. 5., the amplitude feedback scheme produces the maximum V_{ctrl} to ensure stable start-up and adaptively reduces at steady-state for class-C operation with high output voltage swing.

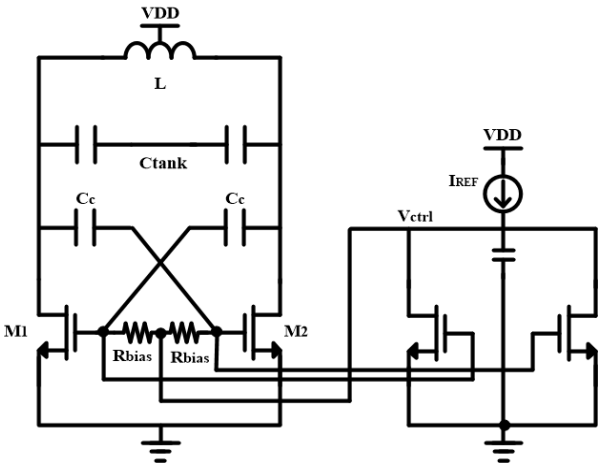

Fig. 1. Schematic of high-swing class-C (HSCC) oscillator used in this work

The value of R_{bias} should not be too small as it could load the tank′s Q and not too large as to avoid amplitude instability in the feedback loop due to the RC network delay. The noise contribution from R_{bias} has no negative impact since it will be filtered out by the low-pass combination of R_{bias} and C_C. Other methods of using transformer coupling may also be beneficial with regard to amplitude stability.

In the next section we demonstrate how to further improve phase noise by combining multiple oscillators.

III. MULTI-CORE OSCILLATOR

To address the aforementioned limitations on the phase noise performance of a CMOS oscillator, we utilize the old idea of combining multiple oscillators [12]–[14] and propose that such coupling can be resistive using, e.g., long and thin traces, which is often convenient in practical realizations. Fig. 2 depicts this idea for N = 2, i.e., a dual-core oscillator. Two identical oscillator cores (generally of any topology, but here the core is the high-swing class-C from Fig. 1) are combined in parallel thus they are

oscillating in-phase. Each of the inductors has its own local capacitor bank. Therefore, the high resonant current of each LC-tank is circulated only locally.

According to Leeson′s formula (4), by halving L and doubling the capacitance, the oscillation frequency remains the same but R_P becomes half, which reduces phase noise by 3 dB.

For deeper insights, consider the following: If we would apply this technique (i.e., doubling the capacitance) to a single core, the inductor needs to be scaled down also by a factor-of-two in order to maintain the frequency. Then, phase noise would improve because of the R_P reduction (as discussed in Section II). However, at some point, the continuous decrease in L hits the physical limits of technology, where Q-factor begins to drop sharply. This is exactly where we back off a bit and picks our inductor value.

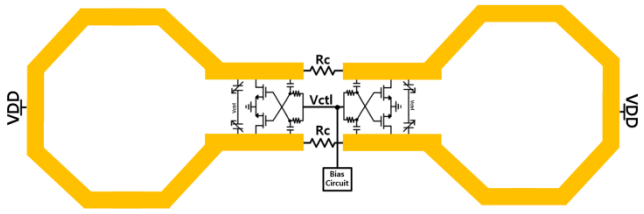

Fig. 2. Dual-core high-swing class-C (HSCC) oscillator

As a result, to move forward with the phase reduction, we then proceed to the dual-core topology. In general, the presence of N tanks reduces the phase noise due to a single noise source by a factor N^2. There are now N current noise sources instead of just one. As the noise sources are all uncorrelated and equal in power, the total phase noise is N times contribution of one of them. Therefore, the total phase noise is N times better than with a single core

$$L_N(\omega) = L_1(\Delta\omega) - 10\log(N). \quad (6)$$

Obviously, since the total power consumption grows N times, FoM is not changed [15]. Hence, the lower phase noise would come at a cost of proportionately higher area and power consumption. For a weakly coupled multi-oscillator system, the oscillators inject small currents into each other and hence take some time to correct the resulting perturbations. These perturbations will affect the coupled system differently according to their frequency content. Low frequency noise perturbations will afford enough time for the system to respond and hence achieve the expected phase noise improvement while fast perturbations or high frequency noise will experience less such rejection. The conclusion is that the coupling factor mainly affects the bandwidth of the PN improvement; i.e., the larger the coupling factor, the wider the bandwidth of the PN improvement.

Combined oscillators have been used to provide multiple phases to integrated transceivers. To design a 2N-phase LC oscillator, at least N (differential) oscillator cores are needed. In theory, they have the advantage of reduced phase noise: N-coupled oscillators have N times less phase noise than a single oscillator [13]. However, such coupling for the multi-phase generation might lead to phase noise degradation due to additional noise from the coupling devices [4], [15], [16].

A major concern that comes along with practical implementations of multi-core oscillators is how to connect all of them in parallel. In our approach, the multiple oscillators are simply coupled electrically through a finite parasitic resistance R_C of the interconnecting wire. Since the footprint of inductors is bulky, interconnections between them are expected long. Hence, the resistance of these interconnects would play a role in the phase noise performance. Another imperfection is a mismatch between free-running frequencies of the cores. In the presence of high interconnect impedance, the mismatch increases the likelihood that the core would oscillate at separated frequencies, creating injection pulling spurs. Therefore, the coupling must be tight enough to achieve the desired phase noise performance.

In an ideal completely matched case, no static or cyclic current flows through the wires inter-connecting the two cores. Nonetheless, a very small noise current (with an average of zero) is flowing back and forth. The current inside the tank is Q times greater than the fundamental current component that injects into it. Thus, if there is a slight mismatch between the corers, if the interconnect resistance is small enough, a small circulating current of the fundamental frequency will pass through the interconnect wire to balance the core and cause it to oscillate at the same frequency.

IV. Simulation Result and Discussions

The dual-core HSCC oscillator is implemented in Samsung 65 nm CMOS. Its chip layout is shown in Fig. 3. The measured output frequency range is from 1.12 GHz to 1.25 GHz, yielding 10.8% tuning range. Simulated phase noise (PN) is plotted in Fig. 4. In case of a dual core, the R_P value is half, so the phase noise is reduced by 3dB compared to a single core. Simulated phase noise and FOM are -135.0 dBc/Hz and 194 dB at 1 MHz offset. Table I compares it with other recently published state-of-the-art CMOS oscillators.

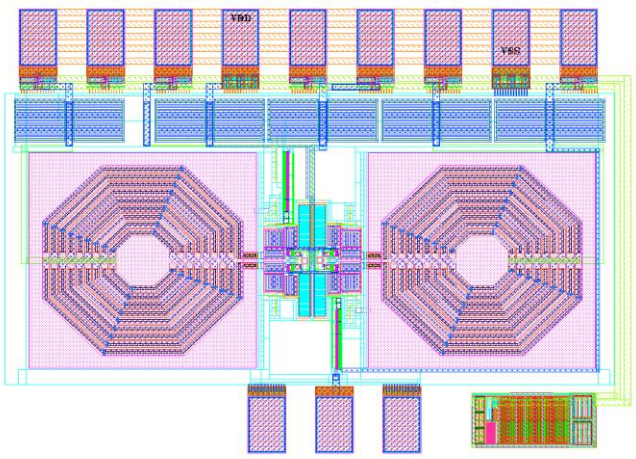

Fig. 3. Chip layout of dual-core high-swing class-C (HSCC) oscillator

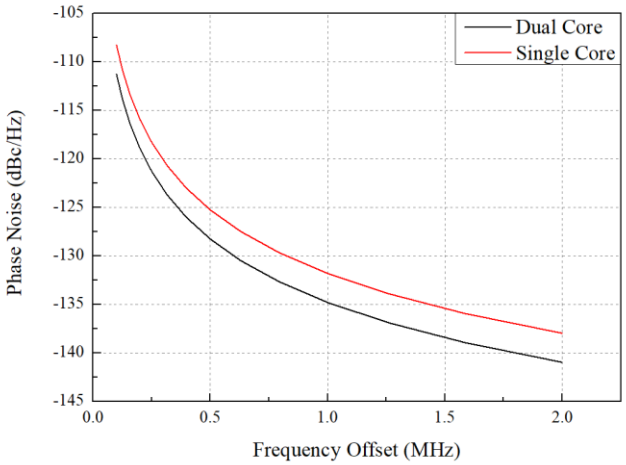

Fig. 4. Simulation results of phase noise of dual-core oscillator and single-core oscillator

The total estimated Q from a post-layout simulation is around 15. The cross-coupled thick-oxide transistors are sized at (40 μm/65 nm). It ensures safe start-up with a reasonable margin for worst case conditions and proper class-C operation. The current mirror ratio should also be chosen carefully (in this design, 4) and its bias capacitance should be chosen properly to avoid voltage squegging. The oscillator drains 1.7 mA from a 1.2 V power supply. Thick oxide devices are used instead due to transistor break down issues.

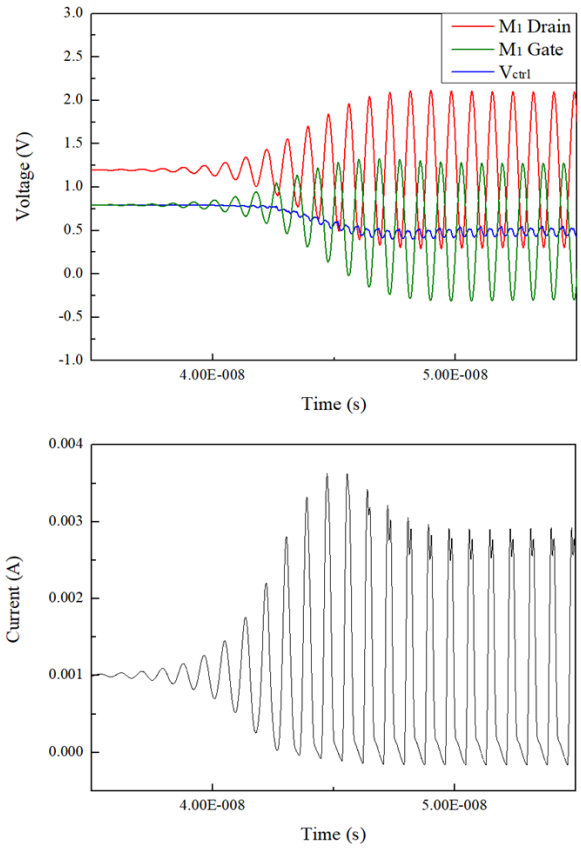

Fig. 5. Transient simulation results of start-up wave forms; (a) voltage of transistor drain, gate, and Vctrl (b) Transistor drain current

TABLE I. Performance summary and comparison with state-of-the-art

	This Work	JSSC'13 [1]	JSSC'13 [2]	JSSC'15 [3]	JSSC'06 [17]
Technology (nm)	65	65	65	65	90
Tuning range (%)	10.8	25	48	18.8	24.3
Frequency (GHz)	1.12	3.7	4.8	4.2	0.92
Phase noise @ 3MHz (dBc/Hz)	-144	-133	-136	-142	-149
Supply voltage (V)	1.2	1.25	0.5	1.3	1.4
Current (mA)	1.7	12	14	32	18
FOM (dB)	194	192	191	191	185

V. Conclusion

To further improve the phase noise (PN) performance of CMOS oscillators, we designed a dual-core a high-swing class-C oscillator.

This approach can be extended to a higher number of cores and to allow reaching far beyond the state-of-the-art phase noise levels at the expense of power consumption and area. The proposed oscillator was implemented in Samsung 65 nm CMOS process.

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