

# A 6-bit Digitally Controlled Vector-Sum Phase Shifter with Current Steering Architecture

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**Abstract** - This paper presents a 6-bit Ku-band vector-sum phase shifter (VSPS) designed for beamforming applications operating in the 10.7–12.7 GHz range. A two-stage RC polyphase filter is adopted for quadrature signal generation, achieving a maximum gain imbalance of 0.218 dB and a maximum phase error of 1.636°, outperforming RL-based alternatives in integration and broadband accuracy. The core uses a digitally controlled current-steering architecture with MOSFET-based RF cells that synthesize precise phase states via binary-weighted vector summation. This structure enables 5.625° resolution, compact layout, and low power operation. Post-layout electromagnetic(EM) simulations show RMS phase errors under 2.5°, gain errors between 0.3 to 0.5 dB, and average gain from -4.55 to -2.17 dB. With only 15.8 mW DC power consumption, the design is efficient and scalable. The proposed architecture combines high resolution, low power, and robust performance, making it well-suited for next-generation phased-array systems in Ku-band satellite communications.

**Keywords**—Current steering, phase shifter, RC polyphase filter, vector-sum architecture

## I. INTRODUCTION

The explosive growth of satellite communications, driven by high-throughput geostationary (GEO) and low Earth orbit (LEO) satellite networks, has increased the demand for compact, low-profile, and electronically steerable antennas operating in the Ku-band downlink frequency range from 10.7 GHz to 12.7 GHz. Phased array antennas are particularly well-suited for this application due to their ability to provide beam agility without mechanical movement. In such systems, broadband and low-loss phase shifters are critical components for achieving high-gain, directionally controllable beams.

Numerous efforts have been made to realize efficient Ku-band phased arrays in this frequency range. For example,

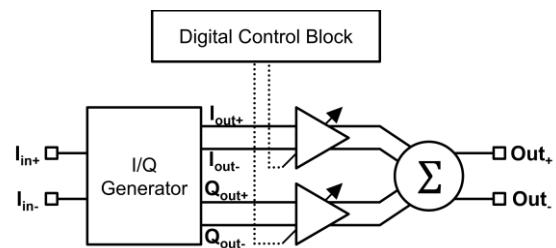


Fig. 1. Block diagram of the VSPS.

dual-polarized 1024-element arrays with embedded transmit-rejection filters have been developed to achieve system G/T values exceeding 10 dB/K while operating from 10.7 GHz to 12.7 GHz [1], [2]. Alternative architectures using meta-surface-based antennas have shown promising results in enhancing aperture efficiency and gain [3]. Compact vehicle-mounted systems using electromagnetic bandgap (EBG) decoupling structures have also been proposed to reduce inter-element coupling and improve pattern integrity [4].

On the circuit level, wideband receivers incorporating temperature-compensated beamforming architectures [5] and low-noise amplifiers with absorptive matching networks [6] have been introduced to meet the strict link budget and linearity requirements of satellite systems. Additionally, miniaturized channel amplifiers integrating analog gain control circuits have demonstrated low-mass and power-efficient solutions for Ku-band repeater systems [7]. Other works have explored compact, electronically steerable flat antennas for digital video broadcasting(DVB) satellite reception, utilizing IF beamforming to simplify RF complexity [8].

Despite these advancements, there remains a need for high-performance Ku-band phase shifters that can support wideband operation, low insertion loss, and high phase linearity, especially for integration into dense planar phased arrays. In this work, we present a Ku-band phase shifter designed specifically for operation from 10.7 GHz to 12.7 GHz, targeting satellite downlink applications. The design balances compactness, phase resolution, and integration compatibility, contributing to the broader effort toward high-performance and cost-effective electronically steerable antennas for next-generation SATCOM systems.

This paper is organized as follows. Section II details the

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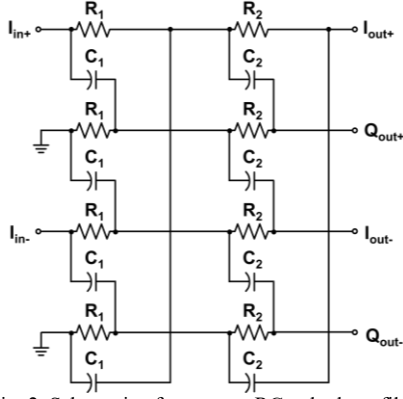


Fig. 2. Schematic of two-stage RC polyphase filter.

TABLE I. Passive Elements Parameters in the Rc Polyphase Filter

R1	C1	R2	C2
100 $\Omega$	100 fF	150 $\Omega$	100 fF

design of the RC polyphase filter. Section III introduces the proposed phase shifter architecture and its circuit implementation. Section IV presents EM simulation results, and Section V concludes the paper.

## II. RC POLYPHASE FILTER

To enable accurate quadrature signal generation from a differential input in the proposed vector-sum-based phase shifter, a passive I/Q generator is required. Among the available techniques, RL filters, transformer-based quadrature couplers, and RC polyphase filters are commonly used. In this work, an RC polyphase filter is adopted due to its superior integration capability, compact layout, and consistent performance across a wide frequency range.

Although RL filters and transformer-based quadrature couplers can generate phase shifts, their dependence on on-chip inductors leads to several disadvantages. These include large area consumption, high sensitivity to process and temperature variations, and increased phase and amplitude errors over wide frequency ranges [9]. Also, at high frequencies such as those in the Ku-band, inductors become excessively large and exhibit frequency-dependent inductance variations, which hinder the realization of accurate phase shifts.

In contrast, the RC polyphase filter provides an inductorless solution that is well-suited for BiCMOS implementation. Its simple structure facilitates the cascading of multiple stages, thereby enabling wideband operation with low phase error and minimal amplitude mismatch between signal paths. Furthermore, RC polyphase networks inherently provide broadband 90° phase-shifted outputs while exhibiting reduced sensitivity to parasitic effects and component mismatches [10], [11].

In this work, a two-stage RC polyphase filter is designed to operate within the 10.7–12.7 GHz Ku-band, targeting quadrature signal generation for the phase shifter. The schematic of the implemented filter is shown in Fig. 2. Fig.

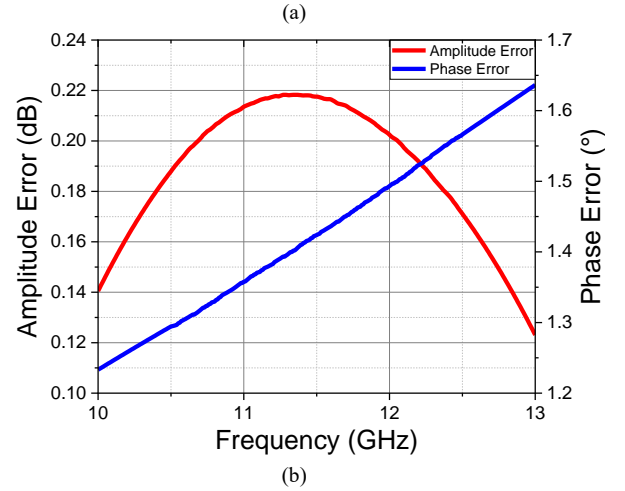
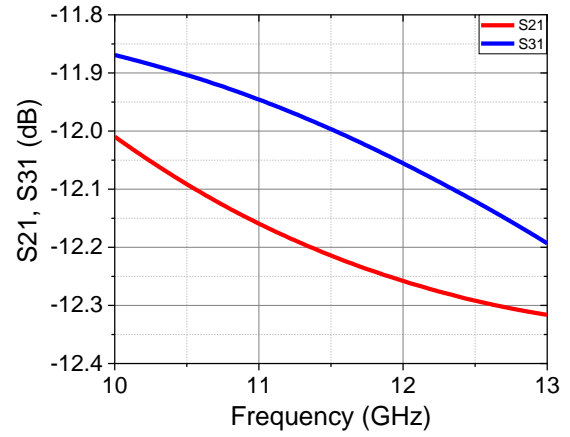


Fig. 3. EM simulation results of RC polyphase filter. (a) S21 and S31, and (b) amplitude and phase error.

3(a) illustrates the insertion loss, while Fig. 3(b) presents the simulated amplitude and phase errors. Post-layout EM simulation results confirm that the proposed filter achieves excellent performance over the target frequency band, with a maximum amplitude error of 0.218 dB and a maximum phase error of 1.636°.

## III. PROPOSED PHASE SHIFTER DESIGN

### A. Vector-Sum Network Architectures

Phase shifters based on the vector-sum architecture have been widely adopted in millimeter-wave phased-array systems due to their compact structure and high-resolution phase control capability. Representative implementations include Gilbert cell-based vector modulation and cascode current-steering vector modulation. The Gilbert cell structure adjusts the amplitude and phase of I/Q signals by steering differential currents between the upper branches of stacked transistors. Amplitude control is achieved by varying the tail current source, and polarity switching is realized using digital logic. This structure is compact and provides full 360° phase coverage. However, the stacked transistors reduce voltage headroom, which can degrade linearity at high frequencies. Moreover, the input impedance varies across different phase states, potentially leading to gain and phase distortion [12].

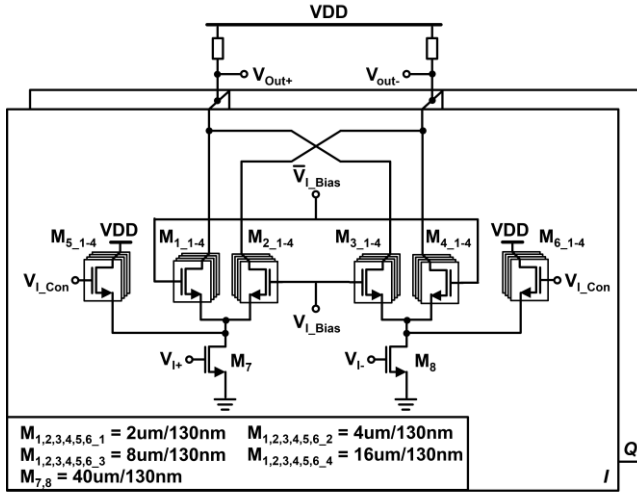


Fig. 4. Schematic of the proposed current steering RF cell array.

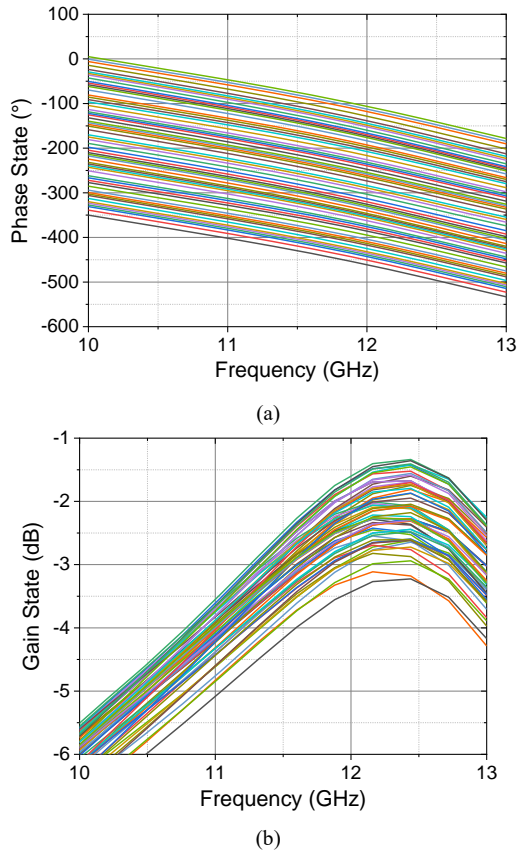


Fig. 5. Simulated results of the proposed VSPS. (a) phase state and (b) gain state.

The cascode current-steering vector modulator operates by steering current between the main signal path and a dummy path to control the gain. This architecture maintains a nearly constant input impedance regardless of the gain state, ensuring stable impedance matching with the preceding quadrature generator and improving the overall accuracy of vector modulation. The impedance-invariant characteristic is particularly advantageous in high-frequency vector modulation, contributing to the minimization of phase and gain errors [13]. Therefore, this work adopts the cascode current-steering vector modulation technique.

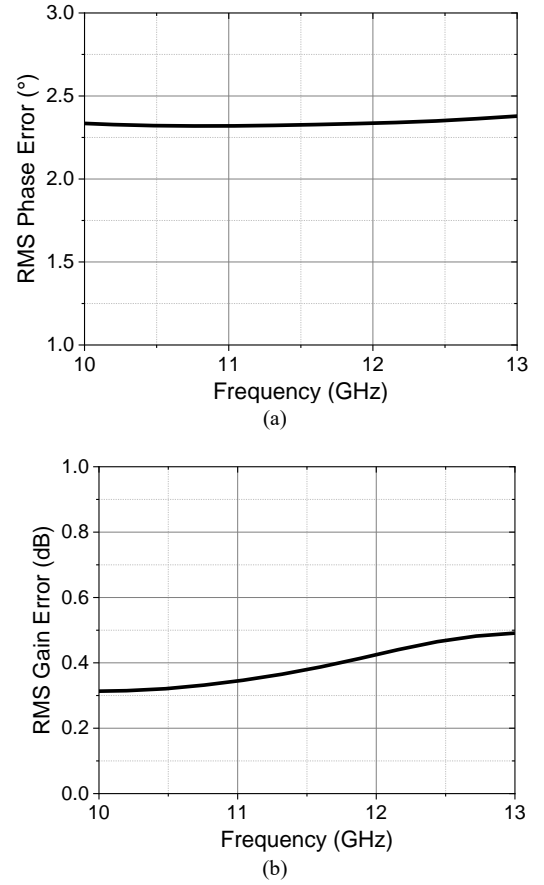


Fig. 6. Simulated results of the proposed VSPS. (a) RMS phase error and (b) RMS gain error.

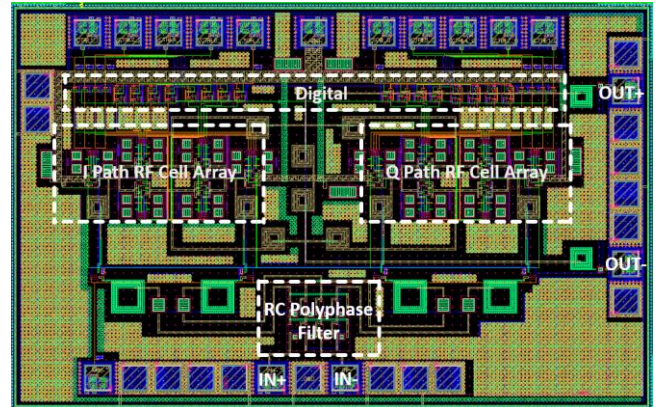


Fig. 7. Layout of the VSPS.

### B. Proposed Current Steering Array

Conventional current-steering vector modulators control the tail current during vector weighting, which leads to dependent power consumption and variations in the input and output impedance. To address this, we propose a digitally controlled, unit-MOSFET RF cell-array phase shifter, as shown in Fig. 4. Each RF cell forms a cascode current path and is selectively enabled by digital control to contribute a weighted vector component along the I or Q signal. The architecture maintains nearly constant impedance while stabilizing power consumption. Digital

TABLE II. Performance Summary and Comparison of Phase Shifter

	JSSC 2007 [14]	MTT-S 2010 [15]	TMTT 2013 [16]	MWCL 2016 [17]	MWCL 2018 [18]	TCAS-2 2021 [19]	MWTL 2023 [20]	This Work
Technology	0.13um CMOS	0.18um BiCMOS	0.18um BiCMOS	0.25um BiCMOS	0.13um CMOS	0.18um BiCMOS	0.13um SOI	<b>130nm BiCMOS</b>
Frequency [GHz]	15~26	6~18	15~35	8~12	8~12	8~12	8~12	<b>10.7~12.7</b>
Vector Modulation Topology	Gilbert cell	Gilbert cell	Gilbert cell	Digital current steering	Gilbert cell	Gilbert cell	Gilbert cell	<b>Digital current steering</b>
Phase Resolution (bits)	4	5	4	6	6	5	6	<b>6</b>
Phase Control Range (°)	360	360	360	360	360	360	360	<b>360</b>
RMS Phase Error (°)	6.5~16	<5.6	4.2~13	<6.4	<4	<4.6	<0.29	<b>&lt;2.5</b>
RMS Amplitude Error (dB)	1.1~2.1	<1.1	1~2.2	<2	<0.9	<0.6	<0.24	<b>0.3~0.5</b>
Avg. Gain (dB)	-4.6~-3	<19.5	-13.5~5	<-2.5	-2.5~1	<1.75	-3.1~-0.8	<b>-4.55~-2.17</b>
Power Consumption (mW)	11.7	61	25.2*	110	37.5	73.92	90	<b>15.8</b>
Area (mm <sup>2</sup> )	0.75×0.6	1.2×0.75	0.52×0.37**	1.87×0.88**	0.75×0.32**	0.11×0.65**	1.7×0.54	<b>1.75×1.11</b>

\* Does not include active balun

\*\* Does not include pad

control selects the I or Q path and drives binary-weighted bits through AND, NAND gates and inverters, such that the total current drawn by the RF cell array remains essentially constant across all codes.

#### IV. RESULTS AND DISCUSSIONS

The proposed 6-bit current-steering-based VSPS was validated through post-layout EM simulations over a frequency range of 10.7–12.7 GHz. The layout of the phase shifter is shown in Fig. 7. Phase control and the arrayed transistors are managed by a digital circuit, with the supply voltage ranging from 1.2 V to 3.3 V. The circuit provides 64 discrete phase states across the full 360° range, corresponding to a phase resolution of 5.625°. As shown in Fig. 5, all 64 phase and gain states are presented. A small amplitude and phase imbalance in the RC polyphase filter causes a vector-combining loss, leading to slight, frequency-dependent fluctuations in the gain states. Nevertheless, the proposed design meets the 3-dB bandwidth requirement across 10.7–12.7 GHz.

The simulated root-mean-square (RMS) phase and amplitude errors are shown in Fig. 6. The RMS phase error reaches a maximum of 2.5°, while the RMS gain error ranges from 0.3 dB to 0.5 dB. These low phase and amplitude errors ensure accurate beam steering and contribute to maintaining a uniform radiation pattern in antenna array systems.

Furthermore, the design achieves low power consumption by employing a current-steering technique, consuming only 15.8 mW of DC power. This efficiency is enabled by a digitally controlled RF cell array architecture, which minimizes unnecessary current paths and eliminates the need for analog bias tuning, thereby allowing fully digital control.

#### V. CONCLUSION

This paper presented a 6-bit phase shifter based on a current-steering vector-sum architecture and validated its performance through post-layout EM simulations. A two-stage RC polyphase filter for quadrature signal generation achieved a maximum gain imbalance of 0.218 dB and a maximum phase error of 1.636° over 10.7–12.7 GHz, confirming wideband phase accuracy. The current-steering implementation with a digitally controlled MOSFET-based RF-cell array provides impedance stability and scalability, enabling precise phase synthesis via binary-weighted summation.

Post-layout EM results show RMS phase error  $\leq 2.5^\circ$ , RMS amplitude error of 0.3–0.5 dB, average gain from –2.17 dB to –4.55 dB, and total DC power of 15.8 mW. These metrics demonstrate suitability for low-power, high-frequency phased-array systems and highlight the benefits of passive I/Q generation combined with digital vector modulation for high resolution and robust signal integrity.

Future work includes silicon fabrication and measurement, calibration for process-voltage-temperature variations, further optimization of linearity and noise, and integration with large-scale arrays for beamforming experiments.

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