A Multi-Path Hybrid DC-DC Converter with Reduced Inductor Current and Wide Voltage Conversion Ratio

Jaekyun Kim and Chulwoo Kim
Department of Electrical and Electronic Engineering, Korea University
E-mail : kjk@kilby.korea.ac.kr, ckim@korea.ac.kr

***Abstract* - This paper presents a 5V input DC-DC converter using a proposed dual-path structure. By leveraging the benefits of a multi-path architecture, the converter reduces inductor's DC current. The topology comprises one inductor, eight power switches, and four flying capacitors, with each path including two to three power switches in series. This structure reduces the inductor's DC current stress, enabling the use of a compact inductor without sacrificing efficiency. The proposed converter supports a voltage conversion ratio (VCR) range of 0 to 1 and is implemented in TSMC 180nm BCD process, occupying a 3.55 mm × 2.36 mm silicon area.**

***Keywords*— Hybrid DC–DC converter, multi-path, Step down converter**

I. INTRODUCTION

As the demand for higher current in system-on-chip (SoC) devices, particularly in wearable and IoT applications, continues to rise, conduction losses in inductors have become a key factor limiting overall efficiency.[1] These losses are proportional to the square of the RMS current (I_{rms}^2) multiplied by the DC resistance of the inductor (R_{DCR}).[2] To address this challenge, we introduce a hybrid dual-path topology incorporating flying capacitors, which helps lower both the voltage and current stresses on the inductor.

Hybrid DC-DC converters have attracted considerable interest due to their capability to support a wide output voltage range without compromising efficiency. While these converters may require larger area footprints and exhibit slower load transient responses, they provide greater voltage flexibility compared to switched capacitor (SC) converters and low dropout (LDO) regulators. Hybrid converter topologies are particularly well-suited for applications requiring precise voltage regulation and the ability to deliver high current efficiently.

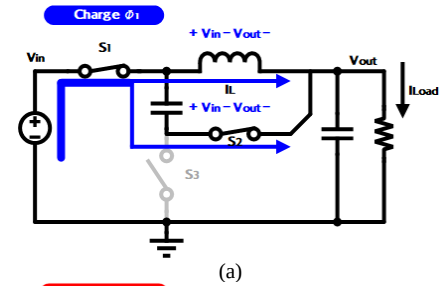
a. Corresponding author; ckim@korea.ac.

Manuscript Received Jul. 31, 2025, Revised Nov. 13, 2025, Accepted Nov. 17, 2025

II. PRIOR WORKS AND PROPOSED CONVERTER

A. Prior Works

In recent years, there has been increasing research into dual-path (DP) and multi-path hybrid buck converters, especially for compact systems that use small inductors. These designs are beneficial in reducing inductor DC resistance (DCR) losses and alleviating stress on the switches. However, current topologies often face a compromise between minimizing the inductor DC current and managing the discharge current of the flying capacitors.



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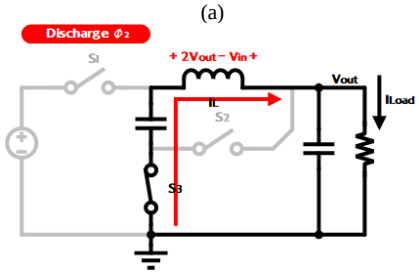

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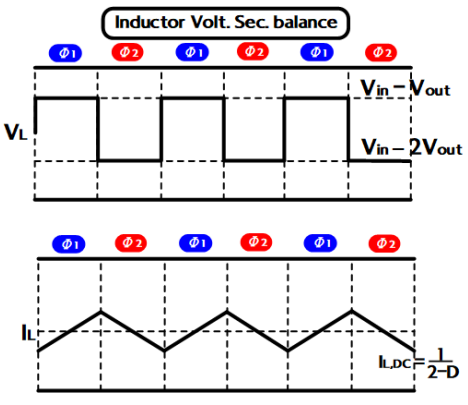
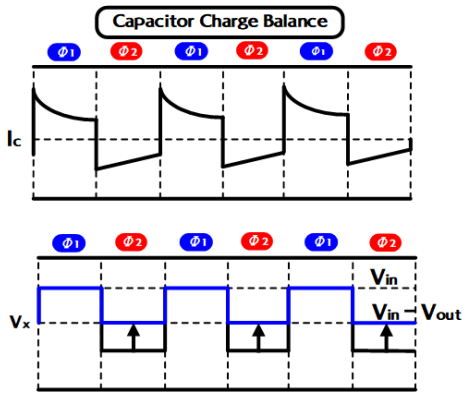




(c)

Fig. 1. Basic Dual path Hybrid DC-DC Converter operation topology (a) during charge phase (b) discharge phase (c) inductor current and flying capacitor current graph.[3]

Fig. 1 illustrates the fundamental topology of a dual-path hybrid DC-DC converter, demonstrating how charge is transferred across both power stages and the corresponding inductor current waveforms. Unlike conventional converters with a single current path, the dual-path configuration allows current to flow through both the inductor and capacitors, thereby reducing the inductor current and its associated losses. This, in turn, enables the use of inductors with higher R_{DCR}.

B. Proposed Work

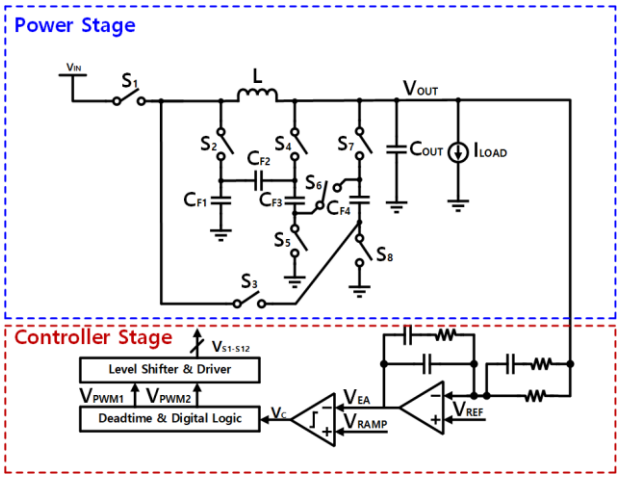
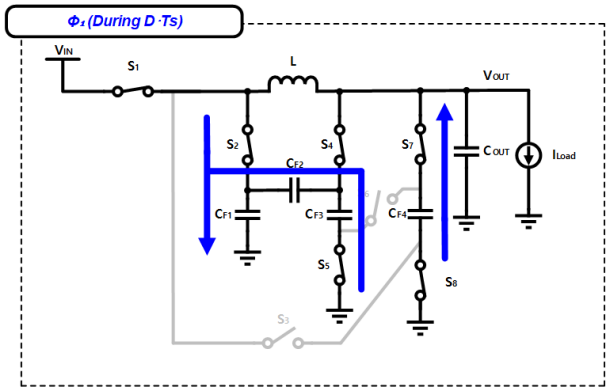


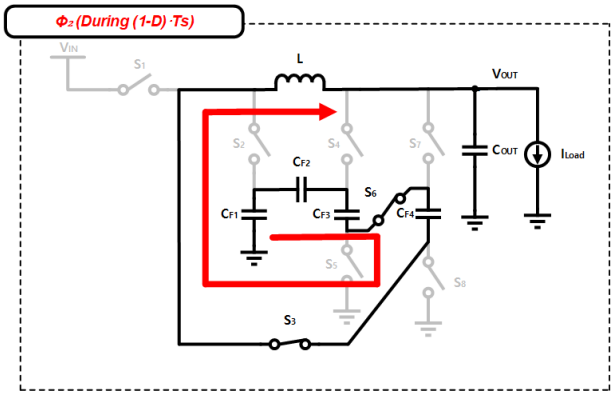
Fig. 2. Proposed Multi-path Hybrid DC-DC Converter top diagram.

Fig. 2 shows the circuit diagram of the proposed multi-path converter. The proposed converter includes one off-chip inductor and four off-chip capacitors in the power stage. The power stage consists of 8 power switches, and it basically operates in two phases: Φ_1, Φ_2.

During the two-phase operation, the output current is delivered through the inductor path and capacitor path. The power stage is controlled by voltage mode control using Type-III compensation. The duty signal is generated by the duty generation circuit which consists of an error amplifier, comparator, sawtooth generator, and digital logic, including minimum duty generation circuit.



(a)



(b)

Fig. 3. Proposed Multi-path Hybrid DC-DC Converter Operation topology (a) Phase 1 (b) Phase 2.

Fig. 3 shows the operation topology during its operating phase. During the first phase which lasts for the duration $D \cdot T_S$ the power stage is connected to Vin. During this phase the inductor is energized, C_{FLY1} charges, and C_{FLY2}, C_{FLY3}, C_{FLY4} discharge. In phase 2 which lasts for $(1-D) \cdot T_S$, the inductor is de-energized, C_{FLY1} discharges, charging C_{FLY2}, C_{FLY3}, and C_{FLY4}. As the power stage has a multi path structure, the inductor DC current is reduced. When a heavy load condition occurs, the primary cause of efficiency degradation in the DC-DC converter is conduction loss ($I_{Load}^2 \times R_{Loss}$), where R_{Loss} is the total resistance, typically consisting of the power switch's on-resistance (R_{ON}) and the inductor DC resistance. Additionally, chip inductors tend to have a much larger R_{DCR} compared to R_{ON}. Therefore, reducing the inductor current helps to minimize efficiency losses.

We can derive the voltage conversion ratio (VCR) of the proposed topology using inductor voltage second balance equation. As shown in Fig. 3 (a) the voltage across the inductor V_L is $V_{IN} - V_{OUT}$ during Φ_1. The inductor slew rate (SR) for Φ_1 is therefore

$$SR_{\Phi_1} = \frac{V_L}{L} = \frac{V_{IN} - 5V_{OUT}}{L} \quad (1)$$

Fig. 3 (b) shows Φ_2, and V_L is $-2V_{OUT}$. The inductor slew rate (SR) for Φ_2 is therefore

$$SR_{\Phi_2} = \frac{V_L}{L} = -\frac{V_{OUT}}{L} \quad (2)$$

By applying the inductor volt-second balance rule, the sum of the volt-seconds over one complete switching cycle must be zero which leads to

$$\mathrm{SR}_1 \cdot (\mathrm{D} \cdot \mathrm{T_S}) + \mathrm{SR}_2 \cdot ((1 - \mathrm{D}) \cdot \mathrm{T_S}) = 0 \quad (3)$$

$$\left(\frac{V_{IN}-V_{OUT}}{L}\right) \cdot D \cdot T_S + \left(-\frac{2V_{OUT}}{L}\right) \cdot (1-D) \cdot T_S = 0 \quad (4)$$

$$(V_{IN} - V_{OUT})D - 2V_{OUT}(1-D) = 0 \quad (5)$$

$$VCR\left(\frac{V_{OUT}}{V_{IN}}\right) = \frac{D}{2-D} (0 \le D \le 1) \quad (6)$$

$$\therefore\ 0 \le VCR \le 1$$

From this we can see that VCR is always between 0 and 1, providing a flexible and efficient voltage conversion ratio. This ability to support a wide VCR enables the converter to efficiently operate across a variety of input and output voltage conditions, making it well-suited for diverse applications requiring both high efficiency and wide voltage regulation.

In order determine the average inductor current (I_L) relative to I_{Load}, we apply the principle of power conservation, assuming ideal converter efficiency.

$$P_{IN} = P_{OUT} \quad (7)$$

$$V_{IN} \cdot I_{IN} = V_{OUT} \cdot I_{OUT} \quad (8)$$

I_{IN} is the average current drawn from the input source which is the sum of all average current s drawn from the input. The input current during Φ_1 and Φ_2 are

$$I_{IN,\Phi1} = I_{L,\Phi1} + I_{C,\Phi1} \quad (9)$$

$$I_{IN,\Phi2} = I_{C,\Phi2} \quad (10)$$

Therefore the total average current is

$$I_{IN} = D \cdot I_{IN,\Phi1} + (1-D) \cdot I_{IN,\Phi2} \quad (11)$$

$$I_{IN} = D \cdot I_L + [(D \cdot I_{C,\Phi1} + (1-D) \cdot I_{C,\Phi2})] \quad (12)$$

By the principle of capacitor charge balance (CCB), the net charge drawn by any flying capacitor over a full cycle must be zero in steady-state. Therefore, the bracketed term equals zero. This will lead to

$$I_{IN} = D \cdot I_L \quad (13)$$

Substitute this result back into the power balance equation,

$$V_{IN} \cdot (D \cdot I_L) = V_{OUT} \cdot I_{Load} \quad (14)$$

By substituting VCR derived before shows the relationship of

$$I_L = \frac{1}{D} \cdot \frac{V_{OUT}}{V_{IN}} \cdot I_{Load} = \frac{1}{2-D} \cdot I_{Load} \quad (15)$$

This equation demonstrates the key benefit of the proposed topology: since the duty cycle D is always less than 1, the denominator (2 - D) is always greater than 1. Consequently, I_L is always smaller than the I_{Load}, which directly reduces the conduction losses associated with the inductor's DCR.

The deadtime generator generates the non-overlapping V_{PWM1} and V_{PWM2} signals, which defines Φ_1 and Φ_2. It inserts a dead-time between these signals, ensuring that a switch in a complementary pair is fully turned off before the other begins to turn on to avoid direct connection from V_{IN} to V_{SS}, thereby preventing shoot-through current.

III. RESULTS AND DISCUSSION

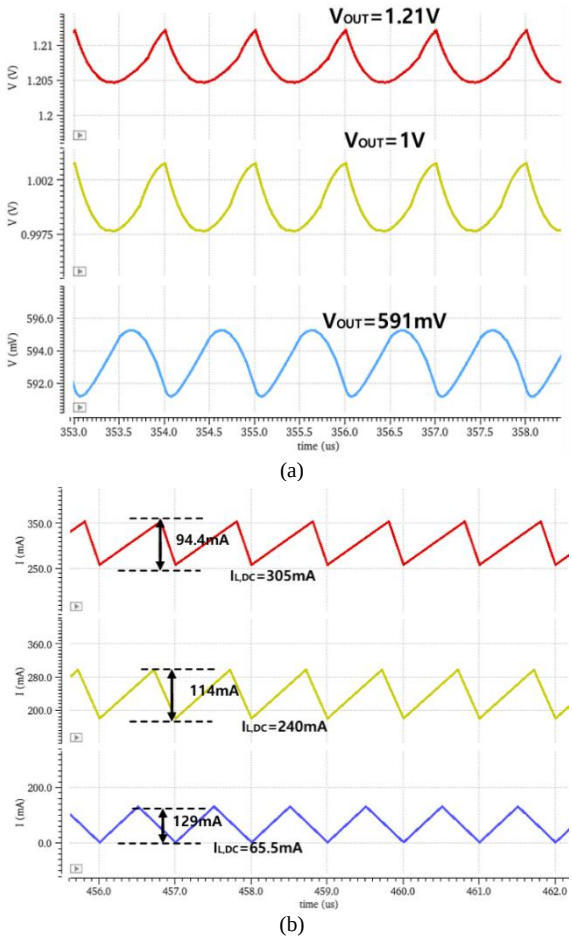


Fig. 4. Simulated waveform of Proposed Multi-path Hybrid DC-DC Converter (a) VOUT and (b) Inductor current when VOUT = 1.21 V, 1 V, 591 mV.

The switching frequency of the proposed converter is 1 MHz, the off-chip inductor value is 4.7 µH which has a value of DCR is 313 mΩ, and the off-chip flying capacitor each has a value of 4.7 µF where the output capacitor has a value of 10 µF. Fig. 4. shows a simulated V_{OUT} and I_L waveform of the proposed converter. With a duty ratio of 0.38, 0.33, 0.21 the output voltages were measured at 1.21 V, 1 V, 591 mV respectively. Fig. 4(b) shows the waveform of inductor current. Each current is shown for V_{OUT} = 1.2 V, 1 V, 591 mV. The load was fixed as a 0.4Ω

resistor, leading currents for each voltage were 510mA, 450mA, 130mA. The inductor DC current is 305 mA, 240 mA, 65.5 mA which is significantly reduced compared to conventional buck converters by the figure of 40%, 46%, 49% respectively, following the inductor current reduction equation.

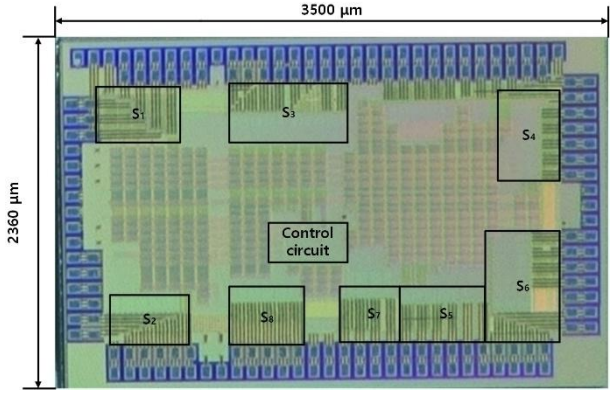


Fig. 5. Chip Layout

Fig. 5 shows the layout of the proposed multi-path hybrid DC-DC converter. To handle high load currents, the power switches are designed with an appropriately large size. These switches are positioned along the pad lines in a way that minimizes the length of the power delivery metal traces, which helps reduce parasitic resistance and improves the overall efficiency of the power conversion process.

To optimize the balance between conduction loss and switching loss, the size of the power transistors is carefully selected to minimize overall energy loss. The control circuitry is placed centrally in the chip layout to shorten the routing paths for control signals to the power stage, thereby enhancing signal integrity and response time. Furthermore, the phase generator block, which is implemented in digital logic, is strategically positioned to ensure proper timing alignment between the control circuitry and the corresponding switching cells. The total area of the implemented design is approximately 4.58 mm². An off-chip inductor was implemented with inductance of

IV. CONCLUSION

TABLE I. Comparison with State-of-the-Art Multi-Path Hybrid DC—DC Converters

	JSSC '19[3]	TPE '15[4]	TPE '23[5]	JSSC '24[6]	This work
Process	180nm CMOS	130 nm BCD	65nm CMOS	65 nm CMOS	180 nm BCD
Topology	DPDC	Multiphase	ACOT FCML	DIL	Multi-path hybrid
V_{IN} (V)	4.5	2.8 – 5	2.7 – 4.5	2.8 – 5	5
V_{OUT} (V)	0.8-4.0	0.68 – 1.92	0.6 – 1.3	0.3 – 1.2	0.3 – 3.5
$I_{OUT,max}$ (A)	1.6	4	1.6	1.5	1.5
L (uH)	4.7	4 x 0.47	0.47	2 x 0.47	4.7
DCR(mΩ)	250	40	15	64	313
f_{sw} (MHz)	1	2.25	2.5	2	1
C_{OUT} (uF)	10	88	10	4.7	10
Peak Eff (%)	96.2	85.5 @ Vin=5V	88.6	90.6	73.2

Table I presents the summarized specifications of the proposed hybrid DC-DC converter. The power stage is composed of one inductor and four flying capacitors. The proposed Multi-path Hybrid DC-DC Converter reduces the inductor current, so it reduces energy loss. Moreover, the proposed cfbonverter achieves a wide VCR ranging from 0 to 1, enabling efficient operation across diverse input and output voltage conditions.

ACKNOWLEDGMENT

The chip fabrication and Electronic Design Automation (EDA) tool were supported by the IC Design Education Center (IDEC), Daejeon, South Korea.

REFERENCES

[1] Y. Zeng, and H. -z. Tan, "Fast-Transient DC-DC Converter using an Amplitude-Limited Error Amplifier with a Rapid Error-Signal," in IEEE International Symposium on Circuits and Systems(ISCAS), Sapporo, Japan, 2019, pp. 1-5.

[2] K. Hata, Y. Jiang, M. -K. Law, and M. Takamiya, "Always-Dual-Path Hybrid DC-DC Converter Achieving High Efficiency at Around 2:1 Step-Down Ratio," in 2021 IEEE Applied Power Electronics Conference and Exposition(APEC), Phoenix, AZ, USA, 2021, pp. 1302-1307

[3] Y. Huh, S. -W. Hong, and G. -H. Cho, "A Hybrid Structure Dual-Path Step-Down Converter With 96.2% Peak Efficiency Using 250-mΩ large-DCR Inductor," in IEEE Journal of Solid-State Circuits, vol. 54, no. 4, pp. 959-967, April 2019.

[4] Y. -S. Roh, Y. -J. Moon, J. park, M. -G. Jeong, and C. Yoo, "A Multiphase Synchronous Buck Converter With a Fully Integrated Current Balancing Scheme," in IEEE Transactions on Power Electronics, vol. 30, no. 9, pp. 5159-5169.

[5] H. A. Zadeh, H. R. Kooshkaki, K. -Y. Lee, and P. P. Mercier, "An Adaptive Constant-on-Time-Controlled Hybrid Multilevel DC-DC Converter Operating From Li-Ion Battery Voltages With Low Spurious Output," in IEEE Transactions on Power Electronics, vol. 38, no. 5, pp. 5763-5776, May 2023.

[6] A. Mishra, W. Zhu, B. Wicht, and V. De Smedt, "A Dual-Inductor Ladder Buck Converter for Li-ion Battery-Operated Sub-Volt SoCs," in IEEE Journal of solid-State Circuits, vol. 59, no. 2, pp. 563-573, Feb. 2024.

Jaekyun Kim (Graduate Student Member, *IEEE*) received B.S. degree in electrical engineering from Korea University, Seoul, South Korea, in 2024, where he is currently pursuing the M.S. degree.

His research interests include integrated power management system designs and low-power CMOS analog circuit designs, and hybrid dc-dc power converters.

Chulwoo Kim (Senior Member, *IEEE*) received the B.S. and M.S. degrees in electronics engineering from the Korea University in 1994 and 1996, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign in 2001.

In May 2001, he joined IBM Microelectronics Division, Austin, TX, where he was involved in Cell processor design. Since September 2002, he has been with the School of Electrical Engineering, Korea University, where he is currently a Professor. He was a Visiting Professor at the University of California at Los Angeles in 2008 and at the University of California at Santa Cruz in 2012. He is a coauthor of two books, namely, CMOS Digital Integrated Circuits: Analysis and Design (McGraw Hill, 4th edition 2014) and High-Bandwidth Memory Interface (Springer, 2013). His current research interests are in the areas of wireline transceiver, power management, data converters and quantum-inspired computing.

Dr Kim has served on the Technical Program Committee of the IEEE International Solid-State Circuits Conference and as a Guest Editor for IEEE Journal of Solid-State Circuits. He has also held leadership roles including Chair of the SSCS Seoul Chapter, Distinguished Lecturer of the IEEE SSCS (2015–2016), and elected member of the SSCS AdCom at large (2022-2024). He is currently on the editorial boards of IEEE Journal of Solid-State Circuits and Transactions on VLSI Systems.