A Duty-Cycled Continuous-Time Delta-Sigma Modulator for ExG Biopotential Acquisition

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***Abstract*—This paper introduces a continuous-time (CT) delta-sigma analog-to-digital converter (ADC) integrated with a capacitively-coupled chopper instrumentation amplifier (CCIA) for ExG biopotential recording. The design features a duty-cycled operation that enhances power efficiency by minimizing unnecessary power dissipation during low-frequency signal acquisition. The system is optimized to meet key requirements such as low noise, low power, high input impedance, and sufficient input range for various biopotential signals. Fabricated in a standard 0.18 µm CMOS process, the ADC achieves FoM_{SNDR} of 170.1 dB for a 10 kHz bandwidth, consuming 4.5 µW at 0.6 V. The active area is 0.138 mm².**

Keywords—**ADC, Delta-Sigma, Duty-Cycling, Biopotential Acquisition**

I. INTRODUCTION

Biopotential measurement systems such as ECG, EEG, EMG, and ENG—collectively referred to as ExG—are widely used in healthcare and brain-machine interfaces due to their ability to provide valuable physiological insights. Fig. 1 shows representative applications of each ExG signal: ECG for heart disease detection, EEG for neurological monitoring, EMG for muscle diagnostics, and ENG for neural research.

A unified ExG recording IC capable of acquiring all these signals offers advantages such as reduced system complexity and improved user convenience in multimodal sensing systems. However, most existing solutions can only measure specific ExG types.

To support all ExG signals, the system must satisfy various design requirements, including bandwidth, input range, noise, and high input impedance. Conventional systems that target the widest-bandwidth signal (ENG) operate with unnecessarily high performance and power consumption when recording lower-frequency signals like EEG or ECG.

This work presents a duty-cycled CTΔΣM ADC for ExG acquisition. By implementing a duty-cycled operation, the system can efficiently measure all ExG signals while minimizing power.

Each ExG signal has unique challenges: EEG requires flicker noise suppression due to its low amplitude, while ENG demands a wide bandwidth beyond 10 kHz. In wearable applications, large motion and stimulation artifacts (up to 100 mV) require a wide input range to avoid saturation. Furthermore, capturing microvolt-level signals requires input-referred noise below 10-20 μV_{rms}, effective common-mode rejection, input impedance above 100 MΩ, and low-power operation below 10 µW to prevent tissue damage [1], [2], [3].

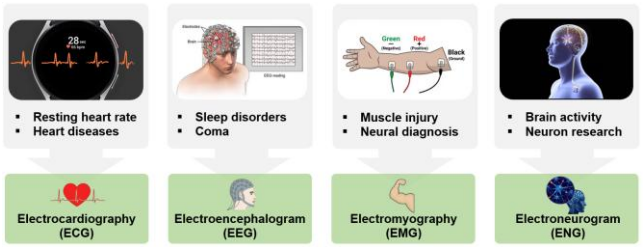

Fig. 1. Necessity of ExG signal acquisition.

II. CONVENTIONAL SYSTEM

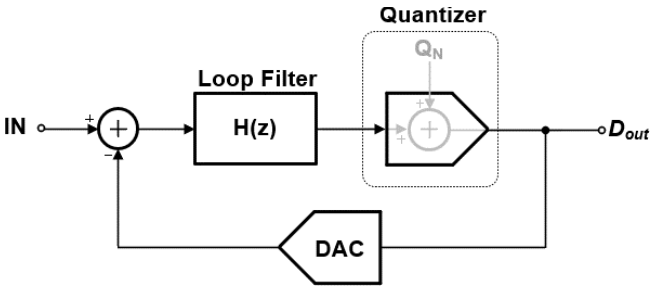

Fig. 2. Block diagram of delta-sigma ADC.

Conventional biopotential acquisition systems typically consist of a high-gain amplifier followed by an ADC [4]. While this architecture reduces the resolution requirement of the ADC, it increases vulnerability to large artifacts such as motion or stimulation-induced saturation. To overcome this limitation, recent designs employ ADC-direct front-ends, where a delta-sigma modulator is directly connected to the body, removing the need for a high-gain amplifier.

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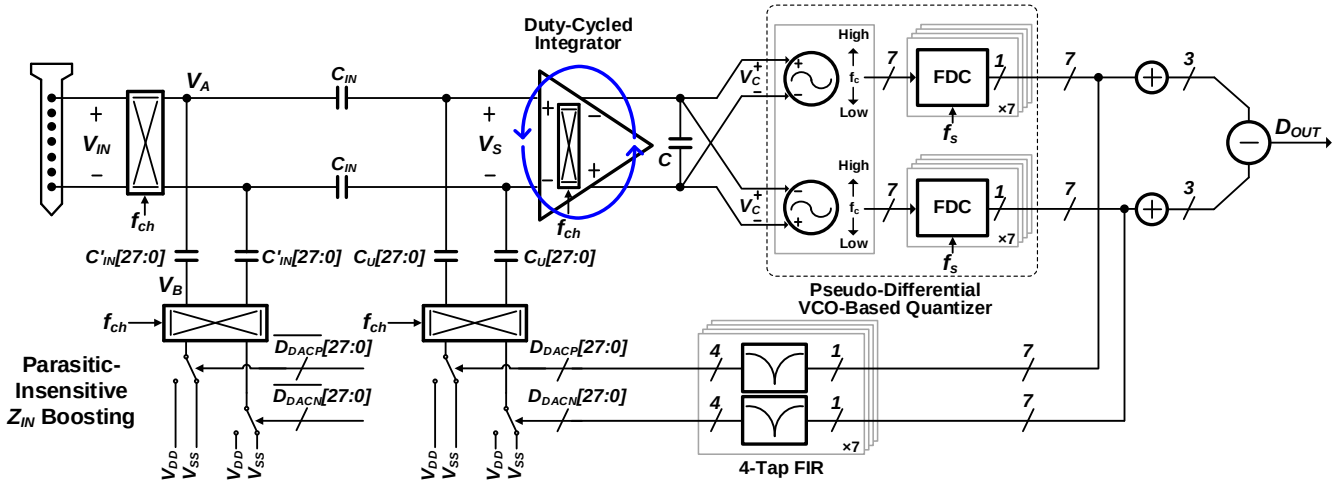

Fig. 3. Overall architecture of the proposed recording system.

Among ADC architectures, delta-sigma modulators (DSMs) are widely adopted for high-resolution signal acquisition due to their use of oversampling and noise shaping. As illustrated in Fig. 2, the DSM consists of a loop filter H(z), a quantizer, and a feedback DAC. The quantization error Q_N is modeled as an additive noise source and shaped by the loop filter in the z-domain. The order of this filter determines the slope of noise suppression within the signal bandwidth.

The in-band quantization noise power spectral density is given by:

$$Q_N = \frac{1}{12} * \Delta^2 * \frac{1}{f_s}, \quad \Delta = \frac{2\pi}{N}$$

where Δ is the quantizer's LSB and f_s is the sampling frequency. Hence, quantization noise can be minimized by increasing the oversampling ratio, increasing quantizer resolution, or using a higher-order loop filter. To meet a noise floor of –140 dB, the proposed system employs second-order noise shaping, a 3-bit quantizer, and an oversampling ratio of 128 for a 10 kHz bandwidth.

III. PROPOSED SYSTEM

Figure 3 shows the architecture of the proposed system. The use of a duty-cycled integrator enables power-efficient operation. A low-noise transconductance amplifier functions as the first integrator, shaping the overall noise characteristics of the loop. The VCO-based quantizer inherently provides first-order noise shaping, and its dynamic element matching (DEM) behavior helps mitigate DAC mismatch.

To suppress flicker noise, chopper stabilization is applied. However, since input impedance degrades with higher chopping frequency, a 4-tap FIR DAC is used to lower the effective chopping frequency while forming a notch at the sampling frequency to suppress quantization noise aliasing. A parasitic-insensitive input impedance boosting (PIIB) technique with positive feedback ensures high input impedance without additional power consumption.

A. Low-noise Linear Trans-Conductance Amplifier (LTA)

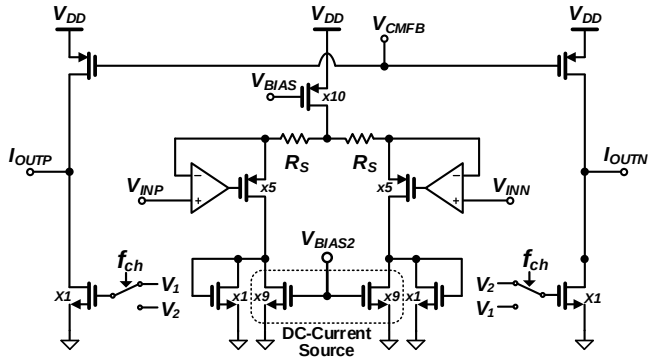

Fig. 4. Schematic of low-noise LTA.

Figure 4 shows the system's first integrator. The first integrator is critical in enhancing the system's noise performance and linearity. Because the system's overall noise characteristics largely depend on the noise behavior of the current-recycling operational amplifier, the integrator incorporates the amplifier to improve its noise performance. The following equation can approximate the input-referred noise of the amplifier:

$$v_{n,in}^2 = v_{n,amp}^2 + v_{n,R_D}^2 + v_{n,I_{DC}}^2$$

Where $v^2_{n,amp}$, $v^2_{n,RD}$ and $v^2_{n,IDC}$ are the input-referred noise of the current-recycling operational amplifier, the degeneration resistor RD, and the DC current source, respectively. Among these, the dominant noise source is the current-recycling operational amplifier, since its gain suppresses other noise contributors. To meet the target noise of 20 μVrms over a 10 kHz signal bandwidth while maintaining high power efficiency, a current-recycling operational amplifier is employed for gm-boosting.

Moreover, chopper stabilization is employed to reduce 1/f noise by modulating the bio-signal into a frequency band with less flicker noise, amplifying it, and then demodulating it back to the original frequency band. Using this technique, the flicker noise can be reduced.

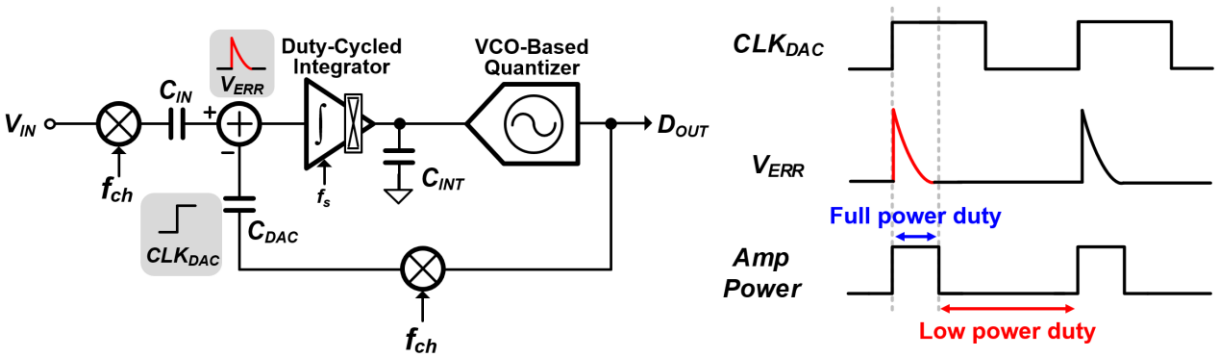

Fig. 5. Basic concept of duty-cycled operation in CTDSM.

And the input-referred thermal noise can be represented as:

$$v_{n,thermal}^2 = \frac{16}{3} \cdot \frac{kT}{g_{mN} + g_{mP}}$$

Where k is the Boltzmann's constant, T is the absolute temperature, and g_{mN} and g_{mP} are the transconductances of the input transistor. This equation shows that increasing the input transistor's transconductance lowers the amplifier's input-referred noise.

Lastly, the VCO operates at $3f_s/4$ to maximize its modulation range. If the VCO parameters are not properly selected, the input range of the quantizer may be limited, leading to nonlinear behavior or output clipping.

B. Duty-Cycled Operation

To reduce analog power consumption without sacrificing performance, the system employs a duty-cycled operation scheme, as illustrated in Figure 5. The key idea is to activate the amplifier at full power only during the conversion phase, where the error voltage (V_{ERR}) occurs at the rising edge of the DAC clock. During non-conversion periods, the amplifier remains in low-power mode, thereby saving power while preserving linearity.

Figure 6 shows the implementation of a duty-cycled amplifier in the first integrator stage. The MOSFET sizing and power duty cycle (25% full-power, 75% low-power) were optimized through simulation to ensure negligible impact on linearity. A safety margin was incorporated in the duty cycle to enhance robustness against PVT variations. As a result, operating the amplifier in low-power mode for 75% of the time enables up to 67% power reduction in the amplifier stage.

However, the reduced amplifier gain during low-power periods may degrade noise performance due to the power–noise trade-off. To mitigate this effect, a noise-shielding technique is applied in the second stage, as shown in Figure 7. Specifically, when operating in low-power mode, 70% of the total resistance is shorted, making the integrator noise less visible at the input. By shorting a portion of the resistor, the thermal noise generated by the resistor is effectively reduced, which further suppresses the overall input-referred noise. Simulation confirms that this technique effectively maintains similar in-band input-referred noise performance even under low-power conditions.

In summary, the proposed duty-cycled operation achieves significant power savings while maintaining linearity and noise performance by dynamically adjusting amplifier activity according to signal conversion timing.

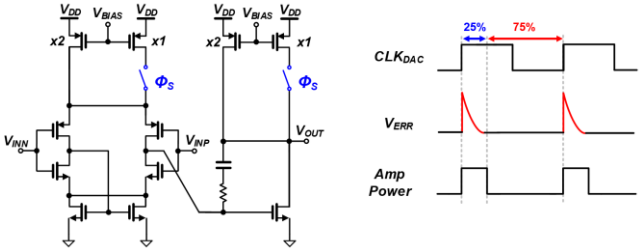

Fig. 6. Duty-cycled amplifier with timing diagram.

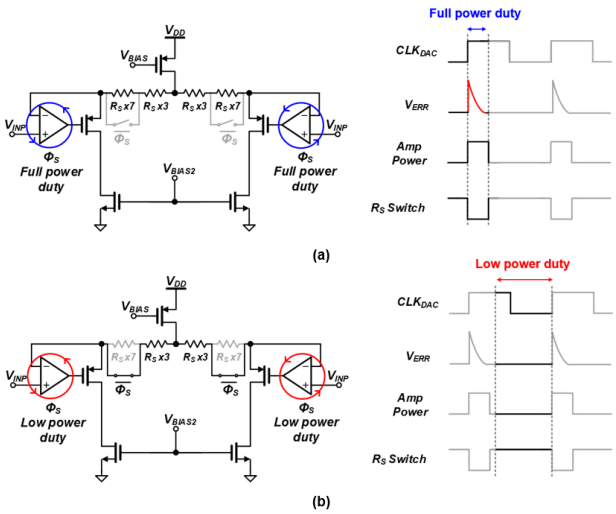

Fig. 7. Duty-cycled integrator of each duty with timing diagram.

IV. MEASUREMENT RESULTS

Figure 8 shows the micrograph of the proposed ExG biopotential recording chip, fabricated in a 0.18 µm standard CMOS process. The chip integrates DACs, VCO-based quantizers, and analog integrators within an active area of 0.138 mm².

To ensure high linearity, particular emphasis was placed on maintaining symmetry in the layout, especially within the DAC section, where mismatch could degrade system performance. In addition, area efficiency was improved by combining MOSCAPs and MIMCAPs to implement key

capacitive elements, such as RC filter capacitors and integrator loads, achieving the required capacitance with minimal footprint. These layout strategies enable a compact, low-power, and high-performance front-end suitable for wearable ExG monitoring applications.

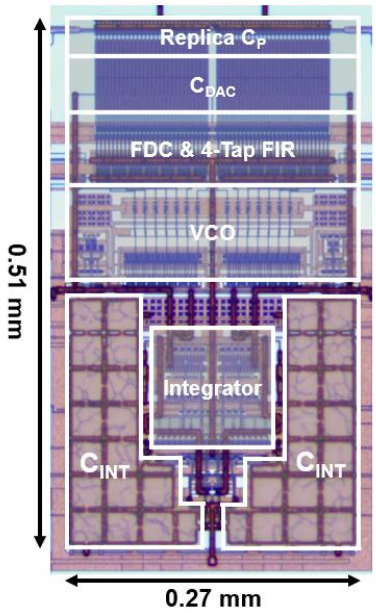

Fig. 8. Proposed chip micrograph.

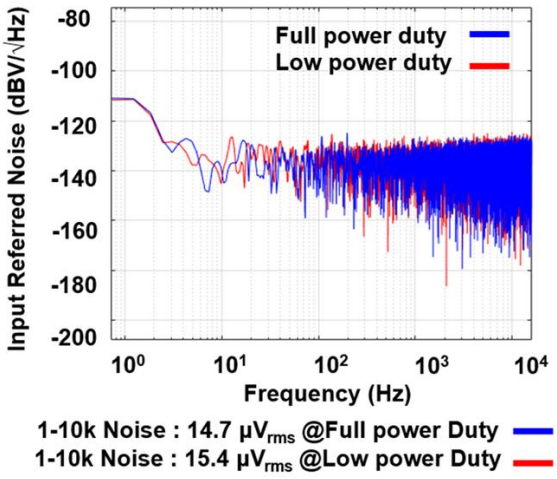

Fig. 9. Measured PSD of input-referred noise.

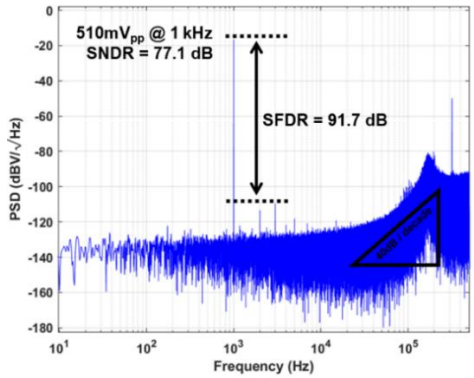

Fig. 10. Measured PSD result.

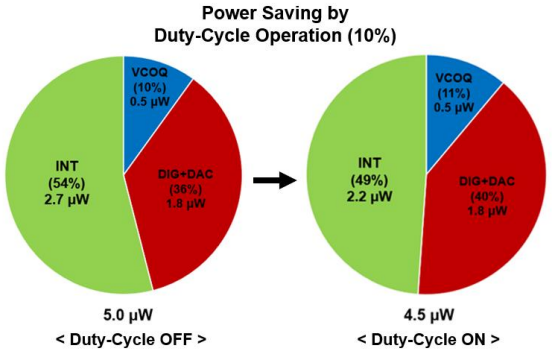

Fig. 11. Measured power consumption of Duty-Cycle OFF and ON modes.

Figure 9 shows the measured power spectral density of the input-referred noise for each duty. One key consideration during the design was ensuring that the noise performance remained consistent for both the full and low power duty. As a result, similar noise performance was achieved across both duties, with input-referred noise measured below 20 μV_{rms}, which is sufficient for accurate ExG biopotential recording.

Figure 10 shows the measured output power spectral density under duty-cycled operation. For input signals of 1 kHz with 510 mV_{pp}, the system achieved SNDR of 77.1 dB with corresponding SFDR above 90 dB. The measured PSD result confirms accurate harmonic characterization and proper noise shaping, with out-of-band noise increasing at 40 dB/decade. The results demonstrate sufficient dynamic range and linearity to support low-amplitude biopotential recording in noisy environments.

Figure 11 presents the measured power consumption in the Duty-Cycle ON and OFF modes. With duty-cycled operation, the total system power decreased from 5.0 µW to 4.5 µW (10 %), and the first integrator—the most power-intensive block—was reduced from 1.5 µW to 1.0 µW (20 %) without degrading SNDR.

This demonstrates efficient operation for accurate biopotential recording (ECG, EEG, EMG, ENG) with minimized power consumption.

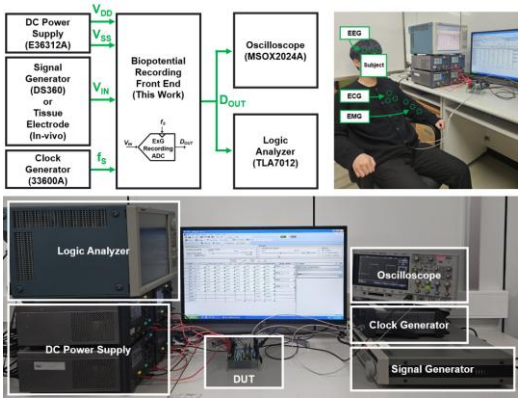

Fig. 11. Measurement setup.

Figure 11 shows the measurement setup. A logic analyzer was employed to record the digital output data, which were subsequently transferred to a laptop for Power Spectral Density (PSD) analysis using MATLAB. An oscilloscope was used to verify the DC power supply voltage and confirm the clock generator's proper operation and D_{OUT}.

TABLE 1. Comparison Table

	ISSCC'20 [5]	ISSCC'21 [2]	ISSCC'22 [1]	CICC'21 [6]	This Work
Technology [nm CMOS]	180	65	180	180	180
Topology	CTΔΣM	CTΔΣM	CTΔΣM	DTΔΣM	CTΔΣM
ExG Recording	No	No	Yes	No	Yes
Duty-Cycle Operation	No	No	No	Yes	Yes
Supply Voltage [V]	1.0	1.2(A)/0.8(D)	0.7	1.5	0.6
Power/Ch [μW]	6.5	5.8	5	2.2 / 4 / 7.1	4.5
Bandwidth [Hz]	10k	1k	10k	400 / 800 / 1.6k	10k
Inp.-Ref. Noise [μV_{rms}]	9.2	3.56	8.5	8.92 / 12.6 / 14.1	15.4
Peak SNDR [dB]	80.4	92.3	85.1	89.3*	77.1
SFDR [dB]	92.2	110	97.0	94.0*	91.7
FOM_{SNDR} / FOM_{DR} [dB]	172.3 / 172.9	174.7 / 174.7	178.1 / 180.3	172.3* / 172.9*	170.1 / 170.6
Peak Input [mVpp]	300	400	560	1400*	510
Z_{IN} @DC [Ω]	∞ @ w/o chopping	60M @ f_{ch}=100kHz	>421M @ f_{ch}=320kHz	-	410 M @ f_{ch}=320kHz
Channel Area [mm2]	0.078	0.075	0.108	0.75	0.138

FOM_{SNDR} = SNDR + 10log(BW/Power) ; FOM_{DR} = DR + 10log(BW/Power) * Bandwidth at 800 Hz

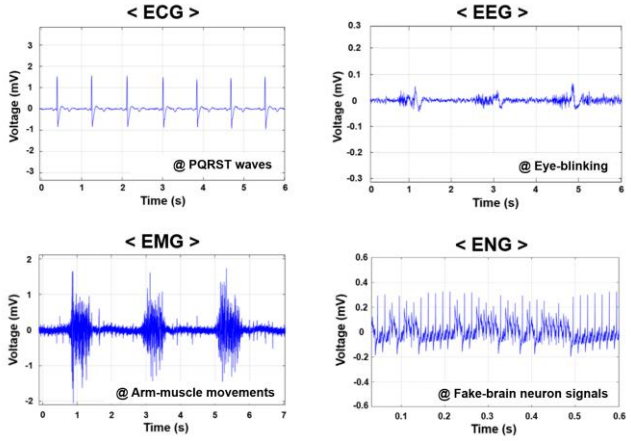

Fig. 12. In-vivo and fake-brain measurement results.

Figure 12 shows the measured ExG signals under duty-cycled operation. ECG, EEG, and EMG were recorded in vivo using surface electrodes placed on the human body, while ENG was measured using a non-invasive "fake-brain" setup. The ECG captures the typical PQRST waveform — where PQRST denotes the characteristic components of an ECG signal, including the P-wave, QRS complex, and T-wave — EEG was recorded during eye blinking, and EMG reflects voluntary arm muscle movements, including contraction and relaxation. The system successfully acquired all signals under appropriate measurement conditions, demonstrating its suitability for comprehensive and accurate ExG monitoring across diverse signal types, including high-frequency signals such as ENG.

The performance of this work is summarized and compared with other state-of-the-art designs in Table 1. The proposed system supports the acquisition of various ExG signals including ECG, EEG, EMG, and ENG. By employing a duty-cycled operation throughout the signal chain, it achieves energy-efficient ExG biopotential recording without compromising signal fidelity.

V. CONCLUSION

In conclusion, we have presented a duty-cycled continuous-time delta-sigma (CTΔΣ) ADC for ExG biopotential acquisition.

By applying duty-cycled operation throughout the analog front-end, the proposed design significantly reduces power consumption while maintaining excellent noise and linearity performance. A low-noise, current-reuse amplifier stage, combined with body-driven VCO-based quantization and a passive-input integrator buffer (PIIB), ensures high input impedance, wide input range, and robust signal integrity.

Fabricated in a 0.18 μm standard CMOS process, the system operates from a 0.6 V supply and occupies an active area of 0.138 mm². It achieves a power consumption of 4.5 μW while maintaining a high FoM_{SNDR} of 170.1 dB. These results demonstrate that the proposed duty-cycled architecture provides an energy-efficient and practical solution for accurate ExG signal monitoring across a range of biomedical applications.

ACKNOWLEDGMENT

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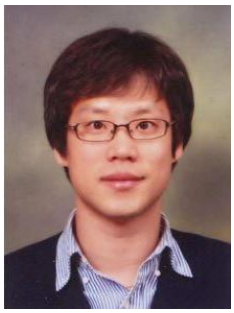

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