Design Study of a 120-GHz Amplifier on InP HEMT Technology

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Abstract - **This paper presents the design and analysis of an amplifier operating at 120 GHz, based on a domestically developed 100 nm InP HEMT process. The maximum available gain (MAG) of three transistor types in the process was compared through simulation. Among them, the 2F20 device exhibited the most stable gain characteristics, making it suitable for high-frequency amplifier design. A single-stage common-source amplifier was fabricated, and its small-signal performance was experimentally verified. The measurement results showed a gain of approximately 3 dB and input and output return loss (|S11| and |S22|) below −4 dB in the target band, which are in good agreement with simulation results. In addition, a planar Marchand balun was designed using a single-metal-layer process. However, the measured insertion loss was significantly higher than predicted by simulation, indicating the need for further research. Finally, a differential two stage amplifier was designed and simulated, achieving a gain of 15.4 dB and a 3 dB bandwidth of 18 GHz at 120 GHz.**

Keywords— **Terahertz Amplifier, Marchand Balun, 100 nm InP HEMT process**

I. INTRODUCTION

The D-band frequency range has attracted considerable attention for next-generation high-frequency applications. Recent advances in semiconductor processing technology have enabled the fabrication of high-frequency circuits with steadily improving output power performance. Research on D-band applications, such as high-speed wireless communication systems, high-resolution radar, and high-precision imaging systems, has grown rapidly in recent years.

To date, most InP-based high-frequency compound semiconductor circuits operating in the submillimeter band, including the D-band, have been fabricated using processes provided by overseas foundries. For example, numerous studies have reported high power gain and excellent linearity in the hundreds of GHz band using InP processes from major foundries. These studies have also demonstrated stable operation in the THz band.

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Most of these high-frequency circuits have relied on overseas fabrication technologies, and no domestic D-band circuits based on InP HEMT processes have yet been reported. This reliance on overseas foundries limits technological independence and process accessibility. However, a 100 nm InP HEMT process has recently been independently developed in Korea, enabling the fabrication of high-frequency amplifiers through a fully domestic process [1].

The InP HEMT process is known to be highly suitable for millimeter-wave and terahertz applications due to its high electron mobility and fast switching speed. Accordingly, research utilizing this newly developed process has been rapidly expanding [2]-[3].

InP-based compound semiconductor processes are widely used in the development of terahertz circuits because of their fast response and excellent output power characteristics at high frequencies. Several studies have reported the simultaneous achievement of high gain and low noise figures even at millimeter-wave frequencies [4]-[5]. These characteristics have established InP HEMT technology as a key enabling technology for future 6G communication systems.

In this study, a circuit was designed using the 100 nm InP HEMT process provided by Quantum Semiconductor International (QSI). A single-stage common-source amplifier was fabricated, and its performance was experimentally characterized. The measured results confirm that the amplifier exhibits the expected power gain and linearity within the D-band, demonstrating its potential as a fundamental building block for more complex phased-array systems or high-performance transceivers.

Although not fabricated in this work, a two-stage amplifier was also designed and analyzed through simulation to explore the potential for further performance enhancement in high-frequency operation. Multistage amplifiers can provide higher power gain than single-stage designs, and recent research has demonstrated that such architectures can achieve higher output power and improved efficiency. These findings suggest that the approach presented in this work can be effectively extended to future terahertz applications beyond the D-band.

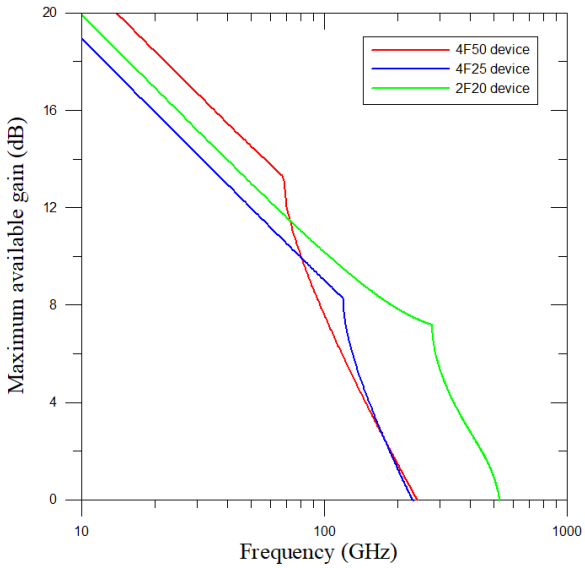


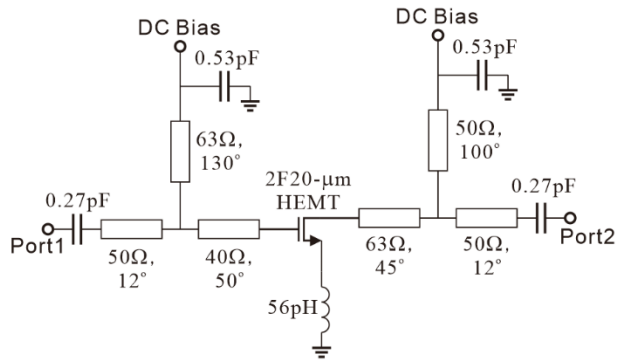
Fig. 1. Simulated maximum available gain (MAG) results for different device geometries

II. TRANSISTOR MAXIMUM GAIN SIMULATION

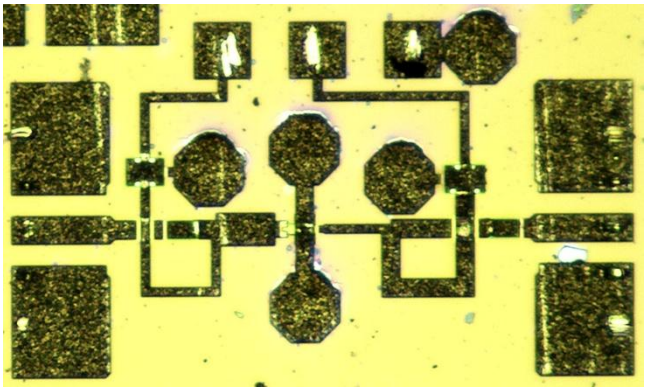
In the amplifier design, we analyzed the frequency characteristics of three transistor structures provided by the 100-nm InP HEMT process: a 4-finger 50 µm device, a 4-finger 25 µm device, and a 2-finger 20 µm device. Simulation results of the Maximum Available Gain (MAG) for each structure are shown in Fig. 1. All devices provided sufficient gain above 12 dB in the low-frequency range (10-50 GHz), but their MAG decreased as the frequency increased. The 4-finger 50 µm device exhibited the highest initial gain at low frequencies; however, its gain dropped rapidly above 110 GHz, falling below 6 dB at frequencies beyond 140 GHz. The 4-finger 25 µm device showed overall lower MAG compared to the 4-finger 50 µm device, but its gain decrease was more gradual, offering 6-8 dB in the 110-150 GHz range, though it reached its limit near 160 GHz. Meanwhile, the 2-finger 20 µm device demonstrated the lowest gain at low frequencies among the three but maintained the most stable MAG of 8-10 dB throughout the 110-160 GHz band. Notably, it still provided practically usable gain at 160 GHz, indicating that it is the most suitable structure for D-band high-frequency amplifier design in this process. Based on these results, we selected the 2-finger 20 µm device for the main amplifier design, prioritizing stable gain and high-frequency performance within the target band.

III. SINGLE-STAGE AMPLIFIER

As shown in Fig. 2(a), the single-stage amplifier adopts a simple single-stub matching network structure to achieve input and output impedance matching. The transmission lines used in the design have characteristic impedances and widths of 40 Ω (35 µm), 50 Ω (20 µm), and 63 Ω (10 µm), respectively, whereas the minimum allowable line width in this process is 5 µm. For high-frequency amplifiers, it is



(a)



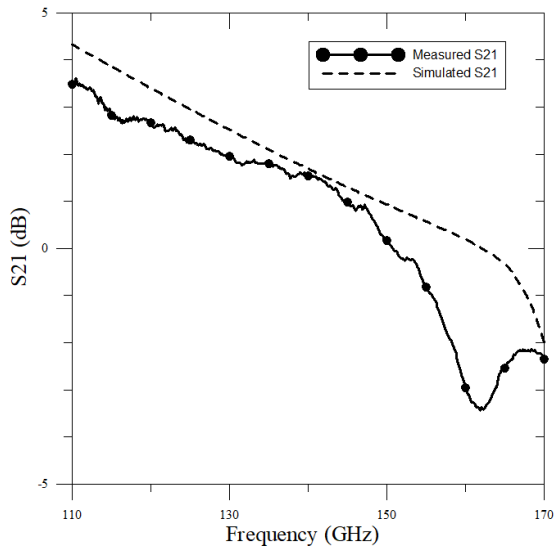
(b)

Fig. 2. (a) Schematic of the single-stage amplifier, (b) Photograph of the single-stage amplifier

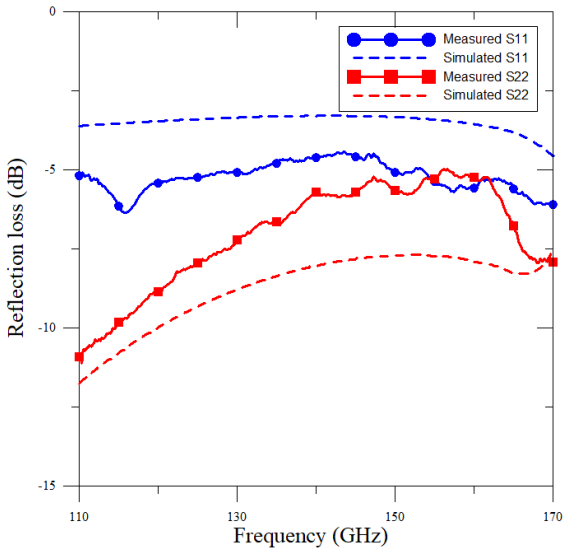
necessary to design transmission lines with various impedances to optimize input and output return loss. However, due to the minimum line width limitation, implementing high-impedance lines above 70 Ω is practically impossible. As a result, the available options are confined to the 40-63 Ω range, restricting the realization of complex impedance transformation networks.

An LC network composed of short transmission lines, a single capacitor, and an inductor provides a simple layout and ensures high reproducibility, as the difference between simulation and measurement results is minimal. Especially at high frequencies, employing a simple matching structure instead of an unnecessarily complex one is advantageous for managing losses and parasitic effects. Furthermore, because only a single metal layer is available in this process, wideband or higher-order matching networks such as λ/4 transformers, double-stubs, multi-resonators, or broadside coupling, which typically require two or more metal layers to overlap or cross lines, are not feasible. These structures are either impossible or highly inefficient due to routing conflicts, the prohibition of crossing lines, or insufficient spacing.

The limitation to a single metal layer also increases the circuit layout area and exacerbates parasitic capacitance or inductance between lines. Consequently, additional matching structures can degrade overall performance under these constraints. Therefore, considering the process restriction of a single metal layer and the limited range of available transmission line widths, the simple single-stub



(a)



(b)

Fig. 3. (a) Small-signal performance of amplifier unit cell, (b) Amplifier unit cell reflection loss (S11, S22)

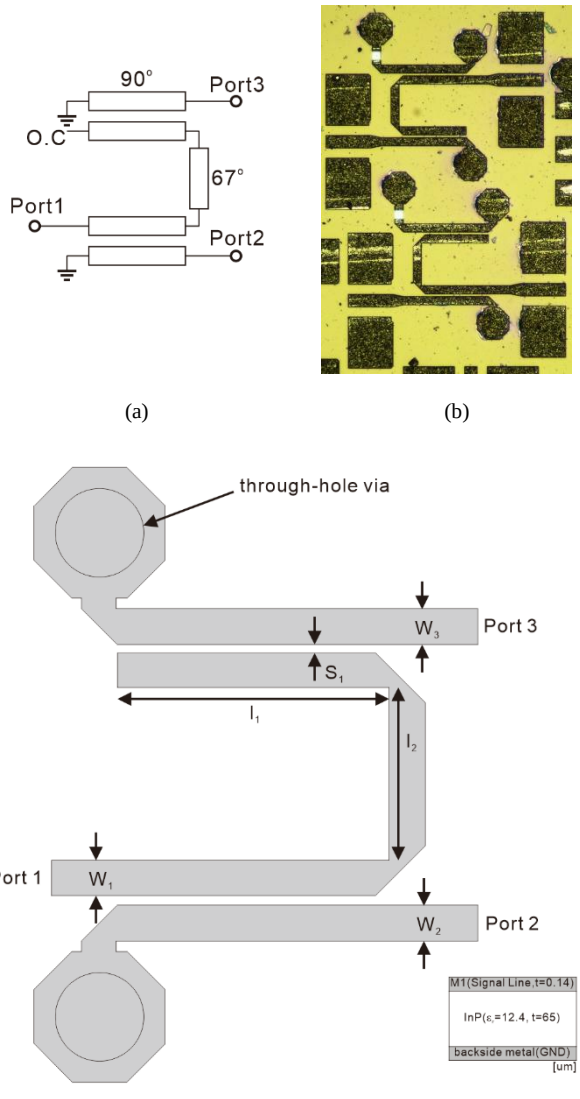
matching network is confirmed to be the most practical and performance-oriented choice. This structure offers significant advantages in terms of process compatibility, reliable repeatability, and efficient design and simulation.

The small-signal performance of the amplifier was characterized using a 67 GHz network analyzer (N5227A, Keysight) in conjunction with a D-band extension module (N5262AW06, VDI). For measurement, a D-band 2-inch waveguide was attached to interface with the measurement probe, and a FormFactor i170-S-GSG-50-BT D-band probe was employed.

Fig. 3(a) and (b) show the measured and simulated S-parameters of the designed single-stage amplifier, respectively. The measured S21, S11, and S22 all closely match the simulated values, and the amplifier achieves a gain of approximately 3 dB. The S11 performance was degraded during the simulation stage because of layout modifications required during the DRC process. Since this was our first fabrication using this process, certain parts of the circuit had to be adjusted to satisfy design rules, leading to a suboptimal layout that affected the impedance matching. This issue will be improved in future design revisions.

At frequencies above 150 GHz, the measured results were somewhat lower than the simulated values, which is attributed to unaccounted-for parasitic inductance from the via ground, in addition to additional passive losses in the fabricated circuit and minor discrepancies in the transistor parameters. The measured S11 and S22 were below −5 dB and −4 dB, respectively, which is consistent with simulation trends overall.

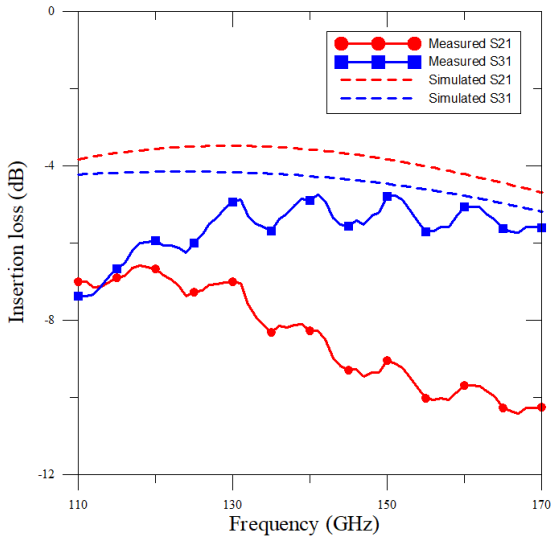
In summary, the amplifier demonstrates experimentally verified insertion gain and reflection characteristics across the 110-170 GHz band, as expected. The discrepancies between measurement and simulation are expected to be further reduced through future process parameter calibration and layout optimization.



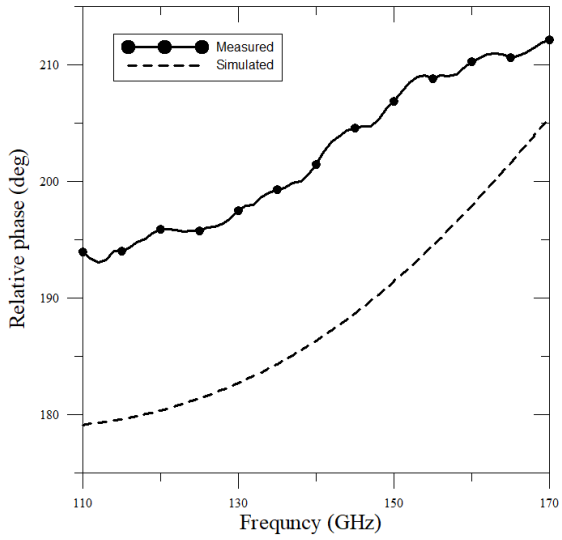
(a) (b)

(c)

Fig. 4. (a) Schematic of balun
(b) Photograph of balun (up = S31, down = S21)
(c) Layout of planar marchand balun and process cross-section
w_1=20μm, w_2=20μm, w_3=20μm, s_1=5μm, l_1=154μm, l_2=94μm



(a)



(b)

Fig. 5. (a) Balun insertion loss (b) Relative phase

IV. MARCHAND BALUN

Fig. 4(a) shows the schematic of the planar Marchand balun designed in this work. The Marchand balun converts a single input signal (Port 1) into two balanced output signals (Port 2 and Port 3) with an 180-degree phase difference. Among various balun structures, the Marchand balun [6] is considered the most suitable solution for single-layer implementation environments, as shown in Fig. 4(c), due to its ease of planar implementation and broad operational bandwidth [7]. In this design, all microstrip lines were fabricated with a width of 20 μm (w_1, w_2, w_3), the coupled line section has a gap of 5 μm (s_1) and a length of 154 μm (l_1), and the connecting lines between each coupled pair were designed to be 94 μm in length (l_2). Vias were placed near each balanced output port to connect to the ground layer. The fabricated and measured balun is shown in Fig. 4(b), where the lower and upper circuits correspond to the S21 and S31 measurement setups, respectively, while the remaining ports were terminated with 50Ω loads.

Fig. 5 presents the simulated insertion loss and phase characteristics of the Marchand balun. Fig. 5(a) shows the insertion loss, where both S21 (Thru) and S31 (Coupled) exhibit simulated insertion losses of −4 to −5 dB across the 110-170 GHz band. However, the measured results show much greater losses, with the measured insertion loss exceeding simulated values by up to 4 dB. Fig. 5(b) displays the relative phase of the balun; the simulation results maintain an approximate 190-degree difference across the band, while the fabricated device shows a slightly larger phase difference of about 200 degrees.

Although the balun operated as expected in simulation, the measured results indicate a significant increase in insertion loss and a degradation in coupling performance after fabrication. The discrepancy is presumed to be caused by the termination not providing an exact 50 Ω load during measurement, and this issue will be addressed in future design revisions.

V. DIFFERENTIAL 2-STAGE AMPLIFIER

As shown in Fig. 6, a differential two-stage amplifier structure was designed, in which the input signal is converted to differential form using a Marchand balun and then amplified by two cascaded stages. Each amplification stage consists of differential transistors (Q_1, Q_2) and matching lines, while Marchand baluns and coupled microstrip lines were incorporated between each amplification stage as well as at the input and output nodes, in order to optimize high-frequency performance. Although the amplifier has not yet been fabricated or measured, its full-band input/output return loss characteristics (S_{11}, S_{22}),

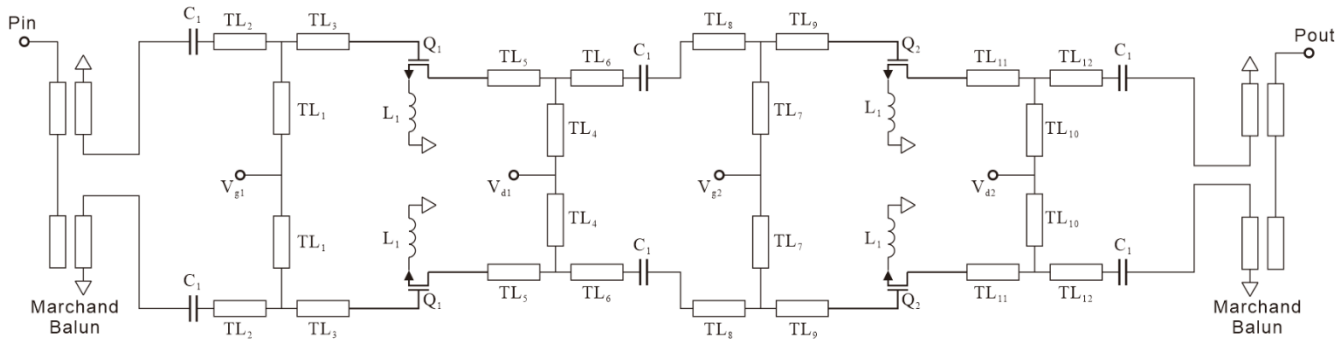
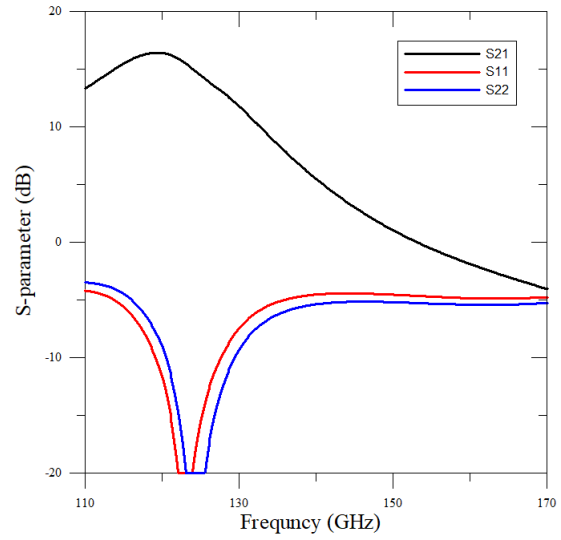
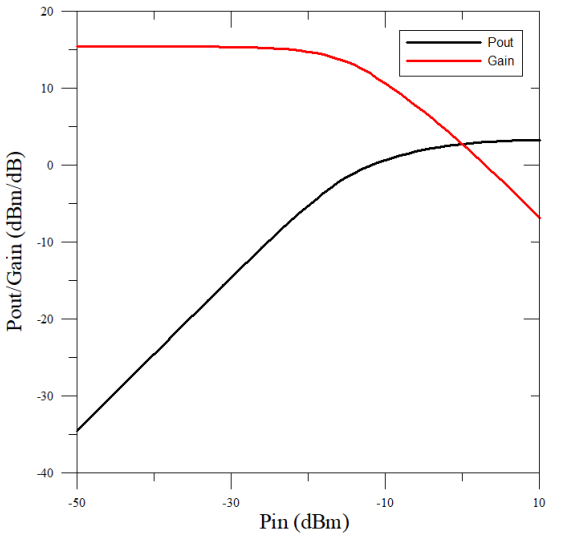


Fig. 6. Schematic of the 120-GHz amplifier



(a)



(b)

Fig. 7. (a) Simulated gain, input and output return loss performance of the amplifier
(b) Simulated output power and conversion gain versus Input power

insertion gain (S_{21}), and output characteristics (Pout, Gain) were verified through simulation.

The simulation results, as shown in Fig. 7, indicate a gain of 15.4 dB at 120 GHz, with a 3 dB bandwidth of 18 GHz. The output 1 dB compression point (OP_{1dB}) was simulated to be −3.5 dBm, indicating that the amplifier is suitable for use as a drive amplifier. The performance of this structure will be further verified through actual fabrication in future work.

VI. CONCLUSION

In this work, a single-stage amplifier, a Marchand balun, and a differential two-stage amplifier operating in the D-band were designed and analyzed using a domestically developed 100 nm InP HEMT process. The single-stage amplifier was fabricated and measured experimentally, and the results showed generally good agreement with simulation across the 110-170 GHz range. An increase in insertion loss and some performance degradation due to parameter mismatches were observed at higher frequencies; however, these issues are expected to be mitigated through further research and process optimization. The Marchand balun, implemented in a single-layer process, exhibited favorable characteristics in simulation, but the fabricated device showed significantly increased insertion loss and some deviation in phase balance. The causes of these discrepancies are under investigation, and research on improved design strategies is ongoing. Finally, although the differential two-stage amplifier has not yet been fabricated or measured, simulations demonstrated a gain of 15.4 dB and an 18 GHz bandwidth at 120 GHz, indicating its promising potential for enhanced high-frequency performance in future applications.

ACKNOWLEDGMENT

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