A Temporal Interference Stimulation Driver IC with Unified Source and Sink Current Capability

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***Abstract* – This paper presents a temporal interference stimulation driver IC (TIS-IC) for deep brain stimulation. The proposed MTIS-IC (Multi-TIS) features high linearity, independent frequency and amplitude control, and a high-voltage amplifier-based architecture. It achieves a peak-to-peak output voltage error within 0.4% and a maximum output current of 2 mA. Measured results show a maximum SFDR of 59 dB and a maximum SNDR of 46 dB. A proposed calibration method improves output signal accuracy and channel uniformity. Fabricated using a 180 nm BCD process, the proposed MTIS-IC overcomes the limitations of existing systems, enabling scalable neural stimulation and expanding biomedical applications.**

***Keywords*— temporal interference stimulation (TIS), calibration, high-voltage amplifier**

I. INTRODUCTION

The treatment of brain diseases has historically relied on drug-based therapies and surgical interventions. However, these approaches often present drawbacks in terms of therapeutic success and impose considerable burdens on patients [1]. Recently, non-invasive methods like transcranial direct current stimulation (tDCS) [2] and transcranial alternating current stimulation (tACS) [3] (Fig. 1) have garnered attention. However, their efficacy is notably compromised due to signal attenuation through the skull, restricting their capacity to stimulate deep brain structures [4].

To overcome these limitations, temporal interference stimulation (TIS), shown in Fig. 1 (bottom left), has been introduced [4], [5]. This method allows for low-frequency deep brain stimulation through the interference of two high-frequency currents. Increasing the number of stimulation channels improves targeting precision, but also requires a multi-channel platform capable of independently driving multiple electrodes [6], [7]. However, with more channels, integrated circuit (IC) and system complexity grow, impeding miniaturization essential for implantable and portable solutions [8].

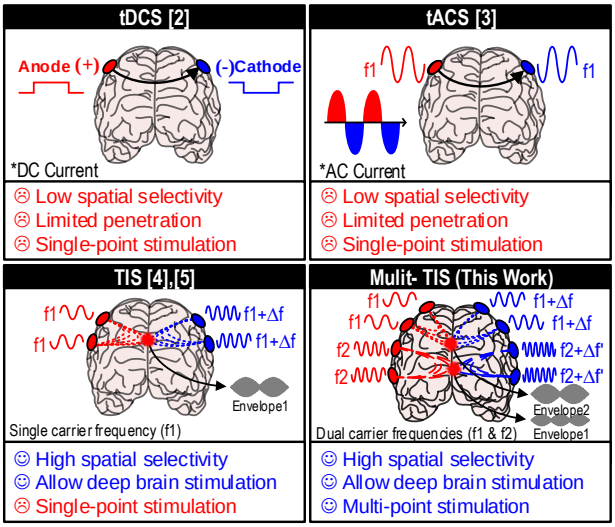

Fig. 1. Operation principles of tDCS, tACS, TIS, and MTIS.

To confront this challenge, multi-TIS (MTIS), shown in Fig. 1 (bottom right), employs multiple carrier frequencies to increase stimulation field [9], yet it currently depends on instrumentation-based systems, which are large and unsuitable for practical deployment. When two sinusoidal currents at high frequencies (f1 and f2), are applied with a slight frequency offset (Δf and Δf'), the resulting high frequency electric field does not directly depolarize neurons. Instead, the difference frequency Δf and Δf' correspond to a low-frequency envelope that falls within the neuronal response band, producing a modulation effect via temporal interference (TI). This mechanism enables targeted deep brain stimulation while minimizing unintended activation of superficial neural structures.

Conventional TIS driver circuits have been implemented at the board-level, requiring external components for each stimulation channel [10]. Such designs inevitably increase system size and weight, limiting scalability in multi-channel TIS applications. Hence, IC-level implementation of TIS driver circuits is crucial to achieve the degree of miniaturization required for implantable systems.

This work proposes a MTIS driver IC that supports scalable architecture for optimized stimulation of deep brain

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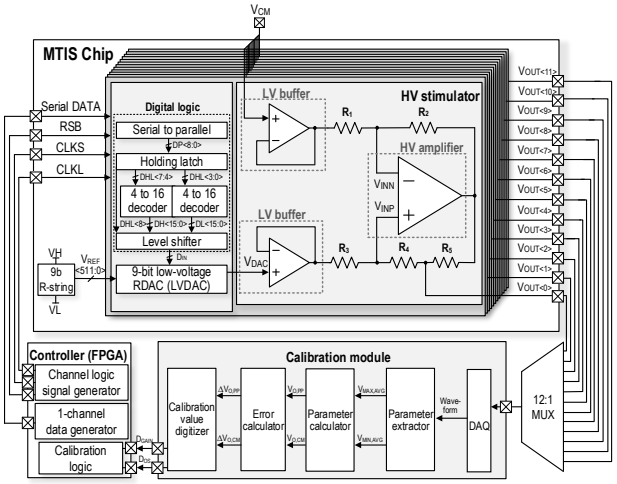

Fig. 2. Architecture of the proposed MTIS-IC and calibration system.

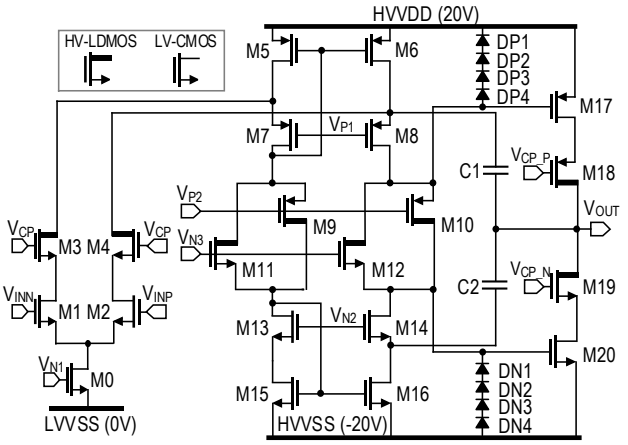

Fig. 3. Schematic of the proposed high-voltage amplifier.

and vagus nerve. It also achieves compactness, facilitating its use in a broader range of clinical applications. The remainder of this article is organized as follows. Section II presents the architecture and operation of the proposed MTIS-IC. Section III describes the measurement results. Finally, Section IV provides the conclusion.

II. PROPOSED MULTI-TIS DRIVER IC

A. Architecture of the Proposed MTIS Driver IC

Fig. 2 illustrates the architecture of the proposed multi-TIS (MTIS) driver IC and its calibration system, which consists of three main components: the MTIS-IC, an FPGA controller, and a calibration module.

The MTIS-IC is composed of three functional blocks: digital logic, digital-to-analog converter (DAC), and high-voltage (HV) stimulator. The digital logic block performs data handling and control functions. It includes a serial-to-parallel converter for data de-serialization, holding latches for timing alignment, a 4-to-16 decoder that forms the DAC input word, and level shifters that translate signal level from the 1.8 V to the 5 V. The DAC block consists of 9-bit low-voltage (LV) resistor-string DAC (LVDAC), which generates the sinusoidal drive signal that serves as the input to the HV stimulator. The HV stimulator block then converts this low-voltage input into a stimulation current. It comprises two LV buffers for input buffering, a five-resistor feedback network that defines the conversion ratio, and a core HV amplifier based on a Howland current-pump (HCP) [11] topology. This HCP-based design provides stable source-and-sink stimulation currents, and the output current is given by:

$$I_{OUT} = \frac{R_2}{R_1} \times \frac{(V_{DAC} - V_{CM})}{R_5} \quad (1)$$

It can provide a constant current even under various impedance conditions. Specifically, the MTIS-IC is designed to support ±1 mA output currents across load resistances ranging from 100 Ω to 15 kΩ.

The FPGA controller generates clock and control signals for the MTIS-IC, streams single-channel data as a 9-bit serial sequence, and embeds calibration logic that integrates correction codes from the calibration module.

The calibration module enables on-system measurement and code generation. It incorporates a 12:1 multiplexer (MUX) for channel selection and a DAQ block for waveform acquisition in the digital domain. A parameter extractor determines the maximum and minimum values of the sinusoid, and a parameter calculator derives the peak-to-peak amplitude and the common-mode level. These are compared with their target values by an error calculator, and the calibration-value digitizer produces the correction codes that are applied to the MTIS-IC. A more detailed description of the calibration is provided in the Section II-C.

B. The Proposed High-Voltage (HV) Amplifier

Fig. 3 presents the proposed HV amplifier designed for stability. The amplifier is implemented as an analog circuit and typically employs LV CMOS transistors to achieve high gain, wide bandwidth (BW), and uniformity. However, the proposed architecture requires operation over a wide high voltage range from +20 V to -20 V, which significantly limits the use of LV CMOS devices alone. To overcome this challenge, the critical components—including the input stage, cascode stage, and output driving transistors—were designed using LV CMOS, while the output stage controller part and protection circuitry were implemented with HV LDMOS.

At the input stage, the amplifier processes low-voltage signals below 4 V, for which LV CMOS transistors M1-M2 were used. To protect their drain nodes, HV LDMOS transistors M3-M4, biased at V_{CP}, were inserted to ensure that the drain voltage of M1-M2 does not exceed V_{CP}-$V_{TH,N}$, thereby guaranteeing breakdown voltage (BV) protection. Similarly, HV LDMOS transistors M9 and M10, biased at V_{P2}, and M11-M12, biased at V_{N3}, were used to protect the drain nodes of M7-M8 and M13-M14, respectively. Applying the same principle, M17 and M20 were protected

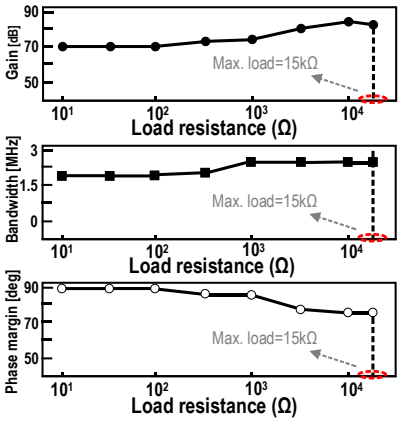

Fig. 4. AC simulation result of the proposed HV amplifier with varying load.

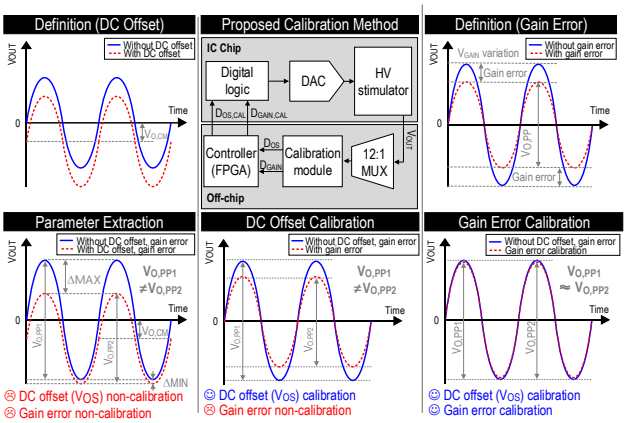

Fig. 5. Proposed calibration sequence for correcting DC offset and gain error. Red curves represent non-calibrated signals, and blue curves represent calibrated signals. (top left) definition of DC offset distortion. (top middle) overall calibration architecture (top right) definition of gain error distortion. (bottom left) parameter extraction process, where the maximum and minimum values are measured to calculate. (bottom middle) DC offset calibration aligning the common-mode level. (bottom right) gain error calibration aligning the peak-to-peak amplitude to the target value.

by HV LDMOS M18 and M19, with gates biased at V_{CP_P} and V_{CP_N} respectively. In addition, diodes were employed such that when the voltage difference between the gate and source of M17 and M20 exceeded 5 V, the diodes turned on to provide BV protection. These design strategies ensure BV protection for all devices during both large-signal slewing and small-signal operation of the HV amplifier.

To generate a sinusoidal output up to 10 kHz while maintaining loop stability, a loop bandwidth at least five times higher than the target signal frequency is required. Considering a feedback factor of 8 and an open-loop gain-bandwidth product of about 2 MHz, the resulting closed-loop bandwidth is approximately 250 kHz. The AC characteristics of the proposed HCP-based amplifier were therefore evaluated through simulation, as shown in Fig. 4. The simulations were carried out with a target output current of 1 mA, while the load resistance was swept up to 15 kΩ.

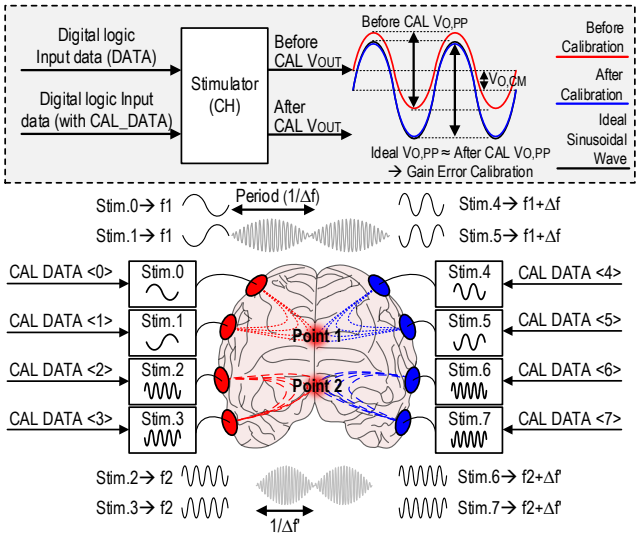

Fig. 6. Post-calibration multi-channel stimulation with uniform sinusoidal outputs. (top) concept of calibration effect: red curves indicate non-calibrated signals with offset and gain error, while blue curves indicate calibrated signals. (bottom) block diagram of the MTIS-IC driving multiple stimulation channels after calibration. Each channel generates an independent sinusoidal waveform with programmable frequency and amplitude, enabling precise multi-channel temporal interference patterns at target points in the brain (Point 1 and Point 2).

As shown in the top plot of Fig. 4, the amplifier maintains a high open-loop gain exceeding 70 dB across the entire load range. The middle plot demonstrates that the bandwidth remains larger than 1.7 MHz under all load conditions, and reaches a maximum of 2.2 MHz. The bottom plot shows that the phase margin consistently stays above 74°, ensuring loop stability. These results confirm that the proposed HV amplifier achieves a minimum gain of 70 dB, a minimum bandwidth of 1.7 MHz, and a minimum phase margin of 74° under varying load conditions, thereby enabling accurate sinusoidal output currents up to 10 kHz.

C. Calibration System

In the proposed MTIS system, calibration is indispensable because process variations introduce errors in the output signals, thereby degrading stimulation fidelity at the target region. As illustrated in Fig. 2, the HV stimulator consists of two LV buffers, resistors R_1-R_5, and an HV amplifier. When process variations occur, the LV buffers exhibit random offset voltages, which shift the DC levels of V_{DAC} and V_{CM} in equation (1). This shift directly produces a DC offset in I_{OUT}. Similarly, resistor mismatch alters the ratio between R_1 and R_2, leading to the gain error in I_{OUT}. These errors distort the output sinusoidal waveform and reduce spatial accuracy at the stimulation target, making calibration essential to prevent per-channel output distortion.

Representative examples of distortion are shown in Fig. 5. A shift in the common-mode level of the output sinusoidal current produces a DC offset (top-left), while a change in amplitude results in a gain error (top-right). In practice, both DC offset and gain error can occur simultaneously, further

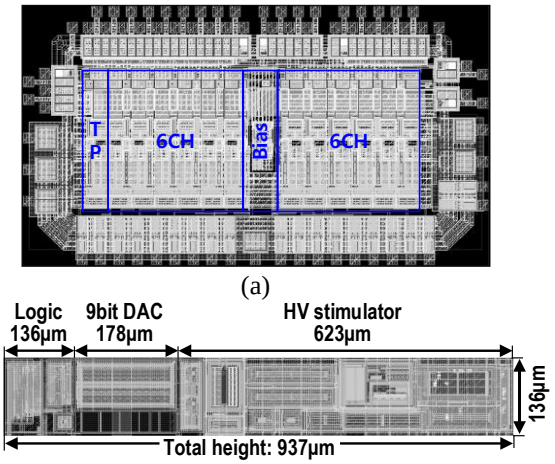

Fig. 7. Layout of the proposed MTIS-IC (a) top circuit (b) single channel circuit.

impairing the accuracy of target-region control. Therefore, the proposed MTIS-IC system incorporates a calibration procedure to eliminate these distortions and ensure precise stimulation.

The proposed calibration architecture is shown in Fig. 5 (top center). It is implemented off-chip and consists of a 12:1 MUX, a calibration system, and an FPGA controller. The MUX selects one of the twelve IC channels and routes its output to the calibration system. The calibration system computes digital correction codes to compensate for both gain error and DC offset, and these codes are written into FPGA registers. The FPGA then programs the IC with the correction codes, enabling the IC to output calibrated sinusoidal current signals.

The detailed operation of calibration is illustrated in Fig. 5 (bottom). The error-affected waveform (red) includes both gain error and DC offset compared with the target sinusoidal signal (blue). In Fig. 5 (bottom-left), $V_{O,PP1}$ represents the target peak-to-peak amplitude, while $V_{O,PP2}$ denotes the measured peak-to-peak amplitude; their difference reflects the gain error. The simultaneous presence of gain and DC offset errors also leads to differences between the maxima and minima of the two waveforms, denoted as ΔMAX and ΔMIN. The calibration begins by extracting the maximum and minimum of the error-affected waveform, from which the DC offset is computed and removed (Fig. 5, bottom-center). Ast this stage, the gain error still remains. Finally, he amplitude is corrected so that $V_{O,PP1}$ and $V_{O,PP2}$ become equal. The resulting waveform, free of both DC offset and gain error, is shown in Fig. 5 (bottom-right). This calibration method can be fully automated.

As illustrated in Fig. 6, once offset and gain errors are compensated, the MTIS-IC generates sinusoidal current signals with adjustable amplitude and frequency, enabling multiple stimulation patterns and precise targeting of the stimulation target region.

III. MEASUREMENT RESULT

Fig. 7 shows the layout of the proposed MTIS-IC: (a) the die micrograph of the chip fabricated in a 180-nm BCD process, where the 12-channel design includes an on-chip test pattern (TP) to verify each functional block; (b) the single-channel layout with an area of approximately 0.13 mm², consisting of about 15% digital, 19% DAC, and 66% HV stimulator.

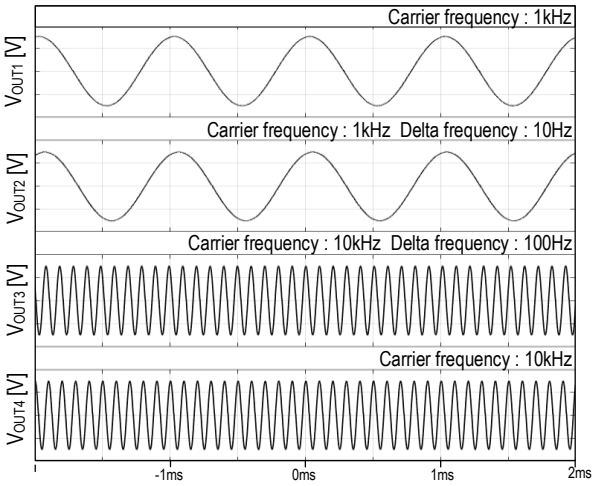

Fig. 8. Measured waveforms: V_{OUT1}(1kHz), V_{OUT2} (1.01kHz), V_{OUT3}(9.9kHz), and V_{OUT4}(10kHz).

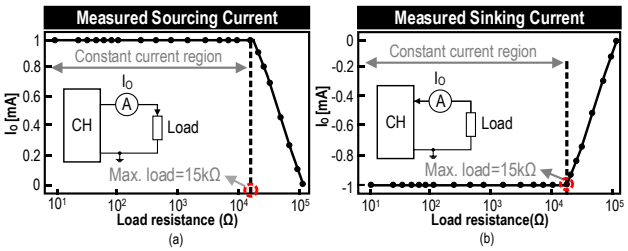

Fig. 9. Measurement of load variation while maintaining constant output current: (a) sourcing; (b) sinking current.

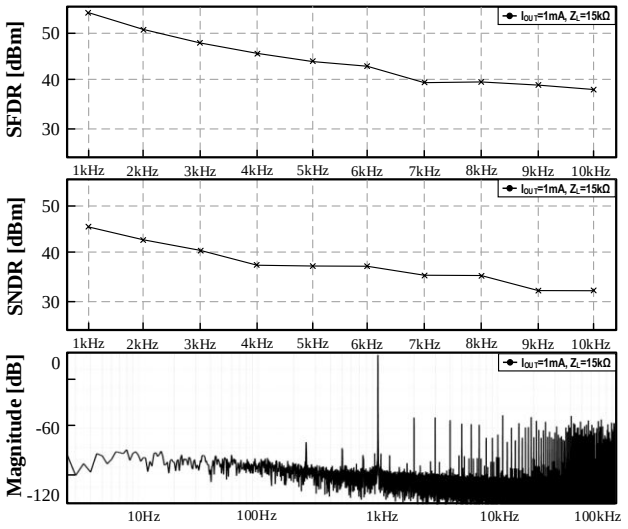

Fig. 10. Measured dynamic performances.

Fig. 8 shows the output voltage waveforms. Each sine wave is configured with an amplitude ranging from -1 mA to 1 mA, and the measurement was conducted under a 15 kΩ load condition. Specifically, V_{OUT1} and V_{OUT2} operate to 1.0 Hz and 1.01 kHz, while V_{OUT3} and V_{OUT4} are set to 9.9 kHz

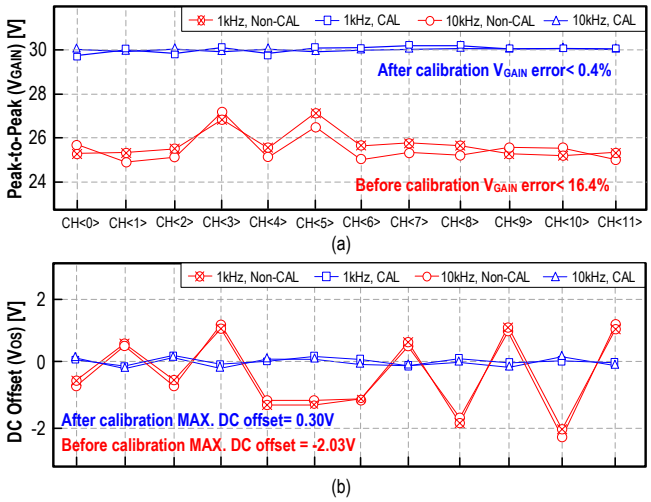

Fig. 11. Effect of calibration on inter-channel uniformity across 12 channels. Red curves show non-calibrated results, while blue curves show post-calibration results. (a) Gain error reduced from 16.4% to <0.4%. (b) DC offset reduced from 2.03 V to 0.30 V.

and 10.0 kHz, respectively. The measurement results demonstrate that an output current frequency resolution of 10 Hz was achieved.

Fig. 9 presents the measured load-sweep results that validate current regulation. The MTIS-IC was configured to deliver target output currents of +1 mA (left) and -1 mA (right) while the load resistance was varied from 10 Ω to 100 kΩ. In both sourcing and sinking modes, the driver maintained stable current delivery up to 15 kΩ, confirming robust regulation under varying load conditions.

Fig. 10 presents the dynamic performance of the proposed MTIS-IC in terms of SNDR and SFDR over the frequency range of 1 kHz to 10 kHz, measured under a load condition of 15 kΩ at a target output current of 1 mA. The maximum SNDR and SFDR are measured at 1.0 kHz, reaching 49 dB and 59 dB, respectively.

Fig. 11 illustrates the effect of calibration on inter-channel uniformity across 12 channels. Fig. 11 (a) shows the gain error before and after calibration at 1 kHz and 10 kHz. Without calibration, the gain error in reached a maximum peak-to-peak value of 16.4%. After calibration, the gain error was significantly reduced to less than 0.4%, demonstrating a substantial improvement in inter-channel amplitude matching. Fig. 11(b) presents the corresponding DC offset (V_{OS}). Prior to calibration, the maximum DC offset was 2.03 V. After calibration, this value was reduced to 0.3 V, confirming effective suppression of offset variation across channels. These results verify that the proposed calibration scheme substantially improves channel-to-channel uniformity, thereby enhancing the accuracy of multi-channel stimulation.

A comparative summary of performance with previously reported works is presented in Table I. The architecture introduced a current mirror structure to generate stimulation currents [12]. While this approach offers simplicity in circuit implementation, it is inherently susceptible to process, voltage, and temperature (PVT) variations. These variations

TABLE 1. Performance Comparison.

	[12] CICC24	[13] ISSCC23	This work
Technology	130nm BCD	65nm	180nm BCD
Application	PNS	PNS	VNS, Brain stim.
Stimulation method	Single-TIS	Single-TIS	Multi-TIS
Stimulation waveform	Sinusoidal	Sinusoidal	Sinusoidal
No. channels/ Stimulators	16/4	64/64	12/12
Compliance voltage [V]	10	3.3	20/-20
Max. Output current [mA]	10	2	1
Output current resolution [μA]	N/A	N/A	7.8
Channel area [mm²]	0.13 (without DAC)	N/A	0.13 (with DAC)
Output signal Max. frequency [Hz]	42k	>2k	10k
Output signal frequency resolution [Hz]	N/A	N/A	10
DAC type	Current	8b	Voltage
DAC resolution	9b	8b	9b
With calibration	Yes	N/A	Yes
Max. SFDR [dB]	57	N/A	59
Max. SNDR [dB]	N/A	N/A	45
Maximum load [Ω]	1.8k	N/A	15k

lead to threshold voltage (V_{TH}) mismatches in transistors, directly impacting current matching accuracy and degrading linearity particularly near the zero-crossing points of the sinusoidal output. Furthermore, generating both sourcing and sinking currents requires polarity-switching operations, which may introduce switching noise and potentially degrade the signal-to-noise-and-distortion ratio (SNDR). In a separate line of research, the prior work employs a current-steering digital-to-analog converter (I-DAC) to generate stimulation current [13]. This architecture similarly necessitates switching between sourcing and sinking phases, which can result in transient glitches and further degrade SNDR.

IV. CONCLUSION

In this work, we presented a high-performance multi-TIS temporal interference stimulation driver IC (MTIS-IC) designed for deep brain stimulation. The proposed architecture, based on a high-voltage amplifier, supports independent control of both frequency and amplitude, enabling precise and scalable multi-channel neural stimulation. Measurement results validate the circuit's effectiveness, achieving a peak-to-peak output voltage error of less than 0.4%, a maximum output current of 1 mA, an SFDR of 59 dB, and an SNDR of 46 dB.

Fabricated using a 180 nm BCD process, the MTIS-IC overcomes the limitations of prior implementations in terms of linearity, miniaturization, and signal fidelity. The architecture proposed in this work generates stimulation currents in the form of a unified sine waveform, thereby eliminating the need for polarity switching between sourcing and sinking phases. This inherently suppresses switching-induced noise and enables superior performance in terms of SNDR.

In addition, the system incorporates a dedicated DAC for each stimulation channel, allowing for independent control of individual electrodes and minimizing inter-channel mismatch. Furthermore, the proposed design achieves a reduced area per channel including the DAC compared to prior works.

The proposed system enables precise sinusoidal current-mode stimulation with enhanced linearity and integrates a mismatch calibration technique to improve output accuracy and channel-to-channel uniformity. Its ability to drive multiple channels with high accuracy makes it a promising solution for next-generation non-invasive stimulation systems.

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