A Small-Size High-Power Single-Pole Four-Throw Switch with a Reconfigurable Matching Inductor

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***Abstract* – A single-pole four-throw (SP4T) high-power switch is presented, which consists of four series transistors (STs) and a reconfigurable matching inductor (RMI). The single inductor is reconfigured through the inductor connection transistors (ICTs) to resonate out the off-capacitance (C_{OFF}) of all off-state transistors. The RMI provides low insertion loss and high isolation simultaneously regardless of the gate width of STs, which allows compact implementation. The switch was fabricated using a 130-nm SOI CMOS process. Measurement results show an insertion loss of 0.7 dB, an isolation of 28.1 dB, and an IP_{1dB} of higher than 27.4 dBm at 3.5 GHz.**

***Keywords*—RF switch, single-pole four-throw (SP4T) switch, high-power switch, reconfigurable matching inductor (RMI)**

I. INTRODUCTION

Sub-6 GHz 5G communication is being widely commercialized and developed in many countries. Both 4G Long-Term Evolution (LTE) communication and 5G New Radio (NR) systems operate in this frequency range, leading to strong demand for sub-6 GHz RF circuits [1]. Among them, the RF switch is an essential component of an RF transceiver, with key parameters including insertion loss, isolation, linearity, and size. It significantly affects the noise figure and the linearity of the transceiver, and needs a high power-handling capability to handle the output power of a power amplifier.

Achieving low insertion loss and high isolation simultaneously is a challenge in previously reported multi-stacked high-power switches [2], [3]. These switches show great performance at low frequency region by using large gate width transistors with small on-resistance R_{ON}. However, their performance degrades significantly at higher frequencies due to large off-capacitance (C_{OFF}), which causes severe leakage into unwanted ports. Furthermore, the inherent trade-off between insertion loss and isolation prevents them from achieving optimal performance. These problems can be mitigated by implementing matching inductors at each port [4], [5], but they are not suitable for sub-6 GHz switches because the required inductance is too large. Other approaches such as a frequency-reconfigurable switch with mode selection function [6], and a dual-band switch have been proposed for broadband operation [7], but they have limited power-handling capability.

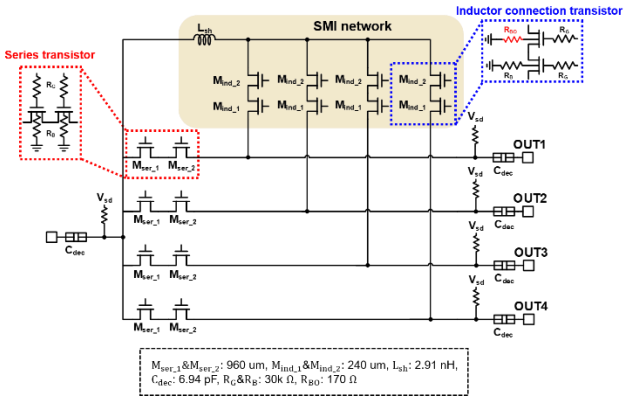

Fig. 1. Schematic of the proposed SP4T switch.

In this paper, we propose a compact single-pole four-throw (SP4T) high-power switch that uses a reconfigurable matching inductor (RMI). The RMI resonates out the C_{OFF} with a single inductor, enabling low insertion loss and high isolation at the target frequency. The resonance frequency can be adjusted by varying the inductance of the RMI, so the switch can be designed regardless of the target frequency. Moreover, the body resistors of the RMI are optimized for high power-handling capability.

II. CIRCUIT DESIGN

A schematic of the proposed SP4T switch is shown in Fig. 1. It consists of four paralleled series transistors (STs) that connect the input to one of the four outputs, and an RMI. The RMI is composed of four inductor connection transistors (ICTs) and an inductor (L_{sh}) shared by them. ICTs connect L_{sh} to the outputs unconnected to the input. For example, in order to route the input signal to output 1, ST of the output 1 path is turned on and the STs along all other paths are turned off. Conversely, ICT of output 1 path is turned off and the ICTs along all other paths are turned on. To enhance the linearity and reduce the C_{OFF}, a source-drain voltage (V_{sd}) is

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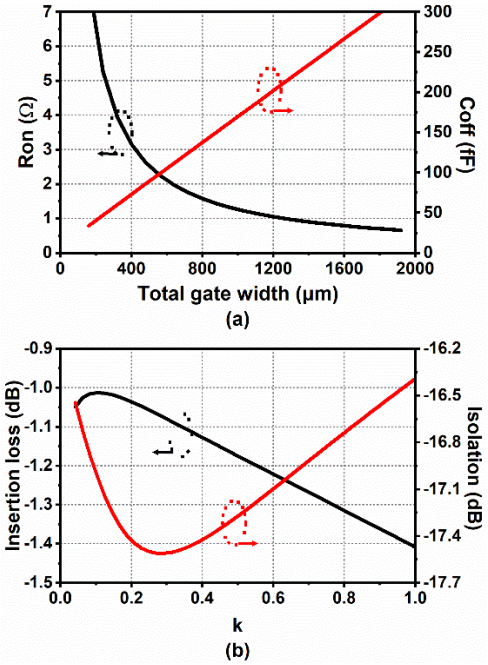


Fig. 2. Transistor size optimization (a) ST, and (b) ICT.

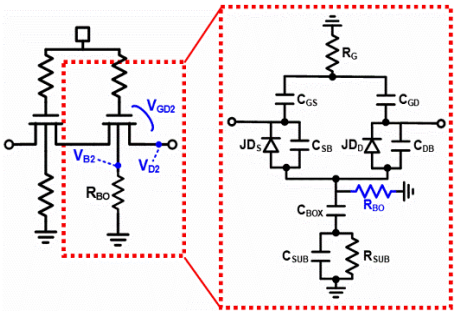


Fig. 3. Equivalent circuit of a 2-stacked transistor.

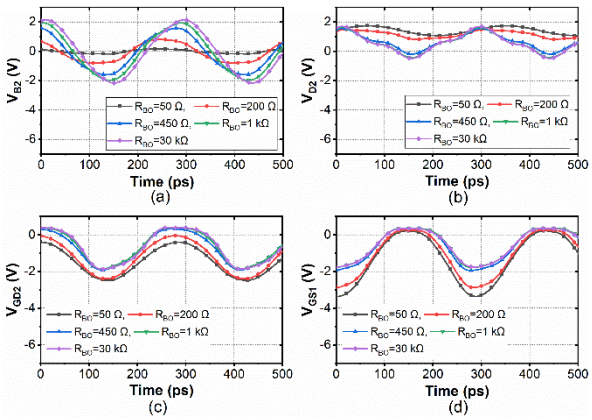


Fig. 4. Simulated voltage swings with respect to R_{BO}: (a) V_{B2}, (b) V_{D2}, (c) V_{GD2}, and (d) V_{GS1}.

applied [8]. Considering the breakdown voltage, V_{sd} is set between 0 V and 2.5 V. On-chip 6.94 pF decoupling capacitors (C_{dec}) are implemented in each port to isolate input and output ports from the switch core.

Transistor size optimization is shown in Fig. 2. The gate width of ST is set to 960-μm, resulting in a sufficiently small R_{ON} of 1.3-Ω, with a C_{OFF} of 163 fF. The simulated insertion

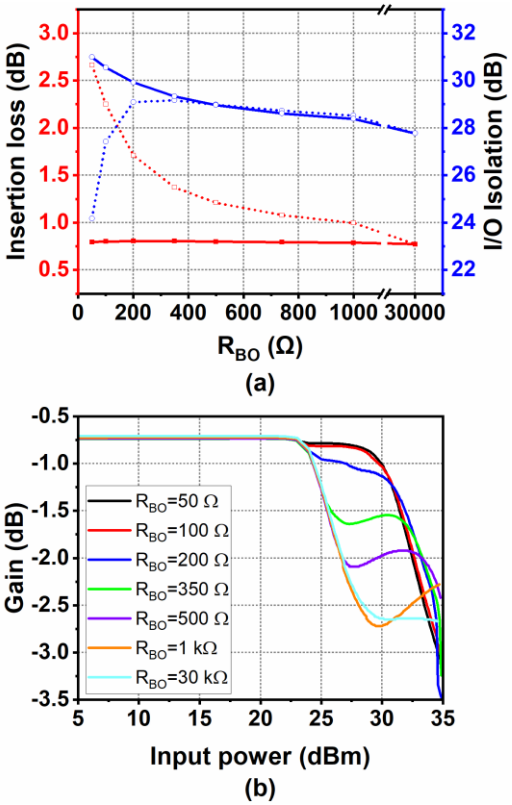


Fig. 5. (a) Simulated insertion loss and I/O isolation with respect to R_{BO} at ST (dotted) and ICT (solid), (b) IP_{1dB} with respect to R_{BO} at ICT.

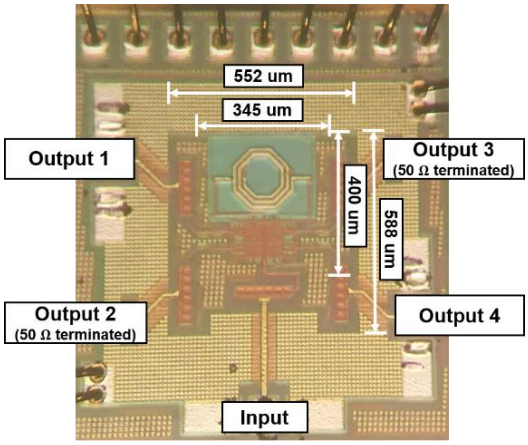


Fig. 6. Photograph of the proposed SP4T switch.

loss and input-to-output isolation (I/O ISO) with respect to k are shown in Fig. 2(b), where k is defined as the gate width ratio of ST and ICT. As the gate width of ICT increases, the quality factor of the RMI increases and the insertion loss of the switch decreases. However, above a certain value of k, the insertion loss increases as the resonance frequency of the isolation network deviates from the operating frequency of the switch. The optimized k value is 0.25, which results in a size of 240-μm for ICT. The RMI should resonate out the C_{OFF} of three STs and one ICT at the desired frequency. Therefore, the value that L_{sh} should have is defined as

$$L_{sh} = \frac{1}{(2\pi f_0)^2 \times C_{OFF,ST} \times (3+k)}. \quad (1)$$

where f_0 is the target frequency of the SP4T switch.

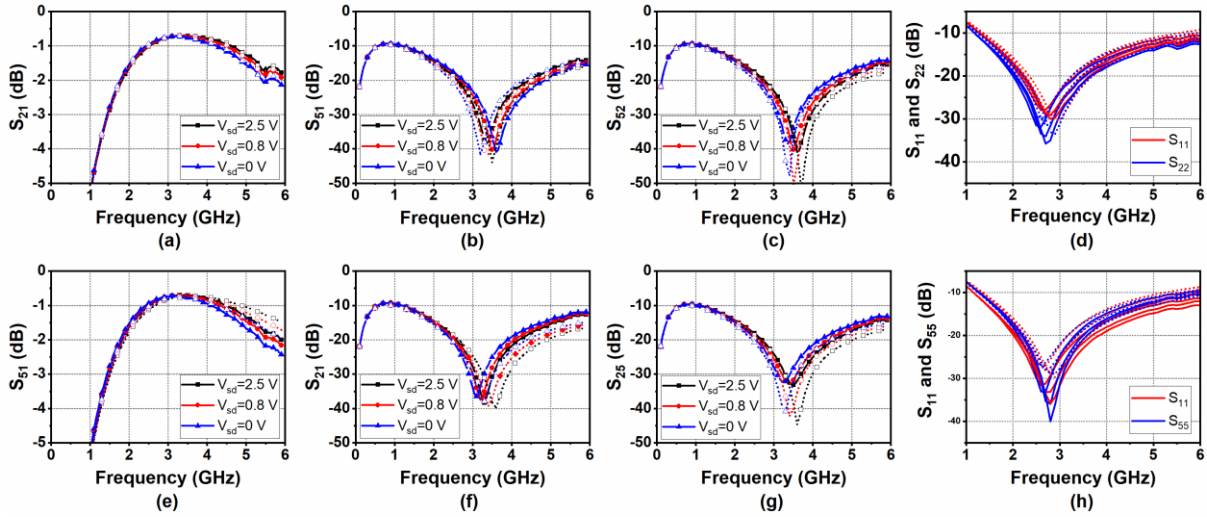


Fig. 7. Measurement (solid) and simulation (dotted) results when Output 1 path is on (a) insertion loss, (b) I/O ISO, (c) O/O ISO, (d) return loss, and when Output 4 path is on (e) insertion loss, (f) I/O ISO, (g) O/O ISO, (h) return loss.

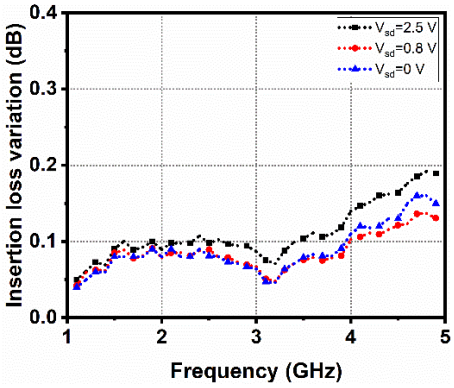
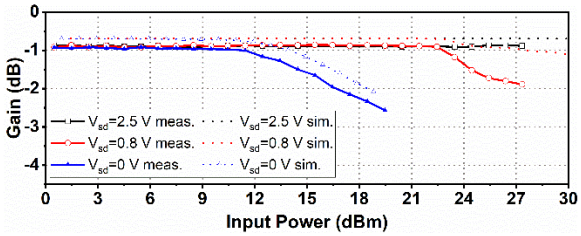


Fig. 6. Insertion loss deviations with respect to V_{sd}.



Unlike conventional switches, the proposed switch can achieve high isolation and small insertion loss simultaneously, since the RMI can resonate C_{OFF} regardless of f_0 and gate width of ST.

As the number of transistor stacks increases, the power handling capability of the switch also increases [9]. However, to maintain same R_{ON}, the gate width of each transistor must also increase proportionally, resulting in a larger circuit area. In practice, transistors with large gate-width have significant parasitic components, which degrades insertion losses and limit the expected improvement in power-handling capability [10]. Therefore, an alternative technique is required to overcome these limitations.

A body-floating technique is a well-known technique for reducing C_{OFF} and enhancing the power-handling capability of the switches [11]. The equivalent circuit of a 2-stack transistor, including parasitic components, is shown in Fig. 3. The transistor body is connected to the source and drain with junction diodes. When the body resistance (R_{BO}) decreases, the peak-to-peak value of the body voltage of the second transistor (V_{B2}) becomes close to 0 V, as shown in Fig. 4(a). Junction diodes prevent the drain voltage of the second transistor (V_{D2}) from falling below V_{B2}, that is, 0V as shown in Fig. 4(b). As a result, the peak of V_{GD2} is reduced as shown in Fig. 4(c), thereby preventing unwanted channel formation. However, as R_{BO} decreases, the peak-to-peak value of V_{GS1} increases as shown in Fig. 4(d), causing a reliability problem [12]. Moreover, this technique can only be applied to the second transistor of ICT or ST, as applying it to the first transistor may induce signal distortion [3].

Fig. 5(a) shows the simulated insertion loss and I/O ISO with respect to the R_{BO} for the ST and ICT. The switch performance is more sensitive to R_{BO} in the ST as the total gate width of off-state ST is very large compared to ICT, causing dramatic C_{OFF} variation. Therefore, we applied body-resistor-optimization to the second transistor of ICT. Fig. 5(b) shows the gain of the switch with respect to the input power for various R_{BO}s. R_{BO} was selected as 200-Ω, as it shows a notable improvement in input power 1-dB compression point (IP_{1dB}) without degrading other performances.

III. IMPLEMENTATION AND MEASUREMENT RESULTS

Fig. 6 shows a photograph of the proposed SP4T switch. It was fabricated with a 0.13-μm SOI CMOS process. The gates of all transistors and the bodies of all transistors except for the second transistor in each ICT are floated with 30-kΩ resistors. The core area of the switch is 0.138 mm^2 without C_{dec} and 0.325 mm^2 with them. The inductor of the RMI has inductance of 2.91 nH with a quality factor of 11.7, which was chosen to resonate out C_{OFF} at the target frequency of 3.5 GHz. To improve the quality factor of the matching network, all transistors are placed outside the inductor. In order to minimize the insertion loss variations of the four outputs, the signal lines from switch core to each output are

TABLE I. Performance Summary and Comparison with Other SPnT Switches.

	This work	[3]	[6]	[7]
Process	0.13-μm SOI CMOS	0.18-μm CMOS	28-nm SOI CMOS	0.15-μm GaAs pHEMT
Topology	Series, RMI	Series-shunt (RX) Series (TX)	Series, Reconfigurable SI	Series, BTC
Number of throws	4	4	4	2
Frequency (GHz)	2.2-4.9	0.5-2.5	DC-4.4/4.4-5.3	2-3/4.4-5.3
Insertion loss (dB)	<1.4 0.7 at 3.5 GHz	<2.4*	<2/<2	<2/<2.1
Isolation (dB)	>15.8 28.1 at 3.5 GHz	>16*	>16.8/>18	>35/>28
Return loss (dB)	>11.8	>12*	-	>20
IP_{1dB} (dBm)	>27.4 at 3.5 GHz	31.5 at 1.9 GHz	>7	14.5 at 2.45/5.8 GHz
Core area (mm^2)	0.325 (0.138 w/o C_{dec}s)	0.54#	0.2	2.43

*Graphically estimated, #Area with pads

designed to be nearly identical. Output 2 and 3 were terminated with on-chip 50-Ω resistors. As all the transistors are operated in passive mode, it does not consume DC power.

The measured and simulated S-parameters for V_{sd} of 0 V, 0.8 V, and 2.5 V are shown in Fig. 7. All measurements were conducted with single-ended 50-Ω GSG probes with SOLT calibration. At 3.5 GHz, the proposed switch achieves an insertion loss of 0.7 dB including the losses of RF pads and C_{dec}s, an I/O ISO of 28.1 dB, and an output-to-output isolation (O/O ISO) of 31.7 dB. From 2.2 to 4.9 GHz, it shows lower than 1.4 dB insertion loss, higher than 15.8 dB isolations, and higher than 11.8 dB return loss at 2.2-4.9 GHz.

The deviations between two outputs are shown in Fig. 8. For all V_{sd} the deviation is less than 0.19 dB at the operating frequency.

Fig. 9 shows the measured and simulated IP_{1dB} of the switch. When 0.8 V V_{sd} was applied, the measured IP_{1dB} was 27.4 dBm, which was the highest input power applicable in the measurement setting used here. According to the simulation, it is expected that the IP_{1dB} will be beyond 27.4 dBm when V_{sd} increases to 2.5 V. The discrepancy between the measurement and simulation is attributed to modeling uncertainty in thick-oxide devices and process variation.

Table I summarizes the switch performance summary and compares it with other reported single-pole n-throw (SPnT) switches. Unlike other designs, the proposed switch is optimized at the target frequency, achieving a high IP_{1dB} with the lowest insertion loss at 3.5 GHz. Also, it has comparable other performances.

IV. CONCLUSION

This paper presents a 3.5 GHz high-power SP4T switch with RMI. The proposed design achieves low insertion loss and high isolation simultaneously by resonating out the C_{OFF} with a single inductor. Furthermore, optimized body resistors enhance power-handling capability without increasing the number of transistor stacks. Measurement results confirm that the proposed switch is suitable for high-power transceivers.

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