A 4x Time Interleaved SAR ADC with Common-Mode Injecting Skew-Detection Method

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Abstract - **This paper proposes a 4-channel time-interleaved successive approximation register analog to digital converter (TI-SAR ADC). The proposed TI-SAR ADC adopts a common-mode injection technique to achieve efficient skew detection. In addition, by employing a switched-capacitor integrator operating at a lower speed than the ADC sampling rate, low-power, background skew detection is realized. The proposed ADC achieves an SNDR of 61.3 dB at a sampling rate of 800 MS/s, while consuming 5.58mW of power and achieving a FoM_w of 7.73 fJ/conv-step.**

***Keywords*— Analog-to-digital converter (ADC), time-interleaving, skew-detection**

I. INTRODUCTION

With the development of next-generation wireless communication standards such as WiFi-7, there is a rapidly growing demand for high-performance analog-to-digital converters (ADCs) capable of achieving resolutions of 10 bits or higher, sampling rates in the GHz range and power efficiency especially for mobile applications.

Among the ADC architectures commonly employed in these resolutions are pipeline ADCs and successive approximation register (SAR) ADCs. Pipeline ADCs are widely adopted in scenarios demanding both high speed and high resolution, as their multi-stage structure enables high sampling rates by distributing the conversion process across several stages. Each stage performs a partial conversion and passes the residue to the next stage, thereby maximizing overall throughput. However, the need for residue amplifiers in each stage results in increased overall power consumption, which is a significant design constraint, particularly in mobile and low-power systems. In contrast, SAR ADCs feature simple architecture primarily based on digital circuits, enabling high energy efficiency and integration density. The binary search algorithm used in SAR ADCs allows for sequential conversion with low circuit complexity and reduced power consumption. However, as the resolution increases, the number of clock cycles required for conversion also rises, imposing a limitation on conversion speed. Furthermore, higher resolution demands stricter comparator noise performance, which degrades both speed and power efficiency. To overcome this limitation, TI-SAR ADC architecture has been proposed [1]-[3], in which multiple SAR ADC channels operate in parallel to increase the effective sampling rate by a factor of N, where N is the number of channels. While this approach offers a significant speed advantage, it introduces channel mismatches such as offset, gain, and timing mismatches that can degrade the overall resolution. Therefore, various calibration techniques are essential to mitigate these mismatches and ensure accurate conversion.

In particular, for TI-SAR ADCs to operate with both high speed and high resolution, precise skew detection is required to correct timing errors that increase proportionally with input frequency. Various skew detection methods utilizing a reference clock have been proposed [4]-[5]. [4] has the advantage of eliminating residual skew by injecting the reference clock into the input path, but it can only operate with foreground detection [4]. Although [5] operates with background detection, a separate reference clock insertion path causes residual skew. Additionally, dithering techniques have been explored, but these typically require input buffers, making them unsuitable for high-resolution ADCs [6].

In this work, we propose a novel skew detection method that detects skew by monitoring variations in the input common mode through common-mode injection. By employing an AC-coupled input network, the proposed method enables common-mode injection without the need for input buffers. Furthermore, an integrator is used to accumulate the results of multiple samples, allowing for simple and effective skew detection without increasing circuit complexity.

The remainder of this paper is organized as follows. Section II describes the proposed ADC architecture and detection methodology in detail. Section III presents simulation results to validate the performance of the proposed technique. Finally, Section IV concludes the paper.

II. DESIGN METHODOLOGY

A. Proposed ADC architecture

Fig. 1 illustrates the architecture of the proposed ADC. This architecture comprises a core time-interleaved (TI)

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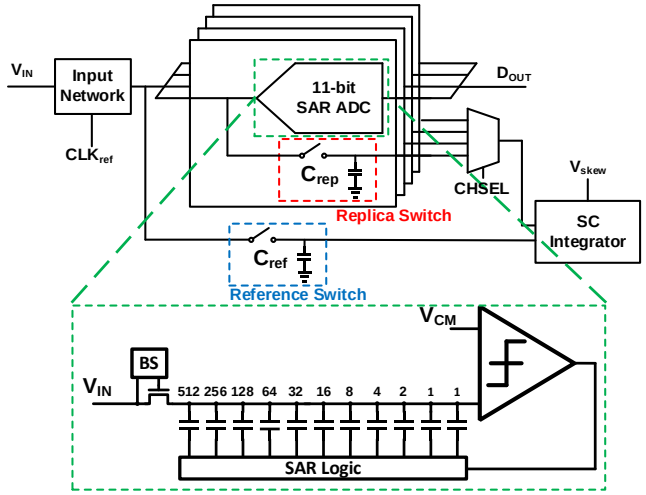

Fig. 1. Proposed ADC architecture

ADC, along with several auxiliary circuits designed to support background on-chip detection.

The ADC core is implemented as a 4-channel TI-SAR structure, with each channel designed as a CDAC-based SAR ADC to operate at 11-bit resolution and a 200 MHz sampling rate, enabling both high speed and high resolution.

To support the detection of this core, an input network is incorporated. This network receives reference clock (CLK_{REF}) and injects it into the common mode of the input signal, a critical step for facilitating common-mode detection. Following this, replica and reference switches are employed to sample the injected common mode voltage. These switches utilize sampling capacitors that are only 1/10 the size of those found in a single-channel CDAC. A multiplexer (MUX) is also integrated in this stage, enabling independent detection procedures for each of the ADC channels. Finally, a switched-capacitor (SC) based integrator is included to accumulate the sampled common-mode signals. This accumulation process serves to improve the overall accuracy of detection.

B. Input network

Fig. 2 illustrates the structure of the input network. The input network consists of an RC circuit and an inverter chain that drives the reference clock. The R_{CP} at the input terminal is a 50Ω off-chip resistor originating from the signal source equipment, while the remaining components are implemented on-chip. The input signal is AC-coupled through the C_{CP} capacitor, which removes the common-mode component.

The common mode of the input signal is generated by the RC circuit located at the center of the input network. The V_{Bias}, which serves as the common-mode voltage for the input signal, is connected across the R_{CM} resistors, and CLK_{REF} is applied between the C_{CP} capacitors. As a result, $VIN_{CP,CM}$, representing the common mode of the AC-coupled input signal, is generated. This signal then varies around the V_{CM} level, reflecting the influence of the injected reference clock.

As depicted in Fig. 3, $VIN_{CP,CM}$ vary in synchronization with the SH signal. When the SH signal timing is consistently identical (i.e., no skew), the same common

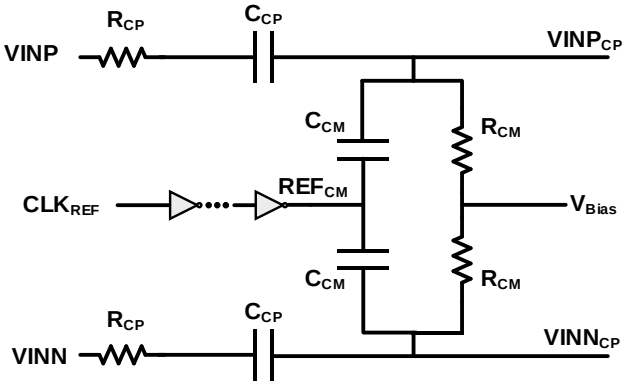

Fig. 2. Input network

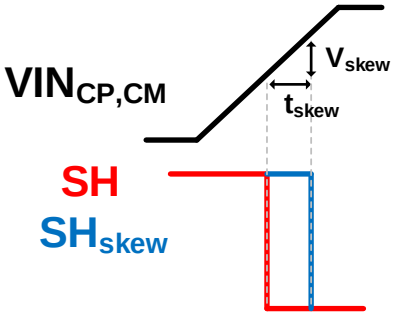

Fig. 3. Skew error visualization

mode voltage is sampled. However, if skew occurs, a difference arises in the sampled common mode voltage. This difference in common mode voltage can then be used to measure the magnitude of the skew in voltage domain.

C. Skew detection

Fig. 4 illustrates the operation timing diagram of the proposed ADC. The 800 MHz CLK_{main} signal is divided into four 200 MHz sampling clocks, $\Phi_{SH<1>}$ to $\Phi_{SH<4>}$, which are supplied to each channel. Skew detection is performed independently for each channel, and Fig. 4 presents an example in which channel 1 is being calibrated. For stable operation and low power consumption of the ADC, the common-mode injection operates at a rate 256 times slower than the ADC operation period. Φ_{CLK_REF} is a clock pulse connected to the inverter chain of the input network. Operating at a period 256 times longer than CLK_{main}, it instantaneously modulates the input signal's common-mode, generating a pulse-shaped waveform $VIN_{CP,CM}$ as depicted in Fig. 4. When the common mode pulse is injected, the replica switch and the reference switch sample simultaneously. The replica switch is situated adjacent to the sampling switch of the channel undergoing detection. The reference switch, acting as the skew reference, is centrally located within the ADC core.

This process is described in detail in Fig. 5. Fig. 5(a) shows that, when the $\Phi_{SH<1>,CAL}$ is applied, the input signal is sampled at the P and N terminals of the replica switch. The $\Phi_{SH<1>,CAL}$, like the common-mode injection, also operates at a period 256 times longer for low-power operation. After the sampling by the replica switch is complete, as shown in Fig. 5(b), the switch connecting the P and N terminals turns on by $\Phi_{CLK,CM}$, shorting them together. At this time, the

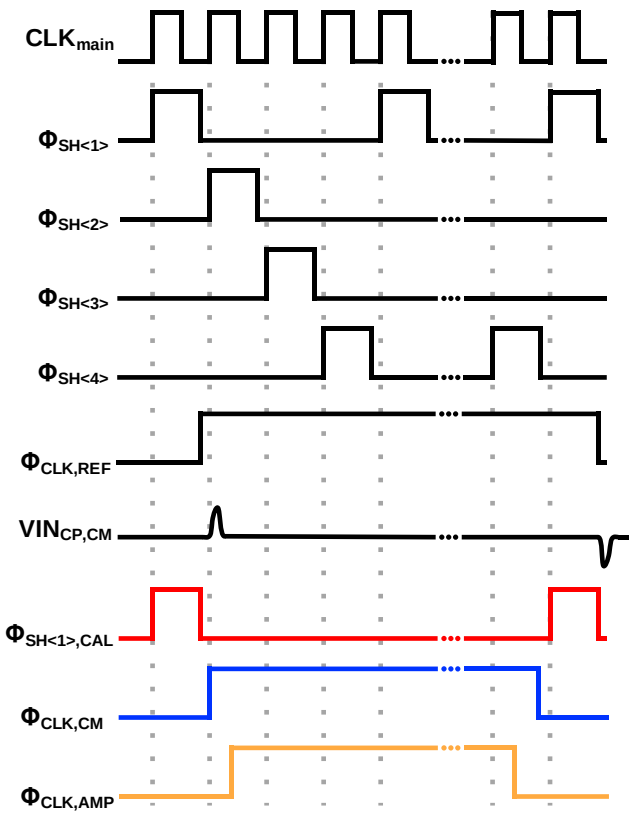

Fig. 4. Timing diagram

capacitors at P and N are connected, and the sampled common-mode voltage of the input signal is stored in the capacitor of the replica and reference switch. This stored common-mode voltage is then connected to the input of the amplifier of integrator, as shown in Fig. 5(c) and (d). At this stage, the replica switch and the reference switch are connected to opposite inputs of the amplifier, so that the difference in common-mode voltage sampled by the replica and reference switches is ultimately integrated.

The replica switch, reference switch, and amplifier together operate as a switched-capacitor integrator, as illustrated in Fig. 6. The amplifier is implemented as a static common-source based two-stage amplifier, which allows for stable operation with very low power consumption, since its bandwidth is set much lower than the ADC's operating rate. This is feasible because the integrator only needs to process signals at relatively slow detection rate, rather than at the full ADC sampling speed.

While the overall topology shares fundamental similarities with a typical switched capacitor integrator, functional difference lies in the handling of the injected common-mode signal. As shown in Fig. 4, the direction of the injected common mode alternates for each sample, a behavior directly governed by the phase of the reference clock. To ensure that the detection signal is always accumulated in the same, predetermined direction within the integrator for accurate signal build-up, the polarity of the connections between the replica and reference switches and the amplifier is reversed on every sample, as depicted in the detailed timing diagram of Fig. 7. This polarity reversal compensates for the alternating direction of the injected common mode, thereby enabling the integrator to

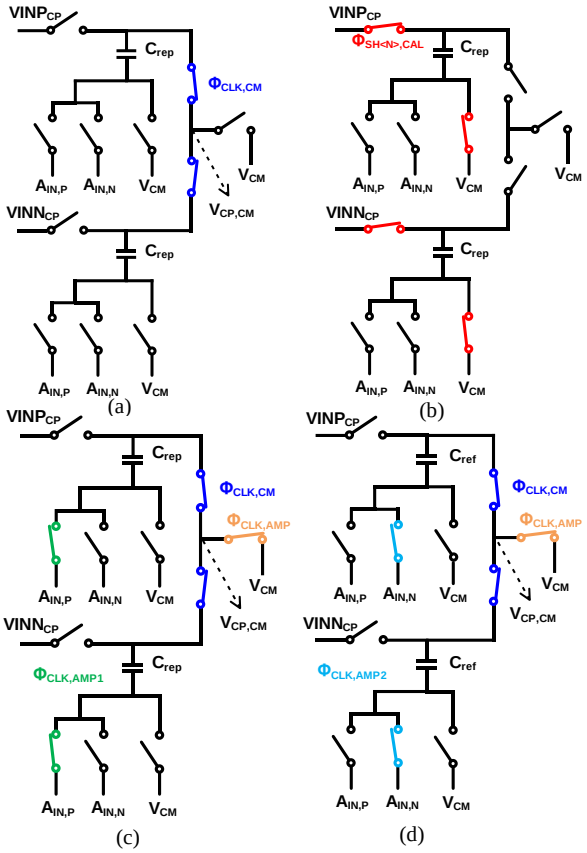

Fig. 5. Detailed common mode sampling
(a) replica and reference switch sampling (b) common mode detection
(c) connection to amplifier (d) opposite side connection

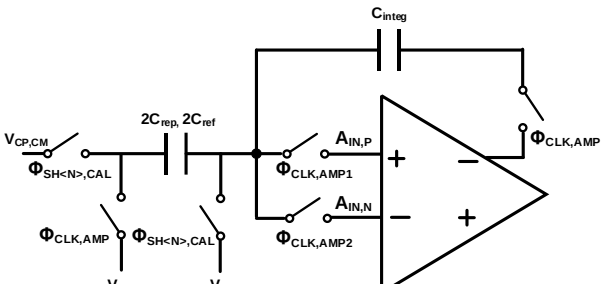

Fig. 6. Switched capacitor integrator

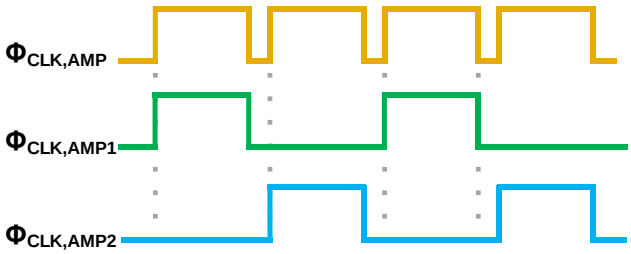

Fig. 7. Integrator timing diagram

consistently accumulate the detection signal in one direction. As a result, monotonic integration is achieved regardless of the specific phase of the injected common-mode signal.

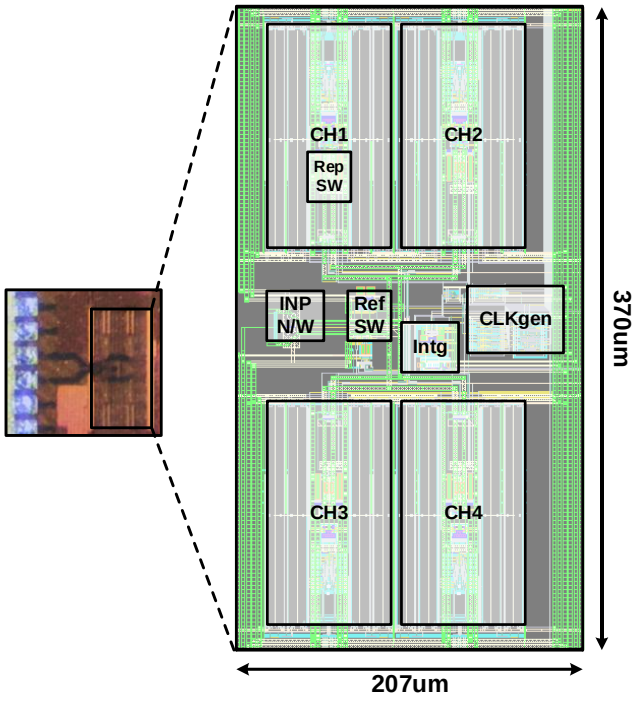

Fig. 8. Die photo

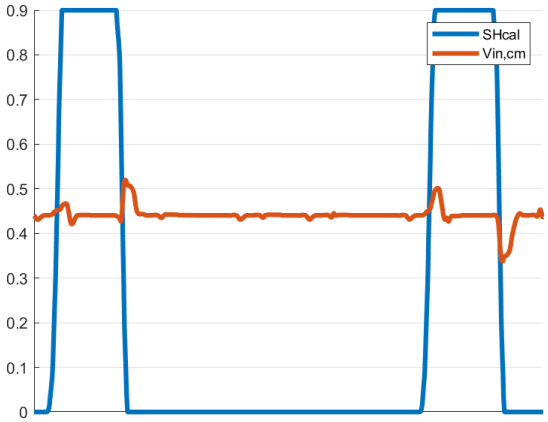

Fig. 9. Simulation result of common mode injection

III. SIMULATION RESULTS

The proposed ADC was designed using a 28-nm CMOS process and occupies an active area of 0.074 mm², as shown in Fig. 8. Due to a design error in the digital control block, simulation results are presented instead of measurement data from the fabricated die. Fig. 9 shows the simulation results for common-mode injection, where the falling edge of the sample-and-hold (SH) circuit is observed at the instant of input common-mode variation. Fig. 10 presents the integrator output under actual skew conditions, demonstrating that skew differences as small as 100 fs are distinguishable in the integrator output, and approximately 1,000 samples were required for detection. Fig. 11 illustrates the post-layout simulation FFT results for a Nyquist input at an 800 MHz sampling clock, achieving an SNDR of 61.3 dB and an SFDR of 72.6 dB. The common-mode signal was injected at a much lower frequency compared to the ADC

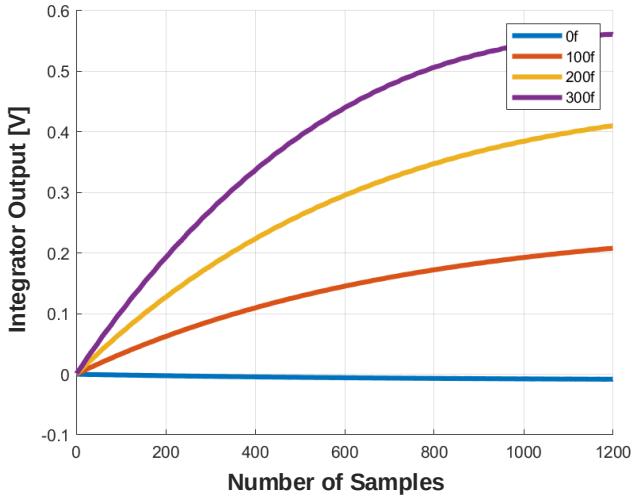

Fig. 10. Simulation result of skew integration

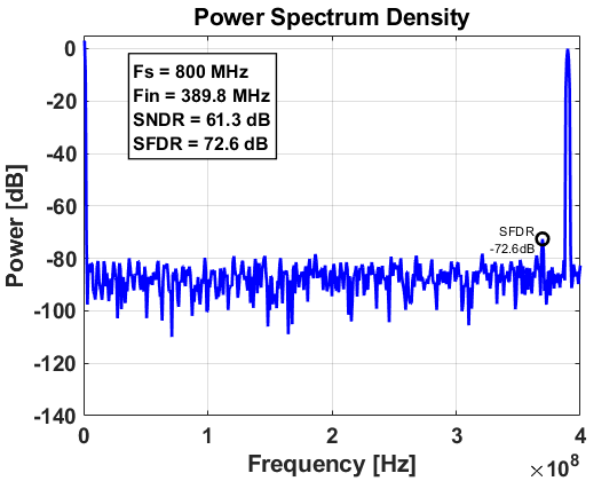

Fig. 11. Power spectral density

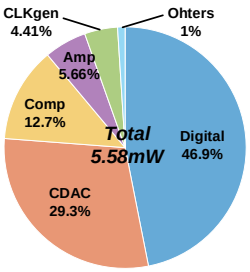

Fig. 12. Power consumption pie chart

sampling rate, thus having negligible impact on SNDR. Fig. 12 presents the power breakdown of the proposed ADC, which consumes a total of 5.58 mW, with only 316 µW consumed by the amplifier used for skew detection. The proposed ADC achieves a figure-of-merit (FoMw) of 7.74 fJ/conversion-step.

IV. CONCLUSION

This paper proposes a novel background skew detection technique for an 800 MS/s, 11-bit time-interleaved SAR ADC. The proposed method utilizes a low-speed switched-

capacitor integrator to enable low-power, on-chip background detection, allowing for the detection of skew as small as 100 fs. The proposed TI SAR ADC achieves an SNDR of 61.3 dB at a sampling rate of 800 MS/s with a Nyquist input, while consuming 5.58 mW of power and attaining a figure-of-merit (FoM) of 7.74 fJ/conv-step.

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