Latch Voltage Modulation of Cryptographic Transistor for True Random Number Generator

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Abstract – We propose a latch voltage modulation of a single MOSFET functioning as a single-transistor oscillator with an analog-to-digital converter (ADC) for a true random number generator (TRNG). The MOSFET generates irregularly oscillating analog signals due to a single transistor latch with latch-up voltage (V_{LU}) and latch-down voltage (V_{LD}), which are then converted into digitized random numbers by the ADC. To achieve a controllable TRNG, it is crucial to examine how process parameters, such as the doping concentration of the pwell (N_{pwell}) , the depth of the p-well (T_{pwell}) , and the junction depth of the source/drain (x_i) , influence V_{LU} and V_{LD} in a singletransistor oscillator implemented on a bulk-silicon wafer (1T- O_{bulk}). The randomly fluctuating output voltage (V_{out}), associated with V_{LU} and V_{LD} , serves as an entropy source for the TRNG. The random oscillation of V_{out} , generated at the drain of the 1T-O_{bulk}, was observed in a fabricated device using the TSMC 180 nm foundry process. Since aligning V_{out} from a 1T-Obulk with the input voltage range of an analog-to-digital converter (ADC) is crucial, the three aforementioned major process parameters are tuned to control V_{out} . This approach contributes to advancing next-generation security technology.

Keywords – Kink, single transistor latch, abrupt switching, oscillator, true random number generator (TRNG).

I. INTRODUCTION

Hardware-based security technology is becoming increasingly important as the use of mobile devices grows, the Internet of Things (IoT) becomes widespread, and edge computing continues to emerge [1],[2],[3],[4]. representative security chip is based on a circuit for the Advanced Encryption Standard (AES), which requires a physical unclonable function (PUF) and a random number generator (RNG). In particular, a hardware-based true random number generator (TRNG), which utilizes a naturally occurring entropy source to provide unpredictable randomness, has been proposed to enhance protection against various security threats. A TRNG surpasses a software-based pseudo-random number generator (PRNG), which generates random numbers through algorithmic processes in terms of randomness and resistance to cyberattacks [4],[5],[6].

To date, a TRNG using CMOS technology has been an

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attractive option for implementation in an AES chip due to its inherent CMOS compatibility. It commonly utilizes either a circuit or a single MOSFET. For instance, CMOS circuitbased TRNGs typically use asynchronization in a ring oscillator and mismatches in SRAM as entropy sources. However, their large footprint and the inevitably increased power consumption due to the number of required transistors introduce significant technical challenges [7],[8],[9]. As an alternative, a single MOSFET-based TRNG, operating in the traditional 'voltage input-current output' mode rather than a complex circuit, utilizes natural noise as an additional entropy source. For example, it leverages random telegraph noise stemming from imperfections at the SiO₂-Si interface in an oxide gate dielectric or random dielectric relaxation arising from the stochastic short-term recovery of charge trapping and de-trapping effects in a high-k gate dielectric [10],[11].

Recently, a novel single-transistor-based oscillator (1T-O) on a silicon-on-insulator (SOI) wafer, hereafter abbreviated as 1T-O_{SOI}, has been proposed for use in a TRNG, utilizing operation-induced signals rather than noise as the entropy source [6]. This approach eliminates the need for external circuits, which would otherwise increase the footprint area and power consumption. By removing the complex circuits, the 1T-O_{SOI} achieves a more compact and energy-efficient design. It is structurally identical to a MOSFET; however, instead of functioning as a switching transistor operating in a 'voltage input-current output' mode, it operates as an oscillator in a 'current input-voltage output' mode. This TRNG module consists of a 1T-O_{SOI}, a parasitic capacitor (C_{par}) connected in parallel with the 1T-O_{SOI}, and an analogto-digital converter (ADC) that converts oscillating analog signals into random digital bits, as shown in Fig. 1.

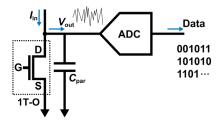


Fig. 1. A TRNG module consisting of a 1T-O, a parasitic capacitor ($C_{\rm par}$), and an ADC.

It was confirmed that a 1T-O fabricated on a bulk silicon wafer (hereafter abbreviated as 1T-O_{bulk}) using the TSMC 180 nm foundry process effectively functioned as an oscillator [12]. Applying the 1T-O_{bulk} TRNG to practical systems is significant, as it enables the integration of

peripheral circuits on a single wafer. The $1\text{T-O}_{\text{bulk}}$, operating in a 'current input-voltage output' mode, generates an oscillating output voltage (V_{out}) at the drain terminal when a constant input current (I_{in}) is applied to the same terminal, as illustrated in Fig. 2. The source is grounded.

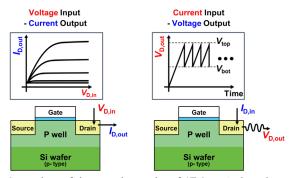


Fig. 2. Comparison of the operation modes of $1\text{T-O}_{\text{bulk}}$: 'voltage input—current output' with on-off switching and 'current input—voltage output' with oscillation, both using the same device structure.

The oscillation is based on a single transistor latch (STL). The STL exhibits abrupt switching and hysteresis due to an electrically floating body (FB) with a heavily doped p-well on a relatively lightly doped p-type wafer ($N_{\rm p_wafer}$). It occurs when the gate voltage ($V_{\rm G}$) is lower than the threshold voltage ($V_{\rm T}$), meaning the transistor is in the off state. It is important to note that the kink effect and STL are distinct, despite both originating from the floating body effect. The kink effect causes a small and gradual jump in the conventional $I_{\rm DS}$ – $V_{\rm DS}$ output characteristic plot when the MOSFET is in the on state ($V_{\rm G} > V_{\rm T}$), as shown in Fig. 3(a). In contrast, the STL in Fig. 3(b) produces a large, abrupt jump from the high-resistance state (HRS) to the low-resistance state (LRS) when the MOSFET is in the off state ($V_{\rm G} < V_{\rm T}$).

In the $I_{\rm DS}-V_{\rm DS}$ plot shown in Fig. 3(b), the voltage at which the current abruptly increases is called the latch-up voltage ($V_{\rm LU}$), while the voltage at which it decreases is called the latch-down voltage ($V_{\rm LD}$). The latch-up current ($I_{\rm LU}$) corresponds to the HRS current at $V_{\rm LU}$, while the latch-down current ($I_{\rm LD}$) corresponds to the LRS current at $V_{\rm LD}$. Due to the abrupt STL, $I_{\rm DS}$ cannot attain an intermediate current level between $I_{\rm LD}$ and $I_{\rm LU}$, creating a forbidden current region. Consequently, $I_{\rm DS}$ must be either $I_{\rm LD}$, associated with LRS, or $I_{\rm LU}$ associated with HRS. When a constant $I_{\rm in}$ between $I_{\rm LU}$ and $I_{\rm LD}$ is applied in the 'current input–voltage output' mode as shown in Fig. 2, $V_{\rm out}$ alternates between $V_{\rm LD}$ (corresponding to $V_{\rm bot}$) and $V_{\rm LU}$ (corresponding to $V_{\rm top}$).

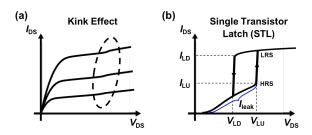


Fig. 3. (a) The kink phenomenon in the conventional $I_{\rm DS}$ - $V_{\rm DS}$ output characteristics. (b) The hysteresis by a single transistor latch in the off-state $I_{\rm DS}$ - $V_{\rm DS}$ output characteristics.

II. OPERATION MODES WITH ABRUPT SWITCHING

A. Latch-up and Latch-down with Voltage Input to Drain

The $I_{\rm DS}-V_{\rm DS}$ characteristics exhibit hysteresis, which consists of the abrupt transition of $I_{\rm DS}$ at $V_{\rm LU}$ and $V_{\rm LD}$. The mechanism of this abrupt transition is illustrated in Fig. 4, which is based on the single transistor latch (STL). The built-in potential between the n⁺-source and the p-type FB ($V_{\rm bi,SB}$) exists in the initial state, as shown in Fig. 4(a).

As $V_{\rm DS}$ increases, as shown in Fig. 4(b), when $V_{\rm DS}$ is much higher than the energy band gap of silicon divided by the unit charge q ($E_{\rm G,Si}/q$) and $V_{\rm G}$ is smaller than $V_{\rm T}$, a fraction of electrons overcoming $V_{\rm bi,SB}$ is injected into the drain via indiffusion. Another fraction of electrons contributes to the leakage current ($I_{\rm leak}$ in Fig. 3(b)) and is supplied to the drain through band-to-band tunneling in the drain junction. It is worth noting that as $V_{\rm DS}$ increases, $I_{\rm leak}$ also increases.

As shown in Fig. 4(c), electrons from the source trigger impact ionization (II), generating numerous electron-hole pairs. The generated holes temporarily accumulate in the FB, while the created electrons add to the pre-existing electrons, forming I_{leak} . These stored holes lower $V_{\text{bi,SB}}$, causing more electrons to be injected into the drain via in-diffusion, which in turn accelerates II. This leads to the generation of additional electron-hole pairs. These iterative processes create a positive feedback loop that continues until the FB is fully charged, flattening the energy band and significantly lowering $V_{\text{bi,SB}}$, as shown in Fig. 4(d).

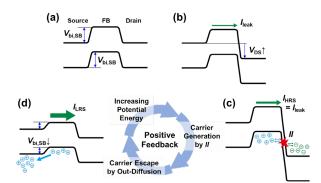


Fig. 4. Mechanism of the single transistor latch with a positive feedback loop. The energy band diagram is shown for (a) the initial state, (b) an increasing drain voltage, (c) the onset of carrier generation due to impact ionization (II), and (d) the accumulation and out-diffusion of holes, which flattens the energy band.

As $V_{\rm DS}$ reaches $V_{\rm LU}$, the $I_{\rm LU}$ corresponding to the leakage current $I_{\rm leak}$ in the HRS at $V_{\rm LU}$ suddenly rises above $I_{\rm LD}$ in the LRS. It should be noted that $V_{\rm LU}$ is observed when the 1T-O_{bulk} is in the turn-off state (HRS), while $V_{\rm LD}$ is observed when the 1T-O_{bulk} is in the turn-on state (LRS). When $V_{\rm DS}$ decreases and falls below $V_{\rm LD}$, the number of electrons supplied by II abruptly decreases, leading to an abrupt transition from $I_{\rm DS}$ in the on-state to $I_{\rm leak}$ in the off-state. Consequently, a counterclockwise hysteresis with abrupt switching at $V_{\rm LU}$ and $V_{\rm LD}$ is formed.

B. Oscillation with Current Input to Drain

When $I_{\rm in}$ is applied to the drain instead of $V_{\rm D,in}$ in the 'current input–voltage output' mode, $V_{\rm out}$ oscillates between

an upper limit (V_{top}) and a lower limit (V_{bot}). The underlying mechanism for iterative voltage oscillations is the repeated charging and discharging process, as shown in Fig. 5.

As I_{in} applied to the drain of a 1T-O_{bulk}, the supplied current at the drain raises its potential energy, as shown in Fig. 5(b). This additional potential energy is transferred to electrons forming I_{leak} as kinetic energy. Consequently, II is initiated, generating numerous electron-hole pairs, as illustrated in Fig. 5(c). The generated holes gradually and temporarily accumulate in the FB. If a sufficient number of holes accumulate, they suddenly escape from the FB via outdiffusion as source current (I_S) toward the source, as shown in Fig. 5(d), while the newly created electrons merge with existing electrons to sustain the II process. When $V_{\text{bi,SB}}$ decreases and flattens due to hole accumulation in the FB, these holes are evacuated through out-diffusion, causing I_S to flow suddenly. As shown in Fig. 5(e), the positive feedback cycle continues, and the source output current appears when the carrier escapes.

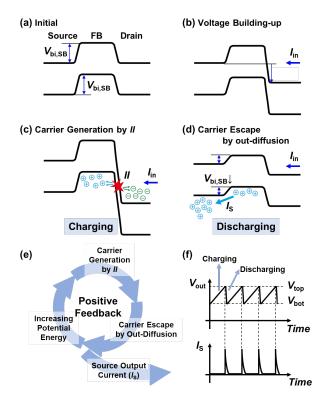


Fig. 5. Mechanism of oscillation through iterative charging and discharging. The energy band diagram is shown for (a) the initial state, (b) an increase in drain voltage due to hole accumulation from the input current, (c) carrier generation by impact ionization (II) during charging, and (d) energy band flattening due to carrier escape via out-diffusion. (e) The positive feedback loop, which includes the source output current (I_S). (f) Oscillation of V_{out} due to iterative charging and discharging, with intermittent I_S exhibiting a spike-shaped waveform.

The gradual accumulation of holes in the FB represents the charging process, while their abrupt escape through out-diffusion to the source represents the discharging process. After discharging, the $1\text{T-O}_{\text{bulk}}$ is automatically ready to begin the next charging and discharging cycle. This iterative process continues as long as I_{in} is supplied. While the output current, represented by I_{S} , intermittently flows with a spike-

shaped waveform, $V_{\rm out}$ oscillates between $V_{\rm top}$ and $V_{\rm bot}$ over time, as shown in Fig. 5(f). The linear increase represents gradual charging, while the sudden drop denotes abrupt discharging. Although the oscillating $V_{\rm out}$ is depicted as a regular waveform, the actual $V_{\rm out}$ waveform will be irregular due to the inherent time-dependent stochasticity of II and out-diffusion.

Since $V_{\rm top}$ and $V_{\rm bot}$ are determined by $V_{\rm LU}$ and $V_{\rm LD}$, respectively, controlling $V_{\rm LU}$ and $V_{\rm LD}$ is crucial for engineering the oscillation voltage range. This can be achieved by adjusting various process parameters, including the doping concentration of the p-well ($N_{\rm pwell}$), the depth of the p-well ($T_{\rm pwell}$), and the junction depth of the source/drain ($T_{\rm ij}$). The magnitude of the oscillation voltage variation is quantified as the peak-to-peak voltage ($T_{\rm ip} = T_{\rm top} - T_{\rm bot}$).

In this work, the hysteresis curve in Fig. 3(b) was analyzed by varying $N_{\rm pwell}$, $T_{\rm pwell}$, and $x_{\rm j}$ to control $V_{\rm LU}$ and $V_{\rm LD}$, thereby defining the oscillation voltage range from $V_{\rm top}$ to $V_{\rm bot}$. The Synopsys Sentaurus TCAD L-2021.03 simulation tool was used to investigate how these process parameters influence $V_{\rm out}$ characteristics. Subsequently, we confirmed that the fabricated 1T-O_{bulk}, using the TSMC 180 nm foundry process, exhibited random oscillations of $V_{\rm out}$ at the drain.

III. PROCESS PARAMETERS

To investigate the effects of process parameters on $V_{\rm LU}$ and $V_{\rm LD}$, TCAD simulations were performed. The major process parameters used in the simulations are summarized in Table I. A cross-sectional schematic of the 1T-O_{bulk} used for simulation is shown in Fig. 6(a). The gate length ($L_{\rm G}$) was fixed at 200 nm, and the area factor of the gate width in the 2D simulation was set to 0.5. The gate oxide thickness was fixed at 30 nm, and $N_{\rm p_wafer}$ was 5×10^{16} cm⁻³. Using these baseline parameters, simulations were conducted with varying $N_{\rm pwell}$, $T_{\rm pwell}$, and $x_{\rm j}$ to evaluate their effects on $V_{\rm LU}$ and $V_{\rm LD}$. During the simulations, $V_{\rm GS}$ was fixed at -2 V to keep the 1T-O_{bulk} in the off state, resulting in a more pronounced STL rather than a smaller kink effect.

TABLE I. Process parameters for simulation

Device Parameter	Value
Gate length, $L_{\rm G}$ (nm)	200
Area factor for gate width	0.5
Gate oxide (SiO ₂) thickness, T_{ox} (nm)	30
Depth of the p-well, T_{pwell} (nm)	60 (split)
Junction depth, x_j (nm)	50 (split)
P-well doping concentration, N_{pwell} (cm ⁻³)	1×10 ¹⁸ (split)
Substrate doping concentration, N_{p_wafer} (cm ⁻³)	5×10 ¹⁶

The difference in doping concentrations between $N_{\rm pwell}$ and $N_{\rm p_wafer}$ induces an additional built-in potential barrier ($V_{\rm bi}$), as depicted in Fig. 6(b). Consequently, the p-well overlying the p-type wafer creates an electrical floating body even in a bulk device (FB_{bulk}). Although $qV_{\rm bi}$ in a 1T-O_{bulk} is much smaller than the 4.5 eV energy band offset between the

channel silicon and the buried oxide in a 1T-O_{SOI} , the FB_{bulk} functions as a virtual FB, similar to how the physical floating body in a device on a SOI wafer (FB_{SOI}) serves as a real FB. In this work, the functionality of the FB_{bulk} was experimentally verified.

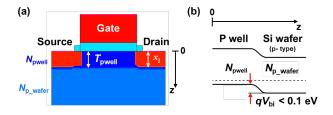


Fig. 6. (a) Cross-sectional view of a 1T-O_{bulk} for simulation. (b) Energy band diagram along the depth direction in Fig. 7(a) to show $V_{\rm bi}$.

IV. RESULTS AND DISCUSSIONS

A. Effects of P-well Doping Concentration (N_{pwell}) on Latch Hysteresis

Understanding the correlation between the process parameters mentioned above and latch voltages is crucial for optimizing the oscillation voltage range, which serves as the input for the ADC in a 1T-O_{bulk}-based TRNG chip.

Fig. 7 shows the simulated results of latch-up and latch-down hysteresis with various doping concentrations in the channel and the corresponding values of the latch-up and latch-down voltages. Since the aforementioned $V_{\rm bi}$, which modulates the strength of the FB_{bulk} effect, is quantitatively modeled as $(kT/q)\cdot \ln(N_{\rm pwell}/N_{\rm p_wafer})$, a $N_{\rm pwell}$ is varied from 5×10^{16} cm⁻³ to 1×10^{18} cm⁻³ to explore its effect on $V_{\rm LU}$ and $V_{\rm LD}$.

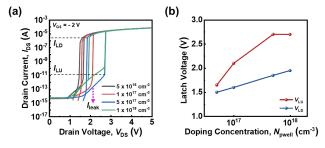


Fig. 7. (a) Simulated latch-up and latch-down hysteresis with various doping concentrations at the channel. (b) Extracted values of the $V_{\rm LU}$ and $V_{\rm LD}$.

As $N_{\rm pwell}$ increases, $V_{\rm bi}$ becomes larger, and the depletion width–proportional to $(N_{\rm pwell})^{-0.5}$ –narrows in the p-well, resulting in steeper energy band bending. These effects suppress the number of electrons surmounting the energy barrier of $qV_{\rm bi}$ and diffusing into FB_{bulk}. A steep energy barrier and a low doping concentration reduce the impact ionization rate ($II_{\rm rate}$), as depicted in Fig. 8(a). The values of $I_{\rm LU}$ and $I_{\rm LD}$ are extracted in Fig. 8(b). These results confirm that a 1T-O_{bulk} with a higher $N_{\rm pwell}$ requires a larger $I_{\rm LU}$. This is because a higher energy barrier, induced by increased $N_{\rm pwell}$, demands greater hole accumulation to sufficiently lower the barrier. As $I_{\rm LU}$ increases, the voltage needed to

trigger latch-up also increases, resulting in a higher $V_{\rm LU}$ [13]. This effect is influenced by the energy band profile, particularly the abruptness of $qV_{\rm bi}$. These findings provide a foundation for further refinement of doping strategies in device design.

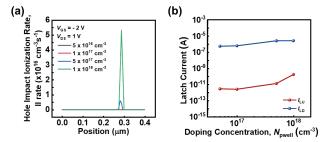


Fig. 8. (a) Hole impact ionization rate of the drain voltage $V_{\rm DS} = 1~{\rm V}$ and $V_{\rm GS} = -2~{\rm V}$ with various doping concentrations at the channel. (b) Extracted values of the $I_{\rm LU}$ and $I_{\rm LD}$.

B. Effects of P-well Depth (T_{pwell}) on Latch Hysteresis

The physical volume of the FB_{bulk} (Vol_{FB}) is the key factor as the physical space to accommodate the holes. It is roughly estimated as $L_{G} \cdot W_{CH} \cdot T_{pwell}$, where W_{CH} is the channel width. Since L_{G} and W_{CH} were fixed, only T_{pwell} serves as the variable determining Vol_{FB} . Therefore, T_{pwell} influences V_{LU} and V_{LD} because this volume determines how many holes generated by II accumulate in the FB_{bulk}.

Fig. 9(a) illustrates the $I_{\rm DS}-V_{\rm DS}$ plot, showing various latch voltages with hysteresis ($V_{\rm hys}=V_{\rm LU}-V_{\rm LD}$). Fig. 9(b) reorganizes the corresponding $V_{\rm LU}$ and $V_{\rm LD}$ values extracted from the hysteresis for different $T_{\rm pwell}$ values. It is observed that $V_{\rm LU}$ increases as $T_{\rm pwell}$ deepens because a deeper $T_{\rm pwell}$ requires more holes generated by II to completely fill $Vol_{\rm FB}$, which in turn increases in $V_{\rm LU}$ to generate additional holes. In contrast, $V_{\rm LD}$ remains insensitive to changes in $T_{\rm pwell}$. These differing dependencies arise from the distinct mechanisms governing hole accumulation in $Vol_{\rm FB}$ during latch-up and hole evacuation during latch-down. $V_{\rm LU}$ depends predominantly on how quickly the holes fill $Vol_{\rm FB}$. On the other hand, $V_{\rm LD}$ depends primarily on when impact ionization is halted due to insufficient low voltage.

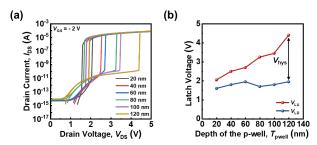


Fig. 9. Simulated latch voltages as a function of $T_{\rm pwell}$ (a) Plot of $I_{\rm DS}-V_{\rm DS}$ showing latch-up, latch-down, and hysteresis for various $T_{\rm pwell}$ values. (b) Extracted values of the $V_{\rm LU}$ and $V_{\rm LD}$.

During the latch-up process, which causes an abrupt increase in $I_{\rm DS}$ from HRS to LRS, the rate at which the holes generated by II fill $Vol_{\rm FB}$ determines $V_{\rm LU}$. Therefore, the extent to which $Vol_{\rm FB}$ is filled is a crucial factor. In contrast, $V_{\rm LD}$ depends primarily on how quickly the holes within $Vol_{\rm FB}$ are evacuated. During the latch-down process, an abrupt

reversal in $I_{\rm DS}$ from LRS to HRS, $Vol_{\rm FB}$ is already filled under high $I_{\rm DS}$ conditions. As a result, $T_{\rm pwell}$ does not significantly influence $V_{\rm LD}$. Since $V_{\rm LU}$ increases while $V_{\rm LD}$ remains unchanged, $V_{\rm hys}$ becomes wider as $T_{\rm pwell}$ deepens, as shown in Fig. 9(b). These results demonstrate the significant role of $T_{\rm pwell}$ in tuning the oscillation voltage range, providing a practical guideline for optimizing device design through process parameter control.

C. Effects of Junction Depth (x_i) on Latch Hysteresis

The variable x_j primarily impacts the leakage current (I_{leak}) at HRS and the II_{rate} rather than directly affecting Vol_{FB} . This x_j controls the magnitude of I_{leak} , which is proportional to the number of electrons (N_{elec}) supplied by the aforementioned BTBT. It drives impact ionization because a larger N_{elec} results in a higher II_{rate} .

Fig. 10(a) presents a plot of I_{DS} – V_{DS} for various x_j values, and the extracted values of V_{LU} and V_{LD} are shown in Fig. 10(b). During the latch-up process, V_{LU} decreases as x_j increases. A deeper x_j results in a higher leakage current due to the enhanced BTBT, which triggers more II, causing holes to fill Vol_{FB} more quickly. Consequently, V_{LU} decreases.

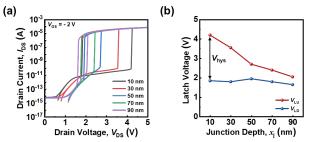


Fig. 10. (a) Simulated latch-up and latch-down hysteresis with various junction depths. (b) Extracted values of the $V_{\rm LU}$ and $V_{\rm LD}$.

In contrast, during the latch-down process, $V_{\rm LD}$ remains nearly unchanged even as x_i deepens. As mentioned above, $V_{\rm LD}$ is insensitive to the size of $Vol_{\rm FB}$ because $Vol_{\rm FB}$ is already filled with holes generated by II, which significantly outweighs the contribution from BTBT. The current from II $(I_{\rm II})$ is proportional to $\exp(-B_{\rm II}/E)$, while the current from BTBT (I_{BTBT}) is proportional to $\exp(-B_{BTBT}/E)$, where E is the electric field, and $B_{\rm II}$ and $B_{\rm BTBT}$ are parameters governing II and BTBT, respectively. Since B_{BTBT} is nominally more than 10 times larger than B_{II} , I_{BTBT} is much smaller than I_{II} . Hence, I_{BTBT} does not significantly contribute to total hole generation compared to II. As a result, x_j does not influence $V_{\rm LD}$, just as $T_{\rm pwell}$ does not affect $V_{\rm LD}$. Since $V_{\rm LU}$ notably decreases while $V_{\rm LD}$ remains unchanged, $V_{\rm hys}$ becomes narrower as x_i deepens. These results provide insight into how x_i can be leveraged to fine-tune the oscillation characteristics of 1T-O_{bulk}, enabling more precise control over device behavior through process optimization.

D. Co-relation of Latch Hysteresis and the Oscillation

As mentioned above, $V_{\rm LU}$ and $V_{\rm LD}$ in the hysteresis correspond to the upper and lower limits ($V_{\rm top}$ and $V_{\rm bot}$) in the oscillation voltage of the 'current input-voltage output' mode. Before experimental verification, the oscillation

behavior was confirmed using the Sentaurus simulation tool with the current source voltage measurement (CSVM) method. An $I_{\rm in}$ of 10 nA, between $I_{\rm LU}$ and $I_{\rm LD}$, was applied to the drain of the 1T-O_{bulk}, which was connected in parallel with a 100 pF $C_{\rm par}$, and the output voltage was measured at the same drain. The process parameters used for the simulations are summarized in Table I; however, $N_{\rm pwell}$ was set to 1×10^{17} cm⁻³ to ensure that $V_{\rm pp}$ exceeds 0.2 V. As shown in Fig. 11, $V_{\rm LU}$ corresponds to $V_{\rm top}$ and $V_{\rm LD}$ corresponds to $V_{\rm bot}$ in the $V_{\rm out}$ waveform. The simulated $V_{\rm out}$ appears to oscillate periodically and regularly because data sampling of the oscillating $V_{\rm out}$ was performed at the same point in each cycle.

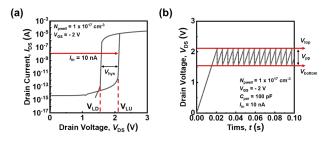


Fig. 11. (a) Simulated latch-up and latch-down hysteresis at N_{pwell} of 1×10^{17} cm⁻³. (b) Simulated oscillation output drain voltage using the current source voltage measurement (CSVM).

The hysteresis caused by STL and the oscillation characteristics were measured using a semiconductor parameter analyzer (B1500A) from the fabricated 1T-O_{bulk} using the TSMC 180 nm process. The gate length was 180 nm, and the gate width was 300 nm. Fig. 12(a) shows the measured $I_{\rm DS}$ vs. $V_{\rm DS}$ characteristics with the gate floating. It represents the hysteresis with abrupt switching, including $V_{\rm LU}$ and $V_{\rm LD}$. In Fig. 12(b), an $I_{\rm in}$ of 20 μ A was applied to the drain of a 1T-O_{bulk} to produce oscillating $V_{\rm out}$ with 1 nF of $C_{\rm par}$. The experimentally measured $V_{\rm out}$ oscillated non-periodically and irregularly.

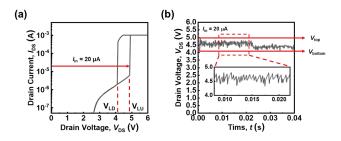


Fig. 12. (a) Measured latch-up and latch-down hysteresis from the fabricated 1T-O_{bulk} with the gate length of 180 nm and the gate width of 300 nm using the voltage source current measurement (VSCM). (b) Measured oscillating V_{out} using the current source voltage measurement (CSVM).

This irregularity arises from inherent random fluctuations caused primarily by carrier generation via II and the escape of carriers through out-diffusion, which is further associated with recombination at the source/drain junction and the temporal stochasticity of hole accumulation. These effects become more pronounced under gate-floating conditions. Additional fluctuations in $V_{\rm out}$ are attributed to the low sampling rate, which is limited by the resolution of the

parameter analyzer. When a sampling time interval of 100 μ s—too large to capture the regular frequency—was used, an irregular oscillation shape was observed. Despite this irregularity, the results confirm that $V_{\rm LU}$ corresponds to $V_{\rm top}$ and $V_{\rm LD}$ corresponds to $V_{\rm bot}$ in the $V_{\rm out}$ waveform.

The ADC outputs were extracted using MATLAB and evaluated using the NIST SP 800-22 statistical test suite to assess their randomness. An 8-bit ADC was implemented, and the least significant 4 bits (LSB 4) were used for testing. A total of 25,000 bits were collected and divided into 10 bitstreams of 2,500 bits each. Among the applicable tests, seven tests exhibited a pass rate higher than 0.7, satisfying the NIST criteria. Detailed results of each statistical test are summarized in Table II. Although limited in scale, these preliminary results suggest that the proposed device can serve as a viable entropy source for TRNG applications. Further improvements in both randomness quality and operational reliability are anticipated through voltage and oxide thickness optimization.

TABLE II. NIST SP 800-22 Statistical Test Results

Statistical test	Pass rate
Frequency (monobit)	0.8
Frequency within a Block	0.9
Runs	0.8
Longest Run of Ones in a Block	0.9
Discrete Fourier Transform	1.0
Cumulative Sums	0.8
Linear Complexity	0.9

The continuous and random oscillation of $V_{\rm out}$ generates a set of random digital bits through an ADC, enabling the 1T-O_{bulk} to function as a TRNG. The output voltage range of the 1T-O_{bulk} could be adjusted to match the input voltage range of the ADC, ensuring seamless integration for TRNG applications.

V. CONCLUSION

This study investigates techniques for controlling the output voltage (Vout) range of a single-transistor-based oscillator (1T-O_{bulk}), which offers a smaller footprint and lower power consumption than circuit-based oscillators. The inherent randomness of V_{out} , arising from irregular carrier generation and escape, serves as an entropy source. The goal is to optimize the voltage range for integration into a true random number generator (TRNG) module with an analogto-digital converter (ADC). To ensure compatibility between the 1T-O_{bulk} and the ADC, it is essential to align V_{out} with the ADC's input voltage range, which involves lowering the voltage of the single transistor latch. This adjustment requires fine-tuning process parameters during fabrication. Using Sentaurus TCAD simulations, we analyzed latch-up and latch-down characteristics across different doping concentrations of the p-well (N_{pwell}), p-well depth (T_{pwell}), and source/drain junction depth (x_i) . Our findings indicate that reducing N_{pwell} and T_{pwell} while increasing x_{j} helps improve voltage matching. These insights provide a foundation for optimizing 1T-O_{bulk} design and facilitating its integration with an ADC for TRNG applications.

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