Development of an Optimized Single-Slope Analog-to-Digital Converter Readout Circuit for Gas Sensing Systems

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Abstract **- This paper presents the design and implementation of a readout integrated circuit (ROIC) optimized for gas sensor applications. The proposed ROIC integrates essential components, including a ramp generator, digital DDR counter, comparator, and peripheral bias generation blocks, to ensure accurate signal processing. The ROIC achieves a power consumption of 1.31 mW and operates with a 1.2V input range, achieving a 62.5 kHz conversion rate and a performance of 9.41 bits effective number of bits (ENOB). Additionally, the figure of merit (FoM) of the system is measured at 30.81 pJ/step. The results indicate that the proposed ROIC provides a robust solution for high-precision gas sensing systems, demonstrating its potential to significantly enhance the performance of sensor-based applications, particularly in environments that require fast and accurate measurements. The chip, fabricated using TSMC 180nm CMOS technology, shows promise for real-world applications in industrial and environmental monitoring.**

Keywords **— Gas sensor, readout integrated circuit (ROIC), single-slope analog-to-digital conversion (ADC), slow response gas sensing system.**

I. INTRODUCTION

Gas sensor systems have become indispensable in various fields, such as hazardous gas detection, environmental monitoring, and smart home systems in industrial environments [1]. These sensors employ diverse sensing methods, including semiconductor-based, electrochemical, and infrared techniques [2], [3]. Among these, electrochemical and semiconductor-based gas sensors are widely used due to their relatively low cost, excellent sensor sensitivity, and adaptability. Despite these advantages, several challenges persist in the effective deployment of gas sensor systems, primarily related to sensor performance under varying environmental conditions. Issues such as initial instability, slow response times, and sensitivity fluctuations due to environmental factors like temperature and humidity are common [4], [5].

These factors significantly impact the overall performance of the sensor and complicate its use in real-world applications. In the context of such challenges, the development of a suitable readout integrated circuit (ROIC) for gas sensors is crucial for ensuring the accurate reading and processing of sensor signals [6], [7]. ROICs are integral in converting the analog output signals from gas sensors into digital data, which can then be analyzed for meaningful information.

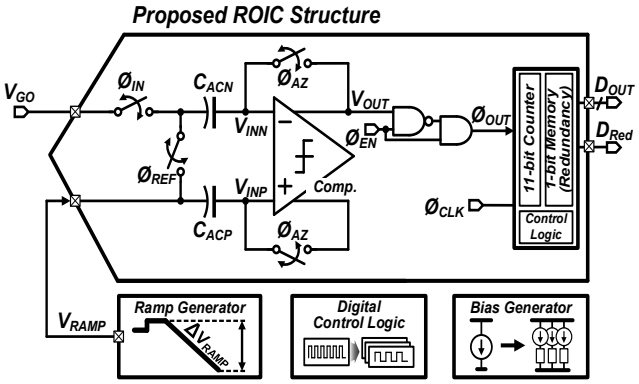

Fig. 1. Hardware architecture of the proposed ROIC.

This paper focuses on the development of an optimized ROIC for gas sensor systems based on a single-slope analog-to-digital converter (ADC) architecture. To address the performance issues mentioned, we introduce an auto-zeroing technique that enhances the stability and accuracy of the sensor output. Furthermore, an AC-coupled input network is employed to effectively detect and adjust the input signal levels from the gas sensor, compensating for the sensor's environmental sensitivity. The design also incorporates a ramp generator for generating an SS A/D reference, ensuring that temperature and humidity variations during signal extraction are properly accounted for. These design features aim to mitigate the volatility and slow response of gas sensors, thereby improving their performance in practical gas sensor applications.

The remainder of this paper is organized as follows: Section II provides a detailed description of the proposed ROIC. Section III outlines the measurement results and a discussion of the ROIC's performance. Finally, Section IV presents the conclusions.

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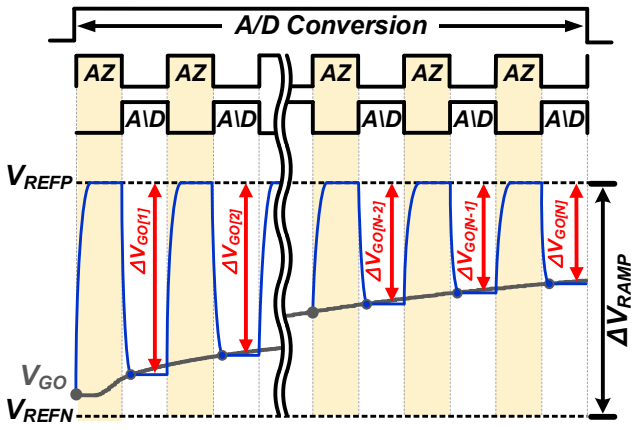


Fig.2. Simplified operation of the proposed ROIC.

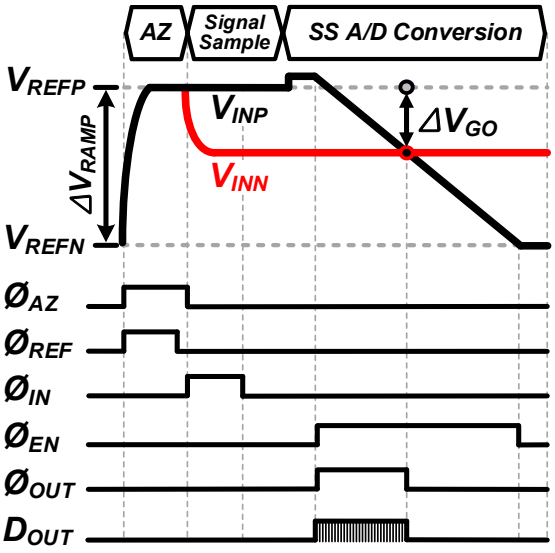


Fig.3 Simplified readout timing diagram of proposed ROIC.

II. PROPOSED ROIC HARDWARE ARCHITECTURE AND OPERATION

A. Proposed ROIC Hardware Architecture

Fig.1 shows the hardware architecture of the ROIC based on the proposed single-slope ADC [8], [9]. The main components of the circuit include an AC-coupled input network, which is responsible for effectively extracting the gas sensor's signal. Additionally, a comparator is used to compare the input signal with the reference signal, while a ramp generator creates the reference signal required for the A/D conversion process. The system also includes a digital counter to manage the conversion process. Furthermore, the architecture is equipped with digital control logic for precise timing control and a bias generator to provide the necessary bias supply. The proposed ROIC performs single-slope A/D conversion, which processes changes in the input signal after the auto-zeroing procedure. The AC-coupled input network ensures that the input signal is correctly extracted, while the timing and operation of all unit blocks are synchronized to ensure optimal system performance.

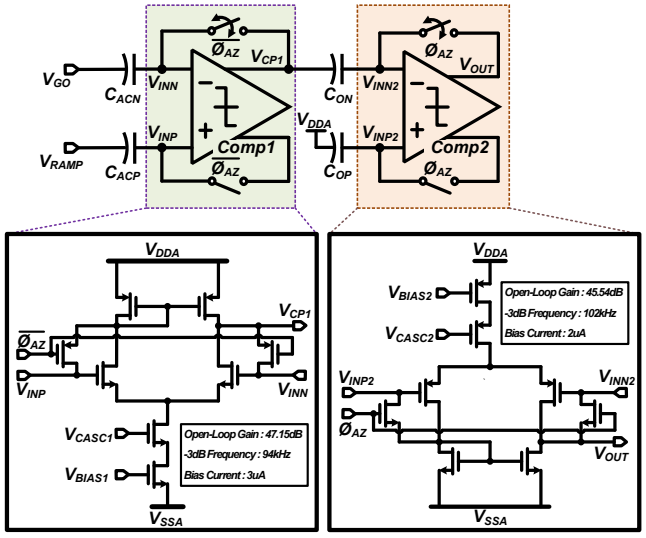


Fig.4. Comparator design of the proposed ROIC.

B. Description of the Proposed ROIC Operation

Fig.2 illustrates the simplified operation of the proposed ROIC. The ROIC operates within the output range (ΔV_{RAMP}) defined by the ramp generator. During each auto-zeroing process, the output voltage of the ramp generator is initialized, and the input signal voltage, V_{GO}, is adjusted by the difference ΔV_{GO}. This process enables the conversion of the input signal into a digital output. This method, which is repeated several times, is particularly effective in compensating for slow response characteristics inherent in resistive gas sensors, typically on the order of tens to hundreds of seconds. To mitigate the reduction of signal-to-noise ratio (SNR) caused by signal leakage, the ROIC incorporates an optimization technique based on the initial reference voltage provided by the ramp generator. In the case of resistive gas sensors, there are various sensor circuits, such as voltage dividers, Wheatstone bridges, and transimpedance amplifier structures [10], [11], [12]. While these structures are commonly used, the proposed structure features an AC-coupled input design, which effectively utilizes the ROIC's dynamic range, regardless of the initial value of the reference voltage. This technique is applicable to general gas sensor signal extraction circuits, ensuring optimized signal processing by maximizing the dynamic range of the ROIC without being affected by variations in the initial reference voltage. This optimization ensures that changes in the sensor signal are accurately tracked while minimizing errors caused by external factors or environmental conditions.

Fig.3 presents the simplified operation timing diagram for the proposed ROIC, depicting the flow of the input signal V_{GO} during the three main phases of operation: the auto-zeroing phase, the signal sampling phase, and the single-slope A/D conversion phase. In the initial auto-zeroing phase, the $Ø_{REF}$ switch is turned on, and the bottom plate of the coupling capacitor C_{AC} is sampled with the initial voltage V_{REFP} from the ramp generator. After this sampling, the $Ø_{AZ}$ and $Ø_{REF}$ switches are turned off, and the $Ø_{IN}$ switch is

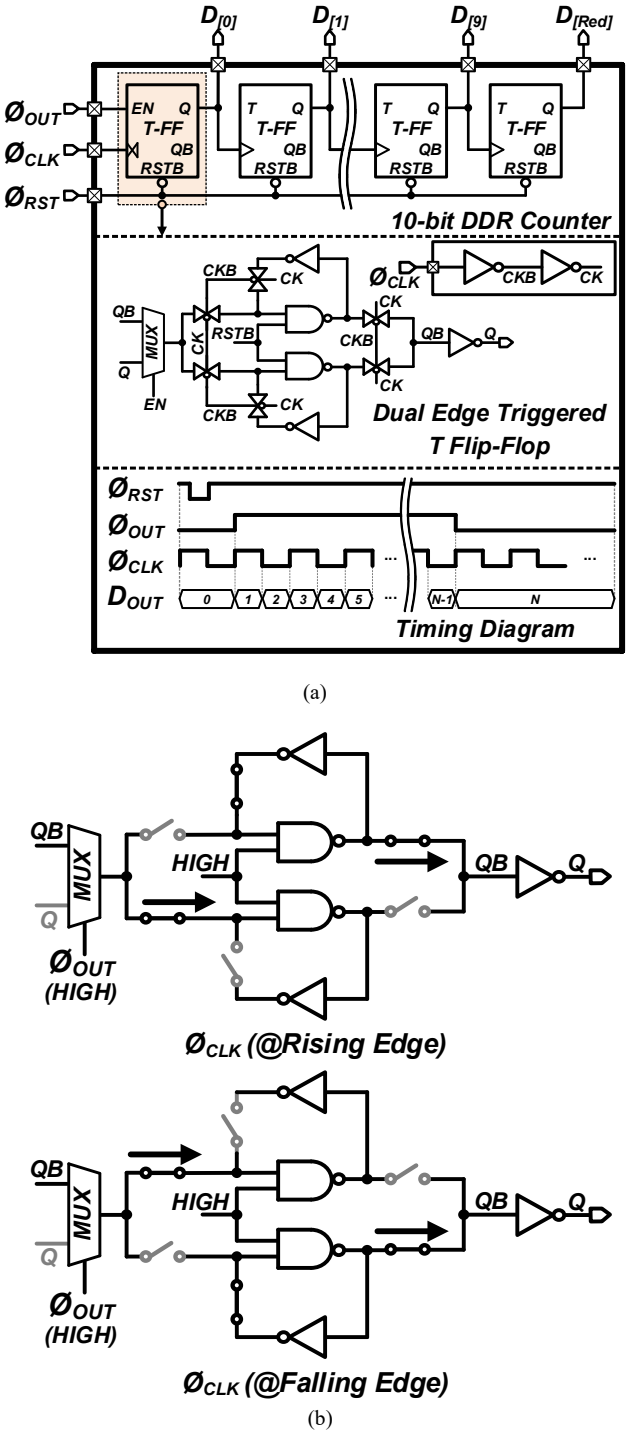


Fig.5. (a) Block diagram of the DDR Counter design with timing diagram, and (b) Dual edge triggered T flip-flop operation at rising and falling edges.

activated. The voltage V_{REFP} from the previous phase is then sampled. Following this, the input signal V_{GO} is applied, causing a change in the signal. This change is then transmitted to the negative input of the comparator (V_{INN}). Finally, in the SS A/D conversion phase, the $Ø_{EN}$ switch is turned on, and the ramp generator is activated. The ΔV_{RAMP} generated by the ramp is synchronized with the clock signal ($Ø_{CLK}$) and is delivered to the positive input of the comparator (V_{INP}), completing the A/D conversion process.

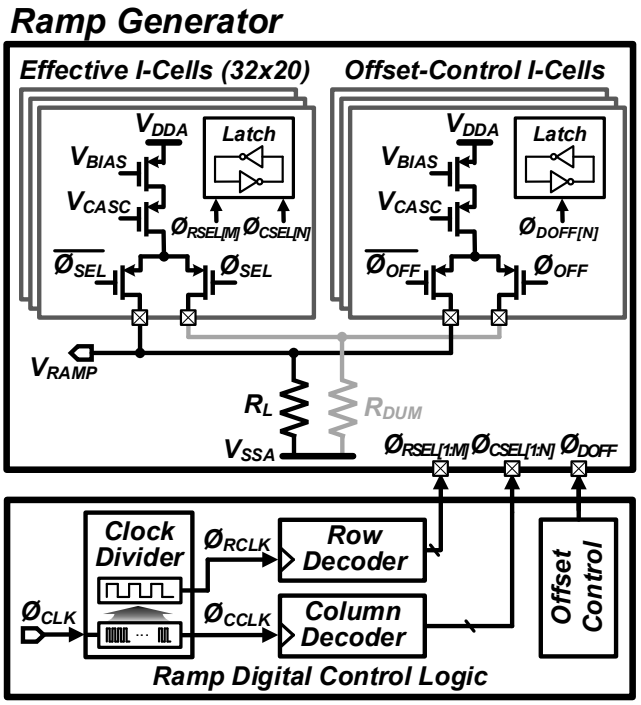
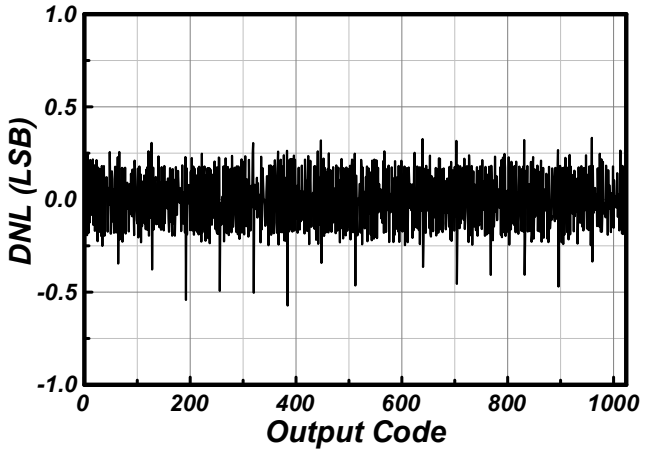


Fig.6. Current DAC-Based ramp generator architecture of the proposed ROIC.

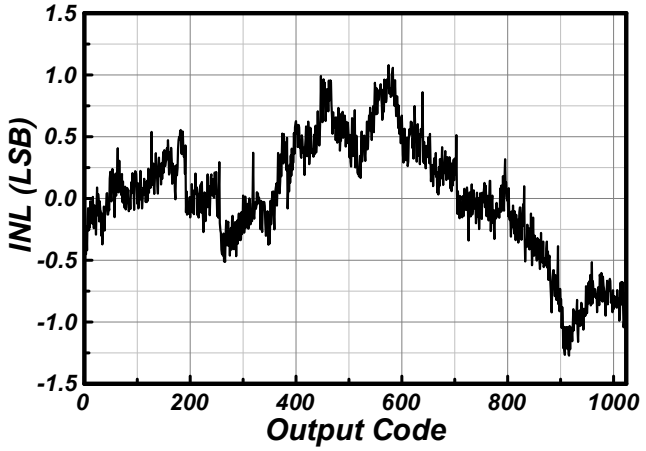
III. PROPOSED ROIC DESIGN AND IMPLEMENTATION

Fig.4 shows the comparator design of the proposed ROIC. The comparator consists of a two-stage continuous-time comparator architecture. The first stage is based on an NMOS-based operational transconductance amplifier (OTA), and the second stage is based on a PMOS-based OTA. The NMOS-based OTA operates with a bias current of 3 μA, providing an open-loop gain of 47.15 dB and a 3dB cutoff frequency of 94 kHz. The PMOS-based OTA, on the other hand, operates with a bias current of 2 μA, providing an open-loop gain of 45.54 dB and a 3dB cutoff frequency of 102 kHz. As a result, the overall comparator achieves a total gain of 92.69 dB. The output signal of the comparator, V_{OUT}, is combined with the $Ø_{EN}$ signal through a NAND logic gate to generate the final output signal $Ø_{OUT}$. This output is then transmitted to the digital counter logic, which controls the timing of the counter's operation.

Fig.5(a) shows the block diagram of the double data rate (DDR) counter design used in the proposed ROIC [13]. The counter is built using an asynchronous architecture, with the least significant bit (LSB) flip-flop constructed from a dual-edge T-Flip Flop to perform DDR operations. Fig.5(b) illustrates the operation of the dual-edge T flip-flop, showing both the rising edge and falling edge behaviors. The dual-edge T flip-flop consists of two parallel latches, and is controlled by the $Ø_{RST}$ signal for reset. The operation occurs on both the rising and falling edges of the $Ø_{CLK}$ signal. In each clock cycle, one latch stores the toggled output, while the other latch outputs the data stored during the previous edge. This configuration allows the counter to trigger both



(a)



(b)

Fig. 7. Measured linearity of the proposed ROIC : (a) DNL and (b) INL

on the rising and falling edges of the clock signal, effectively generating two counts per clock cycle. The system is synchronized with the master clock, which ensures that the counter operates in a precise and reliable manner. The counter design consists of 11 T-Flip Flops, which are included to read the redundancy code of the 256 steps. The counter performs a digital up-counting operation based on the comparison output signals $Ø_{OUT}$ and $Ø_{EN}$, which drive the counting process. This structure ensures high efficiency and accuracy in the timing operations within the ROIC.

Fig.6 shows the simplified schematic of the current-DAC-based ramp generator architecture proposed for the ROIC. This ramp generator is an integrated block used to generate the reference signal V_{RAMP}. It consists of two main types of current cells: the effective current cells for generating the ramp signal swing and the offset-control current cells for managing offset control. Each current cell utilizes a thermometer structure, where the current flow is regulated to produce the desired voltage levels for V_{RAMP}. The switch signals for the current cells are controlled by a clock divider, synchronized with the $Ø_{CLK}$ signal. The effective current cells are configured in a 32 × 20 arrangement, allowing for precise control of the ramp output. The column decoder, controlled by the $Ø_{CCLK}$, ensures synchronization with the master clock $Ø_{CLK}$, enabling DDR operation. The row

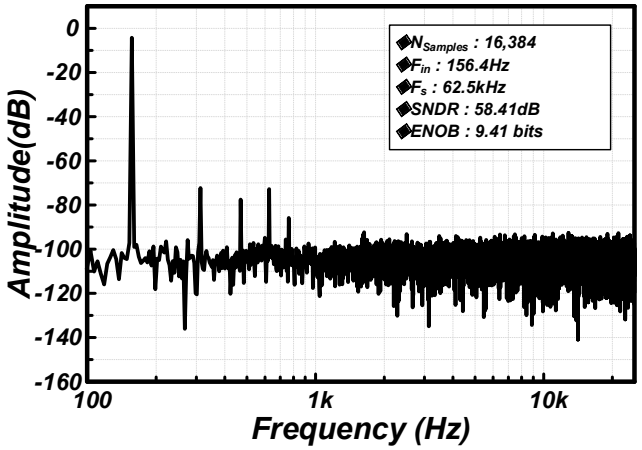


Fig.8. FFT results of the proposed ROIC.

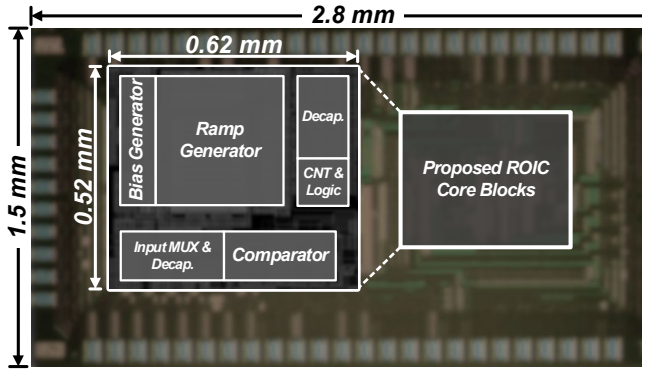


Fig.9. Chip microphotograph.

decoder and column decoder are structured based on shift registers. The row decoder sequentially selects 32 rows with the $Ø_{RCLK}$ signal, while the column decoder sequentially selects 20 columns with the $Ø_{CCLK}$ signal. The M^{th} row signal $Ø_{RSEL[M]}$ and the N^{th} column signal $Ø_{CSEL[N]}$ control the current cell's latch within the M^{th} row and N^{th} column, respectively. These signals control the amount of current passed through the ramp's load resistance R_L, thus determining the ramp output voltage level V_{RAMP}. With a total of 1,280 steps in the current DAC, the output DC levels for the reference voltages V_{REFP} and V_{REFN} are adjusted to maintain accurate input signal levels, ensuring reliable signal processing throughout the ROIC.

IV. MEASUREMENT RESULTS AND DISCUSSION

Fig.7 presents the results of the differential nonlinearity (DNL) and integral nonlinearity (INL) measurements for the proposed ROIC. The measurements were taken for a 10-bit resolution, yielding a maximum DNL of +0.332, and a minimum DNL of -0.572. For INL, the maximum value recorded was +1.081, while the minimum value was -1.272.. The DNL variation was observed to occur around the 64th column, which corresponds to a change in the ramp generator's current cell during the readout process. This pattern is consistent with the expected behavior of the current cell structure, confirming that the nonlinearity effects

TABLE I. PERFORMANCE TABLE

Parameter	Value	
Technology	TSMC 0.18μm CMOS Process	
Supply Voltages	2.8 V (Analog), 1.8 V(Digital)	
Input Range	1.2 V	
Power Consumption	Ramp Gen.	1.1 mW
	Comparator	22 uW
	Digital	28 uW
	Bias Gen.	0.16 mW
	Total	1.31 mW
ADC Resolution	10 bits	
Conversion Rate	62.5 kHz	
ENOB	9.41 bits	
DNL	+0.332 / -0.572	
INL	+1.081 / -1.272	
*FoM	30.81 pJ/Conv.	

*$FoM = Power / (Conversion\ Rate \times 2^{ENOB})$

are primarily influenced by the signal extraction process in the ramp generator.

Fig.8 shows the FFT results obtained by applying a sinusoidal input through the proposed ROIC. The FFT was measured under the conditions of 16,384 samples at a sampling rate of 62.5 kHz. The input signal had a peak-to-peak voltage of 1.18 V, and the measurement was performed with a low-frequency input signal of 156.4 Hz. This frequency was selected to account for the slow response characteristics of the gas sensor, ensuring that the system's behavior under these conditions could be accurately captured.

Fig.9 shows the chip microphotograph of the proposed ROIC. The chip was fabricated using the TSMC 180nm standard CMOS process. The total chip area is 4.2 mm² (2.8 mm × 1.5 mm), with the core IP occupying approximately 0.32 mm² (0.62 mm × 0.52 mm). The core blocks of the proposed ROIC include the ramp generator, digital DDR counter, comparator, as well as peripheral blocks. Table I presents the performance measurement results of the proposed ROIC.

V. CONCLUSION

In this paper, we have presented the design and implementation of a ROIC optimized for gas sensor applications. The proposed ROIC achieves a power consumption of 1.31 mW, with a 1.2V input range and a conversion rate of 62.5 kHz, delivering a performance of 9.41 bits of ENOB. Additionally, it achieves a FoM of 30.81 pJ/step. The proposed ROIC provides a robust solution for high-precision gas sensing systems. The results demonstrate its potential to significantly enhance the performance of sensor-based applications. Future work will focus on further optimizing the design for integration with a wider range of gas sensors and expanding the system′s functionality for broader applications in environmental monitoring and industrial safety.

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