Peripheral System for Tunneling Field-Effect Transistor-Based Content Addressable Memory

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***Abstract* – Content Addressable Memory (CAM) is a crucial component in modern computing systems, offering rapid parallel search capabilities that significantly enhance data retrieval efficiency. CAM is increasingly employed in advanced applications such as Deep Neural Networks (DNNs), particularly within Memory-Augmented Neural Networks (MANNs) that utilize one-shot learning techniques. While CAMs can be implemented using various memory technologies such as SRAM, RRAM, and Ferroelectric FETs, this paper specifically addresses the challenges and solutions associated with TFET-based CAMs. We propose a system for TFET-based CAMs composed of four critical components: the Search Data Register, the Matchline Sense Amplifier, the High Voltage Switch, and the Priority Encoder. The functionality and performance of the proposed peripheral circuits have been validated through experimental testing, demonstrating the practical feasibility of integrating TFET-based CAMs into advanced circuit systems.**

***Keywords* - Content Addressable Memory (CAM), Search Data Register, Matchline Sense Amplifier, High Voltage Switch, Priority Encoder**

I. INTRODUCTION

Content Addressable Memory (CAM) represents a pivotal advancement in memory technology, distinguished by its capability to perform rapid parallel searches. Unlike conventional memory systems that require address-based data retrieval, CAM enables data to be accessed based on its content, significantly enhancing search speed and efficiency (Fig. 1). This feature is particularly beneficial in applications that demand quick and frequent data access, making CAM a vital component in various modern computing systems.

CAM operates by comparing input data against stored entries in parallel, yielding the address of the matching data or indicating the absence of a match. This parallel comparison process reduces search times from linear to constant time, offering substantial performance improvements in scenarios requiring high-speed data retrieval.

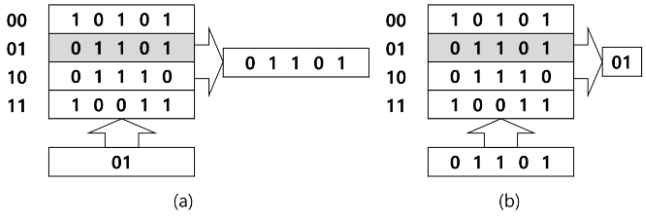

Fig. 1. Data flow of (a) traditional memory and (b) content addressable memory.

Recent advancements in CAM technology have expanded its applicability beyond traditional uses. CAM is integrated into advanced applications such as Deep Neural Network (DNN), where they play a critical role in Memory-Augmented Neural Network (MANN)[1]. MANN leverages CAM's rapid search capabilities to facilitate one-shot learning-an approach that enables models to learn from a single example and generalize to new tasks with minimal data.

A CAM can be constructed using a variety of memory devices, including Static Random-Access Memory (SRAM)[2], Resistive Random-Access Memory (RRAM), and Ferroelectric Field-Effect Transistor (FeFET)[1]. However, in this paper, we focus on Tunneling Field-Effect Transistor (TFET)[3] based CAM.

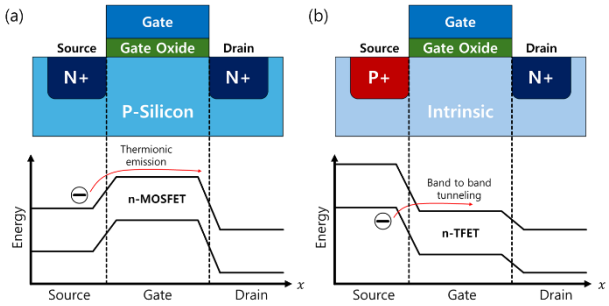

Fig. 2. (a) MOSFET structure and energy band diagram, and (b) TFET structure and energy band diagram.

Unlike MOSFET, the TFET has different doping between the source and drain, and its body is composed of an intrinsic

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semiconductor rather than p-silicon. In MOSFETs, current flows through thermionic emission as electrons move across the junction. In contrast, TFETs rely on band-to-band tunneling for current flow. TFETs have advantages for low-power operation due to their high on/off ratio and low off current. Fig. 2 shows the structure and energy band diagram of MOSFET and TFET.

The proposed system includes four critical components: the Search Data Register, the Matchline Sense Amplifier (MLSA), the High Voltage (HVS), and the Priority Encoder. Through experimental validation, we demonstrate the functionality and performance of the proposed system, illustrating its feasibility for integration with advanced CAM systems.

II. PERIPHERAL SYSTEM

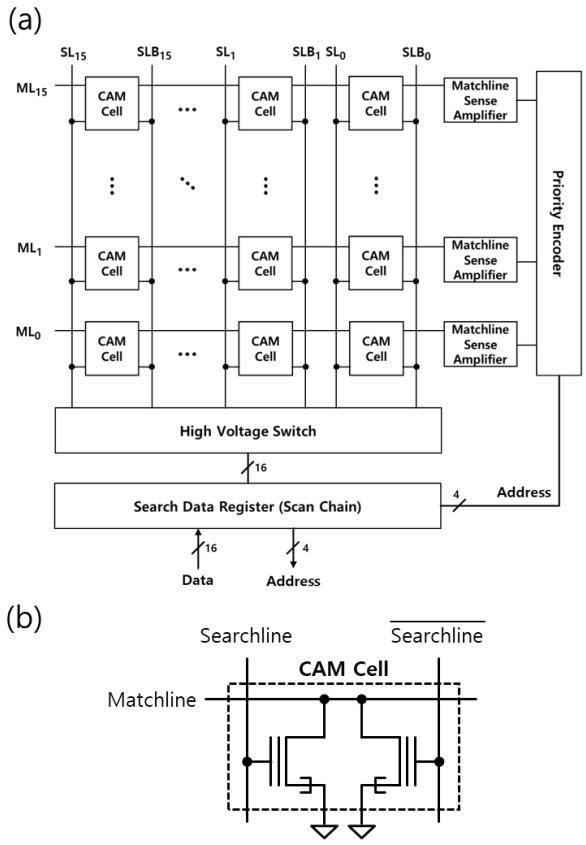
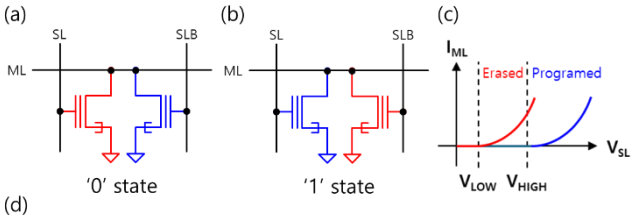


Fig. 3. (a) Overall structure of the CAM peripheral system and (b) TFET-based CAM cell.

The overall structure of the proposed CAM peripheral system is illustrated in Fig. 3(a). It comprises circuits specifically designed to drive a TFET-based CAM array, targeting a 16x16 array configuration.

A single CAM cell consists of a pair of memory elements with opposite states. Fig. 3(b) illustrates a TFET-based CAM cell, where each gate is designated as Searchline (SL) and $\overline{\text{Searchline}}$ (SLB), and the drains are connected, referred to as the Matchline (ML).

A digital search data is input into the SL via a scan chain-based Search Data Register. This digital data is subsequently converted into an analog voltage appropriate for the TFET[3] by the HVS, and then fed into the CAM cells. Once the search is complete, the output from the MLSA is sent to the Priority Encoder, which returns the address of the ML that indicates a match.



(d)

State	Input		Output
	SL	SLB	ML
'0' state	**'0'**	'1'	**Match** (High)
	'1'	'0'	Mismatch (Low)
'1' state	'0'	'1'	Mismatch (Low)
	'1'	'0'	**Match** (High)

CAM Cell	
Read Bias	
'1'-V_{SL}	7V
'0'-V_{SL}	0V
V_{ML_PCH}	1V
I_{ML_Mis}	~100nA

Fig. 4. (a) TFET CAM cell '0' state, (b) TFET CAM cell '1' state, (c) States of TFET CAM cell and (d) CAM operation conditions and read biases.

For CAM operation, the two memory elements that make up the CAM cell must hold opposite states. Fig. 4(a) and (b) show the states of the memory elements according to the CAM cell state, while (c) illustrates the approximate characteristics of the memory elements. When the SL element is programmed, it represents the '1' state, and when erased, it represents the '0' state. CAM operation for each state is shown in (d), along with the drive voltage and current levels of the TFET-based CAM cell targeted in this study.

A. Search Data Register

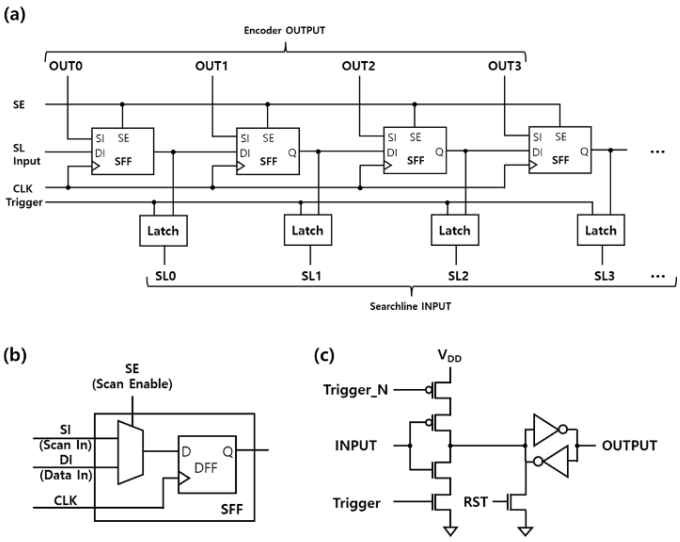


Fig. 5. Schematic design of (a) scan chain-based Search Data Register, (b) Unit scan flip-flop, and (c) Scan latch.

Fig. 5. Shows the schematic design of the Search Data Register. It consists of unit scan flip-flops (SFFs), each composed of a 2x1 multiplexer and a D flip-flop, connected in sequence. Additionally, a trigger latch is included to

enable parallel input to the SL. The design targets a 16x16 CAM array, with 16 SFFs connected to the system. By utilizing the scan chain as the Search Data Register, both the input to the CAM array and the output of the results can be driven by a single circuit. Except for the four outputs from the encoder, the remaining SI signals are used to generate a regular pattern for verifying the scan chain operation.

B. Matchline Sense Amplifier

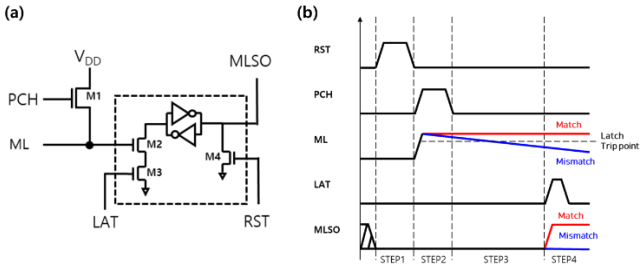


Fig. 6. (a) Schematic design and (b) Timing diagram of the MLSA.

The schematic design and timing diagram of the MLSA are shown in Fig. 6.[3] It includes NMOSs for precharge (M1), reset (M4), and a trigger signal (LAT) (M3), with ML input through M2. After precharge, the voltage level of ML is sensed during the searching, either maintaining or changing the state of the latch. Because the drain read voltage of the TFET (ML) is lower than V_{DD} (1.8V) ($\cong V_{DD} - V_{THN}$), instead of using a PMOS transistor for precharge, an NMOS transistor is utilized.

C. High Voltage Switch

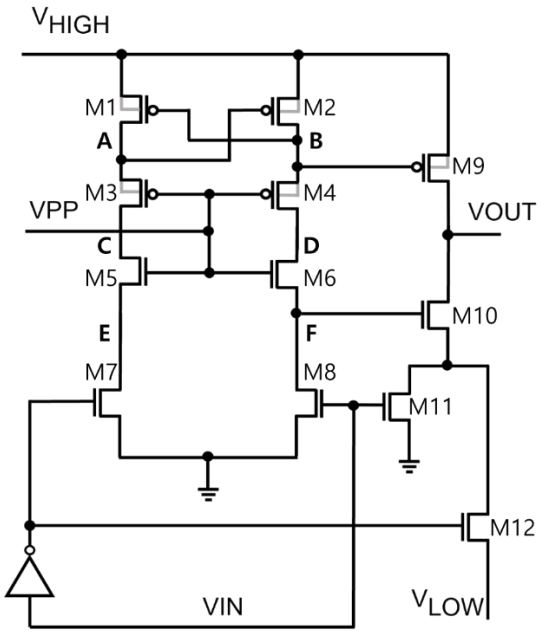
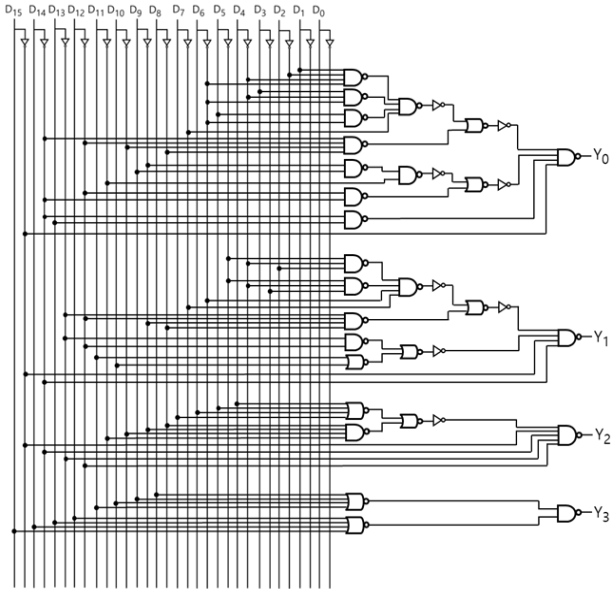


Fig. 7. Schematic design of the HVS.

Given that the gate read voltage for the TFET is about 7~8V, a HVS was designed, as shown in Fig. 7.[4] This switch converts the digital search data input through the Search Data Register into an appropriate analog signal. Additionally, to represent a digital '0', a V_{LOW} driving stage was added to utilize a TFET gate read voltage in the range of 0~1V.

When VIN is high, M8 turns on, pulling the F node down to GND. The resulting large V_{GS} of M6 will turn on M6, pulling the D node down to GND as well. M6 and VPP keep the B node below VPP + $|V_{THP}|$ because, if the B node exceeds VPP + $|V_{THP}|$, M4 will turn on, pulling the B node down to VPP + $|V_{THP}|$. Then, M1 turns on and pulls the A node up to V_{HIGH}, further pulling the B node down to VPP. Consequently, M9 turns on and makes V_{OUT} to V_{HIGH}. Conversely, when VIN is low, M12 and M10 turn on to produce an output of V_{LOW}.

D. Priority Encoder



$$Y0 = \sum (\bar{D}_{14}\bar{D}_{12}\bar{D}_{10}\bar{D}_8(\bar{D}_6\bar{D}_4\bar{D}_2\bar{D}_1 + \bar{D}_6\bar{D}_4D_3 + \bar{D}_6D_5 + D_7) + \bar{D}_{14}\bar{D}_{12}(\bar{D}_{10}D_9 + D_{11}) + \bar{D}_{14}D_{13} + D_{15})$$

$$Y1 = \sum (\bar{D}_{13}\bar{D}_{12}\bar{D}_9\bar{D}_8(\bar{D}_5\bar{D}_4D_2 + \bar{D}_5\bar{D}_4D_3 + D_7 + D_6) + \bar{D}_{13}\bar{D}_{12}(D_{11} + D_{10}) + D_{15} + D_{14})$$

$$Y2 = \sum (\bar{D}_{11}\bar{D}_{10}\bar{D}_9\bar{D}_8(D_7 + D_6 + D_5 + D_4) + D_{15} + D_{14} + D_{13} + D_{12})$$

$$Y3 = \sum (D_{15} + D_{14} + D_{13} + D_{12} + D_{11} + D_{10} + D_9 + D_8)$$

Fig. 8. Gate level schematic design of the Priority Encoder and the Boolean expressions.

Although a standard encoder could be used, we opted for a Priority Encoder to minimize the possibility of errors, as commonly employed in Ternary-CAM (TCAM) systems.[5] Unlike a standard encoder, the Priority Encoder outputs only the address of the Most Significant Bit (MSB) while treating the other bits as don't care. The Boolean expressions were derived from the truth table, and the design was implemented at the gate level based on these expressions (Fig. 8.).

III. MEASUREMENT

A. Measurement setup

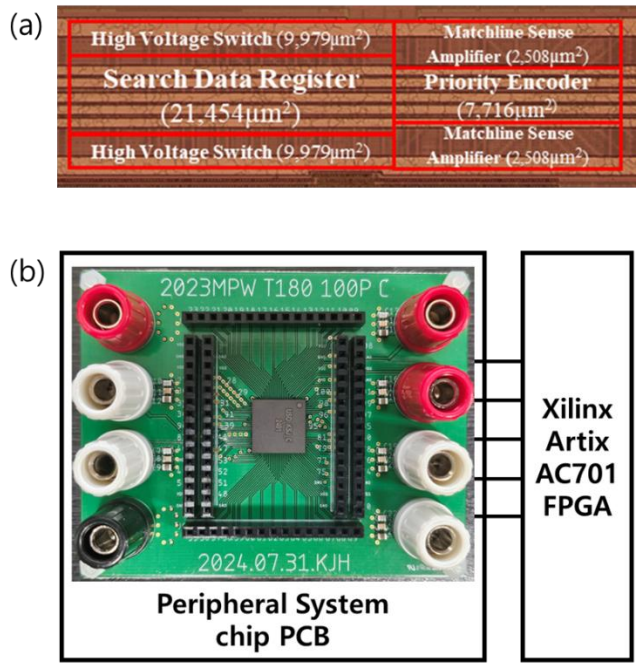


Fig. 9. (a) Microscopic image of fabricated chip, and (b) Block diagram of the measurement system.

The proposed peripheral system was designed and fabricated using a full-custom approach, utilizing the TSMC 180nm CMOS logic process (Fig. 9. (a)). Also, we designed a PCB board and used the Artix AC701 FPGA from Xilinx for measurements (Fig. 9. (b)).

B. Results

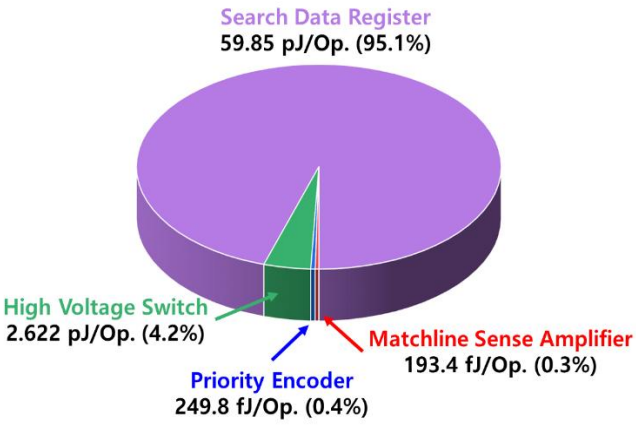


Fig. 10. Energy Breakdown of the peripheral system.

Fig. 10. shows the energy breakdown obtained from simulations. A single search operation achieves an energy efficiency of 62.92 pJ. It can also be observed that the analog circuits, the HVS and MLSA, consume comparatively less energy than the Search Data Register.

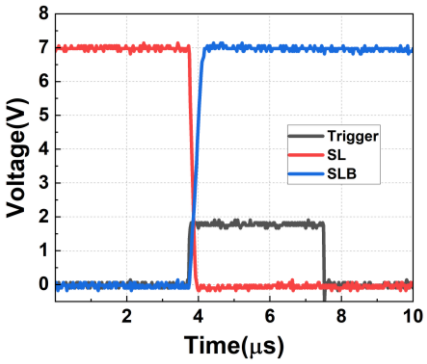
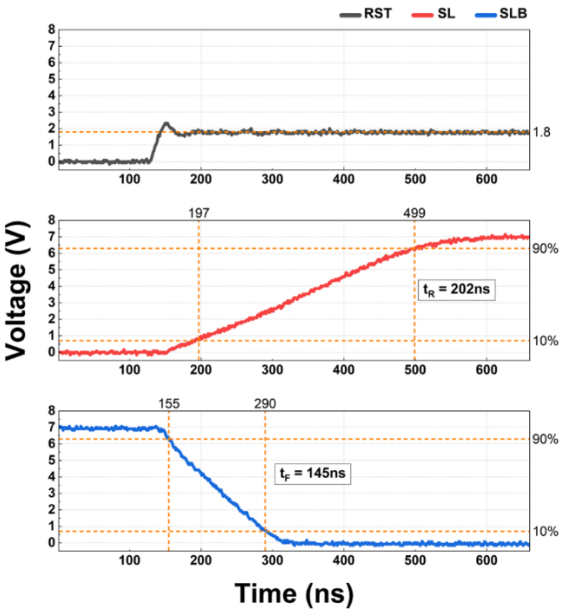
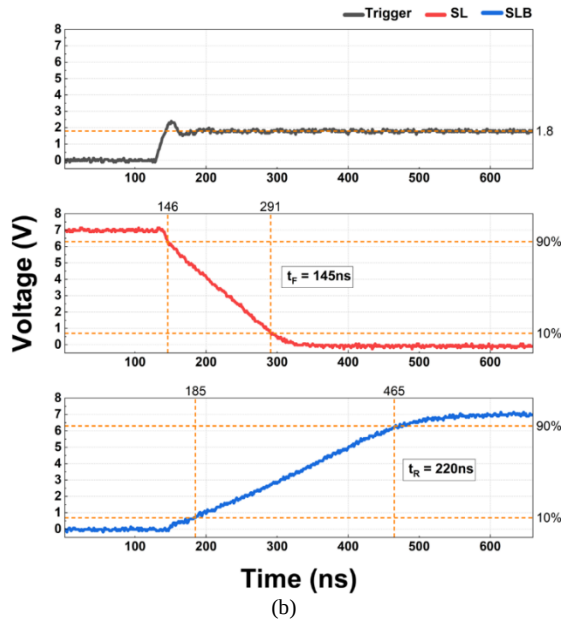


Fig. 11. Transition Results of SL and SLB Through the Search Data Register and the HVS.



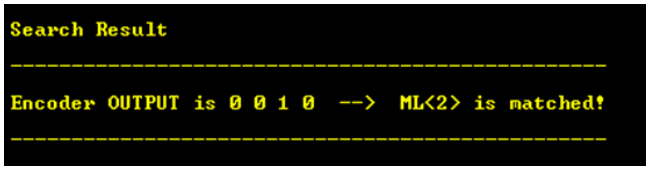
(a)



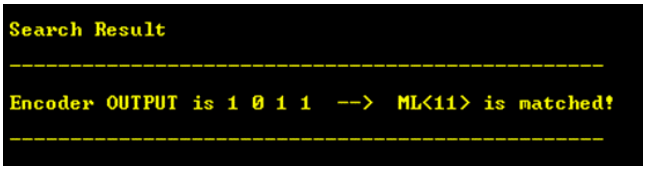
(b)

Fig. 12. Rising and falling time of SL and SLB. (a) SL rising, SLB falling and (b) SL falling, SLB rising.

Fig. 11. shows the results of converting digital data input through the Search Data Register into analog signals via the HVS. The figures illustrate that a digital '1' is output as 7V, while a digital '0' is output as 0V. And the rising and falling time of SL and SLB are shown in Fig. 12. The rising time is approximately 210 ns, while the falling time is 145 ns. This indicates that high-speed operation is feasible even with TFET-based CAM that uses relatively high voltages.



(a)



(b)

(c)

Fig. 13. Operation Results of the MLSA and Priority Encoder Under Various Conditions: (a) ML<2> at V_{DD}, (b) ML<11> and ML<2> at V_{DD}, and (c) ML<15>, ML<11> and ML<2> at V_{DD}.

Before connecting the TFET CAM array, we verified the operation of the MLSA and Priority Encoder by applying V_{DD} to specific MLs and operating the circuit. We confirmed that not only when V_{DD} is applied to ML<2> alone but also when V_{DD} is simultaneously applied to ML<11> and even ML<15>, the address corresponding to the MSB is output (Fig. 13).

IV. CONCLUSION

In this work, we proposed and implemented a peripheral system for TFET-based Content Addressable Memory (CAM). The system was designed and fabricated using a full-custom approach with the TSMC 180nm CMOS logic process, specifically targeting a 16x16 TFET CAM array. The experimental results validate the functionality and practical feasibility of the proposed peripheral circuits, confirming their potential for integration into advanced circuit systems that utilize TFET-based CAM. In the future, we plan to combine the fabricated TFET CAM with the peripheral system to validate high-speed CAM operation.

ACKNOWLEDGMENT

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