Design Study of a 240-GHz Amplifier Frequency Doubler Chain Based on SiGe BiCMOS Technology

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***Abstract* – In this work, an amplifier-frequency doubler chain has been designed in a 130-nm SiGe BiCMOS HBT technology operating around 240 GHz. The amplifier-frequency doubler chain is composed of a 240-GHz frequency doubler integrated with a 120-GHz driver amplifier. The differential driver amplifier exhibited a saturated output power of 10.8 dBm at the center frequency and a peak gain of 13.2 dB with a 23-GHz (109-132 GHz) 3-dB bandwidth. As for the frequency doubler, which is based on a push-push configuration, a saturated output power of 3.3 dBm and a peak output power of 1.8 dBm with a 3-dB bandwidth of 142 GHz (116-258 GHz) were obtained. After integration, the amplifier-frequency doubler chain showed a saturated output power of 3.3 dBm with a 3-dB bandwidth of 48 GHz (210-258 GHz). The total DC power consumption was 103.6 mW.**

***Keywords*—Frequency multiplier, Driver amplifier, 130-nm SiGe BiCMOS HBT**

I. INTRODUCTION

The terahertz (THz) band generally refers to the frequency range from 0.1 THz to 10 THz. This range corresponds to wavelengths of 0.33 to 3.3 mm, which partially includes the sub-mm wave band with wavelengths shorter than 1 mm. Owing to the higher frequency compared to the conventionally employed bands, a much wider bandwidth can be provided and the data transmission speed can also be increased. Traditionally, the application fields of the THz band, which is located between the optics and electronics territories, have been driven by the optics-based technologies such as spectroscopy and imaging. Recently, however, with the rapid advancement of electronic device performances, research efforts using electronic device technology such as communication and radar systems have also become active [1].

On-chip oscillators and frequency multipliers are widely considered effective approaches to implement semiconductor chip-based THz signal sources. THz on-chip oscillators can operate without an external signal source, but they may suffer from a narrow bandwidth and amplitude variation as in the case of voltage-controlled oscillators. On the other hand, frequency multipliers can achieve a wider operation bandwidth with a relatively low amplitude variation, while the output power may be limited when operated alone [2]. To alleviate the low output power performance, a driver amplifier is widely adopted to be integrated with frequency multipliers [3, 4]. The purpose of this work is to design a frequency doubler with an integrated driver amplifier operating around 240 GHz with a high output power and a wide operation bandwidth, crucial performances for terahertz systems [5, 6].

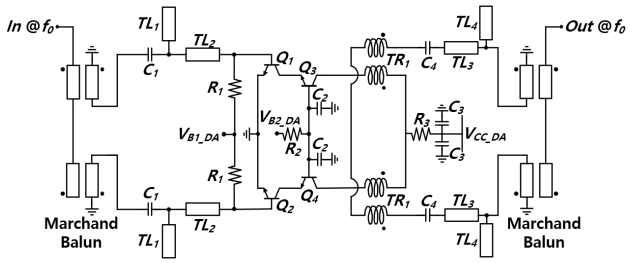

Fig. 1. Schematic of the 120-GHz driver amplifier.

A 120-GHz differential cascode driver amplifier (DA) is integrated with a balanced 240-GHz frequency doubler (FD). The FD needs sufficiently high input power to obtain a reasonable power level at the output of the circuit. The 120-GHz DA precedes the FD to provide a sufficient input power to the FD. The circuits were designed in a 130-nm SiGe HBT process from IHP (Innovations for High Performance Microelectronics). f_T and f_{max} of the devices provided in this process are 300 and 500 GHz, respectively, making them suitable for terahertz system designs [7].

The paper is structured as follows. In Section II and III, the designs of the 120-GHz DA and 240-GHz FD are presented with simulated results, respectively. The integrated 240-GHz amplifier-frequency-doubler chain (AFDC) is described in Section IV. Finally, the conclusion is presented in Section V.

II. 120-GHZ DRIVER AMPLIFIER

The proposed DA shown in Fig. 1 employs the differential cascode topology for relatively high conversion gain and

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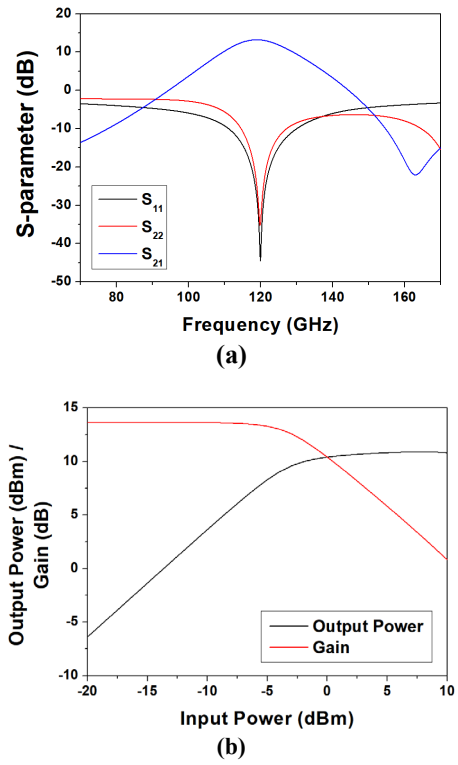

Fig. 2. Simulated (a) *S*-parameters and (b) output power and conversion gain against input power at 120 GHz input frequency of the 120-GHz driver amplifier.

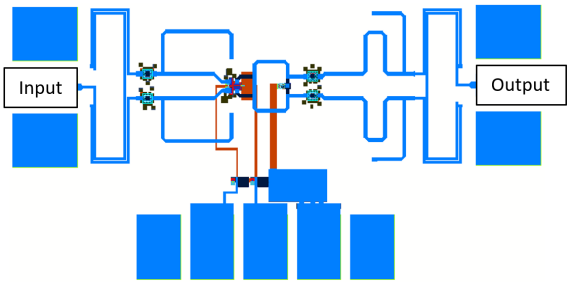

Fig. 3. Layout of the 120-GHz driver amplifier.

output power. A mid-size transistor ($A_E = 6 \times (0.07 \times 0.9\ \mu m^2)$) has been selected to achieve the required gain level. A coupled-line-based Marchand balun is inserted at the front to convert the single-ended 50-Ω input to the differential 100-Ω. This is followed by the input matching circuit composed of transmission lines TL_1 and TL_2 and DC block capacitors C_1 (75 fF). A pair of RF-block resistors R_1 is adopted for current biasing. The balanced cascode stage, composed of Q_1 - Q_4, serves as the main amplifying stage of the DA. The base transmission line section of transistors Q_3 and Q_4 can cause parasitic inductance together with R_2, another RF choke, which may trigger a stability issue of the amplifier. To resonate out the parasitic inductance, a pair of capacitors C_2 is inserted, which also provides DC voltage biasing to the base of the transistors. For output matching, a transformer TR_1 is adopted for a compact design. Because the DA is designed to be integrated with the following FD, TR_1 forms a conjugate match to the FD input along with TL_3, TL_4 and C_4. To verify the performance of the individual DA with a single-ended output, another Marchand balun is inserted at the output stage of the circuit.

Fig. 2 shows simulated *S*-parameters, output power and the gain of the DA with input power variation based on a full-wave EM (electromagnetic) simulator by ADS (Advanced Design System) Momentum. The peak S_{21} is 13.2 dB at 119 GHz and the 3-dB bandwidth is 23 GHz (109-132 GHz). The gain and output power were simulated by the harmonic balance technique. The saturated output power is 10.8 dBm. The layout of the DA is shown in Fig. 3. The chip size is $984 \times 560\ \mu m^2$ including the RF and DC pads.

III. 240-GHZ FREQUENCY DOUBLER

An individual 240-GHz FD was also designed for a separate performance verification. The schematic of the FD

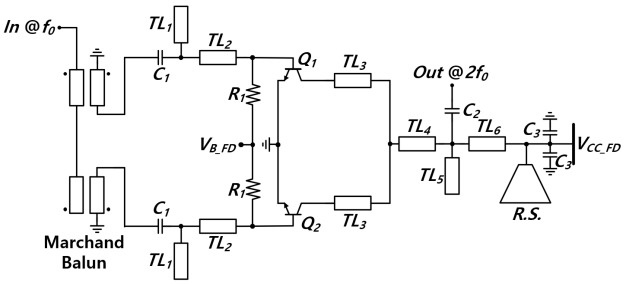

Fig. 4. Schematic of the 240-GHz frequency doubler.

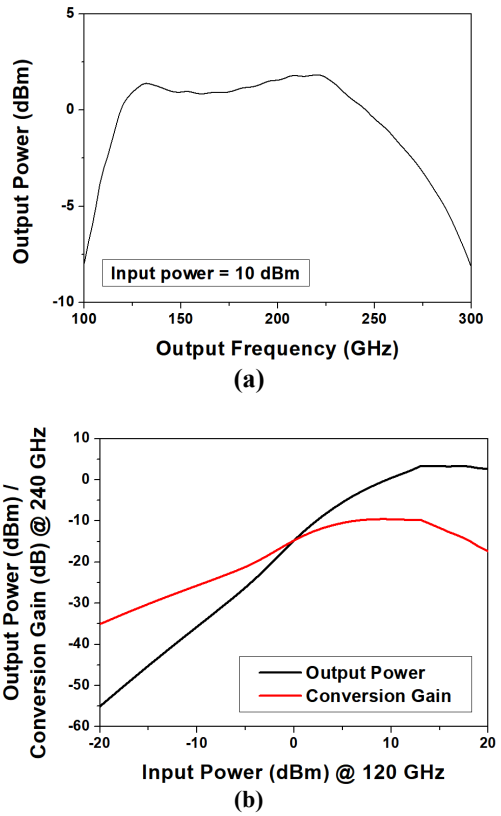

Fig. 5. Simulated output power against (a) output frequency and (b) input power and conversion gain at 120 GHz input frequency of the 240-GHz frequency doubler.

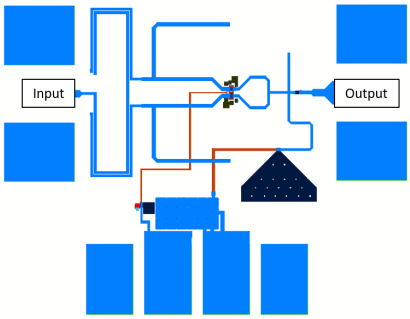

Fig. 6. Layout of the 240-GHz frequency doubler.

is shown in Fig. 4. For the FD, a balanced structure is employed, which is a popular choice for FDs due to its effective odd-harmonic suppression and the high conversion gain [8]. Relatively small-sized transistors ($A_E = 4 \times (0.07 \times 0.9\ \mu m^2)$) have been selected for the circuit, which showed a large second harmonic current. To verify the individual FD in the single-ended configuration, a Marchand balun is inserted at the front of the circuit, similar to the case for the DA. The input matching network, which is composed of transmission lines TL_1, TL_2, a pair of DC-block capacitors C_1, and RF-block resistors R_1, is also similar to the one used for the DA as described in the previous section. The core of the FD is formed by the differential pair composed of Q_1 and Q_2, which generate a second harmonic signal due to the inherent nonlinearity at the tied collector output through transmission lines TL_3 based on the push-push operation. Transmission lines TL_4 and TL_5 are employed for output matching. The collector bias line TL_6 is designed as a quarter-wavelength at the second harmonic frequency $2f_0$, providing a virtual open for $2f_0$ to maximize the output signal level. The radial stub (*R.S.*) with a high Q-factor and self-resonant frequency is employed to reduce the effect of the parasitic inductance arising from the DC bias line as well as bypass capacitor C_3 [9]. It will also help provide a stable AC ground for a wide frequency range along with the bypass capacitors C3, which are large in size, leading to a rather low self-resonant frequency.

The simulation results of the FD are presented in Fig. 5. A peak output power of 1.8 dBm at 220 GHz was achieved with a 3-dB bandwidth of 142 GHz (116-258 GHz). These results were achieved with a 10-dBm input power, which is the saturated output power of the DA. The saturated output power of the FD is 3.3 dBm with a 13-dBm input power at 240 GHz (center frequency). The peak conversion gain is -9.6 dB with a 9-dBm input power. Fig. 6 shows the layout of the FD. The chip size is $690 \times 570\ \mu m^2$ including the pads.

IV. 240-GHZ AMPLIFIER-FREQUENCY DOUBLER CHAIN

The two circuits described so far, DA and FD, are integrated together to form an AFDC, the schematic of which is shown in Fig. 7. As mentioned earlier, the DA provides optimal input power to the FD thus improving the conversion gain of the integrated chain. The DA and FD are combined through a pair of transformers TR_1, which are designed to serve as the interstage matching between the two circuits. Compared to the case with stub matching with transmission lines, the size of the matching network could be further reduced by employing the transformer scheme. It also obviates the need for additional DC bias block capacitors, another factor that leads to a compact design. The transformers are based on a stacked structure built on the thick metal levels. To provide the desired conjugate matching, the line width and the radius of the inner turn of the transformer are optimized for the matching point. To avoid interstage feedback between the DA and FD, a series resistor R_3 is inserted at the injection point of the collector bias V_{CC_DA} [10].

The integrated circuit was simulated and the results are shown in Fig. 8. The peak output power is 3.2 dBm at 240 GHz, which is an apparent increase compared to the case with the individual FD. The 3-dB bandwidth is 48 GHz (210-258 GHz), which is obviously limited by the amplifier bandwidth doubled by the FD. The linearity plot obtained at the center frequency of 240 GHz (Fig. 8(b)) exhibits a saturated output power of 3.2 dBm with a 0-dBm input power and peak conversion gain of 6.7 dB with a -7-dBm input power. Fig. 8(c) shows the output spectrum at an input frequency of 120 GHz. It is obvious from the plot that the

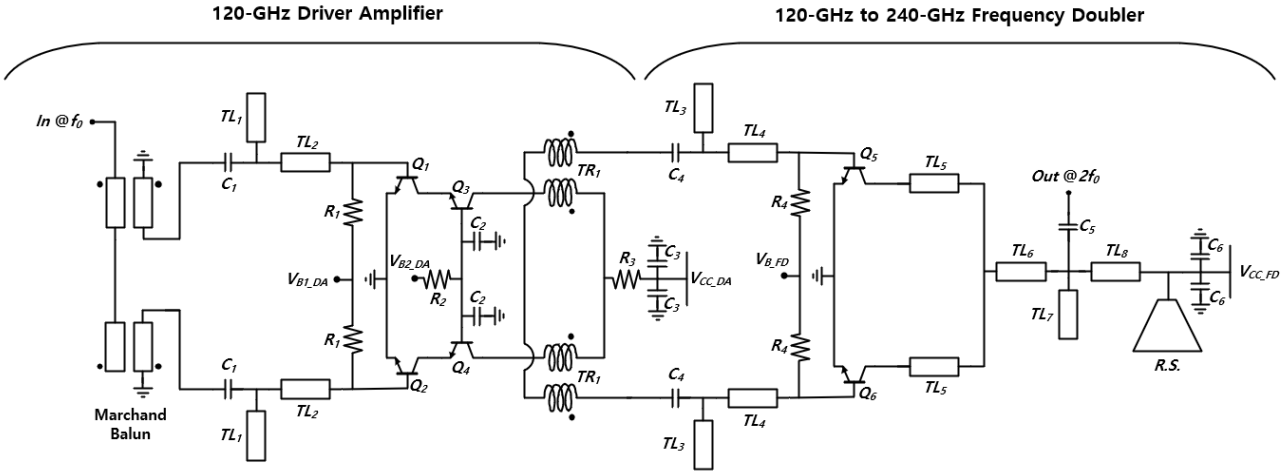

Fig. 7. Schematic of the 240-GHz amplifier-frequency doubler chain.

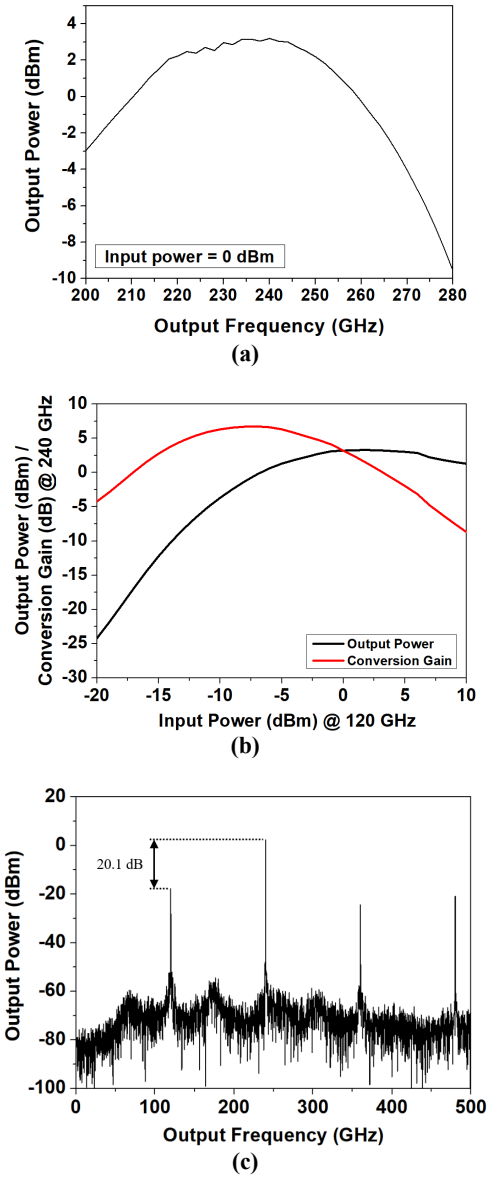

Fig. 8. Simulated output power against (a) output frequency and (b) input power and conversion gain at 120 GHz input frequency (c) harmonic suppression at 120 GHz input frequency of the 240-GHz amplifier-frequency doubler chain.

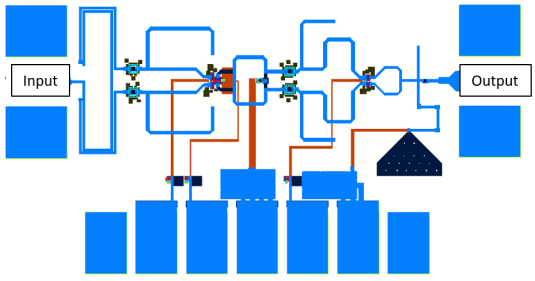

Fig. 9. Layout of the 240-GHz amplifier-frequency doubler chain.

unwanted harmonics are sufficiently suppressed, with a fundamental frequency suppression of 20.1 dBc. The saturated output power of the AFDC is similar to that of the FD as shown in Fig. 5 (b). However, it is not trivial to routinely access an input power level of over 10 dBm from external sources. This is the main reason why the DA with an output power level of 10 dBm at a more feasible 0-dBm input power is integrated with the FD to form an AFDC. Fig. 9 shows the layout of AFDC. The size of the layout is $1016 \times 576\ \mu m^2$.

V. CONCLUSION

A 240-GHz AFDC, which comprises a frequency doubler integrated with a driver amplifier, has been designed based on 130-nm SiGe BiCMOS technology. The simulated results of the circuit exhibited an output power of 3.2 dBm at 240 GHz and a 3-dB bandwidth of 48 GHz. The individual frequency doubler and driver amplifier were also designed and characterized. The designed AFDC will be well suited for various applications including communication and radar systems that require high power and wide bandwidth near 240 GHz.

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