A 28-GHz Down-Converter for 5G Direct-Conversion Receivers in 65-nm CMOS Technology

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***Abstract* – A millimeter-wave down-converter employing an on-chip balun transformer with improved common-mode rejection ratio is presented for 5G direct-conversion receiver. The down-converter consists of a down-conversion mixer and local-oscillator (LO) buffer. The down-converter was implemented in a 65-nm CMOS process. It consumes a power of 13.7 mW from a 1-V supply voltage. It shows a gain greater than 11 dB, a noise figure of approximately 9 dB and a third-order output intercept point higher than 13 dBm when LO input power is -10 dBm in the frequency ranges from 26.5 GHz to 29.5 GHz.**

***Keywords*—5G, CMOS, Down-converter, Millimeter-wave**

I. INTRODUCTION

Due to the explosive increase in the amount of data that must be processed in a wireless environment, 5G wireless communication standards have been developed and the 5G wireless communication system is currently in use [1]. In the 5G wireless communication system, millimeter-wave (mmWave) band transceivers have been used to process Gbps data rates [2].

Dual-conversion single-quadrature architecture and direct-conversion architecture have been used to implement 5G mmWave wireless communication systems [2], [3]. In general, the receiver linearity of these architectures is affected by the linearity of the down-conversion mixer in the receiver front end. Millimeter wave band circuit design requires a CMOS process with a cutoff frequency (f_T) of several hundred GHz, which has been made by continuous scaling-down of the gate length in CMOS technology. Recent scaling-down CMOS process uses a power supply voltage of 1V or less. Therefore, it is necessary to design a down-conversion mixer without linearity deterioration in an environment where the power supply voltage is approximately 1V. The mixer circuit that can operate at low supply voltage uses an on-chip balun transformer-based circuit topology [4]. In bands below several GHz, the common-mode rejection ratio (CMRR) performance of the on-chip balun transformer is good because the parasitic capacitance effect of the on-chip balun transformer is small.

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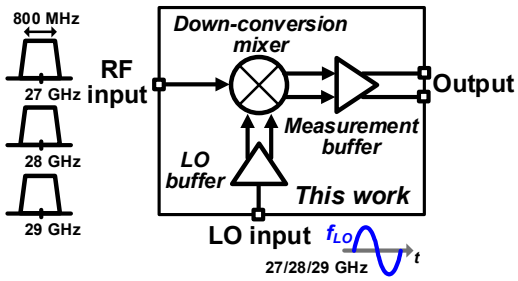


Fig. 1. Block diagram of the presented 28-GHz down-converter composed of a down-conversion mixer and LO buffer.

However, the parasitic capacitance degrades the CMRR performance of the on-chip balun transformer in the millimeter wave band [5], [6]. The mmWave on-chip balun transformer can deteriorate the balancing characteristics of the differential output signal that is converted from the single-ended input signal by the transformer. This may cause RF performance such as conversion-gain degradation of the down-conversion mixer [5], [6].

In this paper, a 28-GHz down-converter employing an on-chip balun transformer with improved CMRR and DC offset adjusting load is proposed for 5G direct-conversion receiver. The down-converter has been implemented in a 65 nm CMOS process and has high output-referred third-order intermodulation point (OIP3) at 1-V supply voltage.

II. CIRCUIT DESIGN

Fig. 1 presents the block diagram of the presented 28 GHz down-converter composed of a down-conversion mixer and an LO buffer for 5G direct conversion receivers. The RF input and LO input have single-ended 50-Ω terminations. The RF input frequencies are 27, 28, and 29 GHz with a 3-dB bandwidth of 800 MHz, respectively. A measurement buffer is used for measurement of baseband output signal. An LO buffer is employed in order to drive the switching pair of the down-conversion mixer using the LO input signal with the input power of less than −5 dBm. The LO buffer is composed of a two-stage common source (CS) amplifier.

Fig. 2 shows a simplified schematic of the proposed down-conversion mixer. The down-conversion mixer consists of a transconductance stage and a switching stage. In the conventional Gilbert mixer, the switching stage is stacked on the transconductance stage, making it difficult to achieve high linearity performance without using linearity

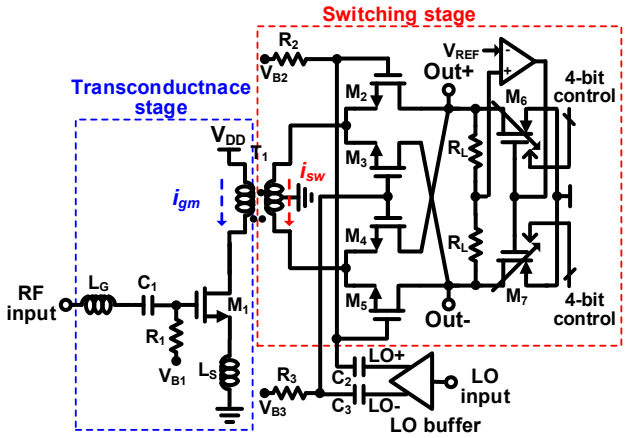


Fig. 2. Simplified schematic of the proposed down-conversion mixer.

improvement techniques when the supply voltage is low. In this design, because a low supply voltage of 1-V is used, a topology in which the transconductance stage and switching stage are magnetically coupled with an on-chip transformer T_1 is used instead of a stacked topology. Typically, the more current the transconductance stage consumes in the mmWave band, the better RF performance of the down-conversion mixer can be achieved. On the other hand, the more current switching stage consumes, the less efficient the switching operation is, thus deteriorating the performance of the down-conversion mixer. Therefore, since DC current value of the transconductance stage required to optimize the performance of the down-conversion mixer operating in the mmWave band are different from that of switching stage, the overall mixer performance can be optimized by adjusting DC current of each stage in the presented down-conversion mixer of Fig. 2. The transconductance stage is a CS amplifier. The input impedance $Z_{in}(j\omega)$ of the transconductance stage can be approximately expressed as

$$Z_{in}(\omega) \approx \frac{g_{m1}L_s}{C_{gs}} + j\omega\left[L_g + L_s - \frac{1}{\omega^2}\left(\frac{1}{C_{gs}} + \frac{1}{C_1}\right)\right] \quad (1)$$

where C_{gs} and g_{m1} are the gate-to-source capacitance and transconductance of transistor M_1, respectively [7]. To satisfy 50-Ω input impedance matching at the RF operating frequency, the design parameters in (1) are set so that the $Z_{in}(\omega)$ value is 50-Ω.

An on-chip balun transformer T_1 was used at the output load of the transconductance stage to convert the single-ended drain current of the transistor M_1 into a differential input current signal of the double-balanced switching stage. The on-chip balun transformer with high CMRR can have good balancing characteristics of differential input current signal of the double-balanced switching stage. The parasitic capacitance between the primary winding and secondary winding of the on-chip transformer and the impedance Z_R caused by the routed line from one node of the primary winding to the VDD PAD can deteriorate the balancing characteristics of the differential signal in mmWave frequency band [5], [6], [8]. Fig. 3(a) shows the simplified

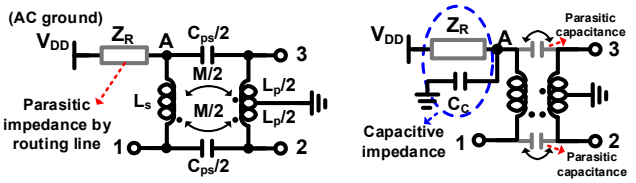


Fig. 3. (a) Simplified equivalent circuit of on-chip balun transformer T_1 for CMRR analysis, (b) on-chip balun transformer T_1 with capacitance compensation for balancing characteristics improvement. L_p and L_s represent the self-inductances of the primary and secondary windings, respectively, M is the mutual inductance, and C_{ps} is the parasitic capacitance between the primary and secondary windings [8].

equivalent circuit of the on-chip balun transformer T_1 for CMRR analysis. The condition for maximizing the CMRR of the on-chip balun transformer T_1 was derived in [5], [8] as follows:

$$Z_R = -j\omega \frac{\omega^2 \frac{L_p}{2}\frac{C_{ps}}{2}\left(\frac{L_pL_s - M}{2}\right) + \frac{L_pL_s}{2}}{L_p\left\{\omega^2 \frac{C_{ps}}{2}\left(\frac{L_p + L_s - 2M}{2}\right) - 1\right\}}. \quad (2)$$

Since the impedance due to a routed line is usually inductive, additional capacitance C_C is added to node A on one side of the primary winding to satisfy Equation (2), as shown in Fig. 3(b).

The relationship between the output current i_{gm} of the transconductance stage and the input current i_{sw} of the switching stage is linear as follows;

$$i_{sw} \simeq G_c i_{gm} \quad (3)$$

where G_c is current gain [4]. Since the down-conversion mixer of Fig. 2 has a structure in which the transconductance stage and switching stage are not stacked and the current from the transconductance stage is transferred to the switching stage without distortion, the down-conversion mixer can be expected to have high linearity.

The linearity and switching loss of a down-conversion mixer depend on the amplitude of the LO signal. Typically, mmWave down-conversion mixers require large LO drive signals to obtain high linearity and improve conversion gain of the down-conversion mixer [9]. The LO buffer consisting of a two-stage CS amplifier is employed to drive the switching stage of the down-conversion mixer.

The performance of a direct-conversion receiver can be affected by output DC offset of a down-conversion mixer [3]. A DC offset voltage may occur at the output of the down-conversion mixer in Fig. 2 due to mismatch between switching transistors, load transistors, or load resistors. To compensate for the dc offset in the differential output, the size of the output load transistor of the down-conversion mixer was adjusted through 4-bit control, allowing the DC voltage in the range of 0 to 15 mV to be varied at one output of the mixer.

Two single-ended source followers with high linearity

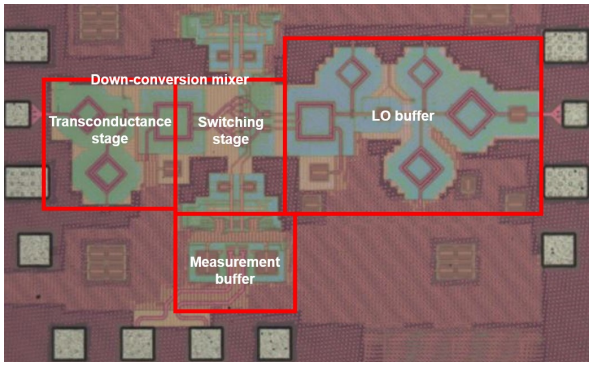
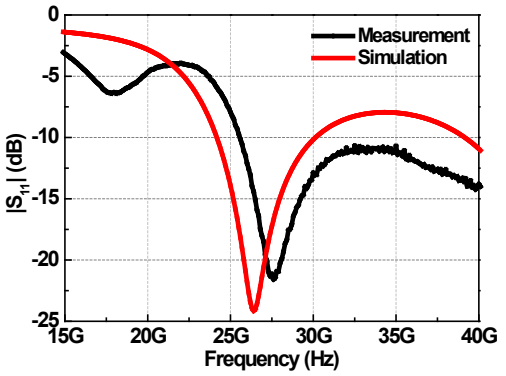
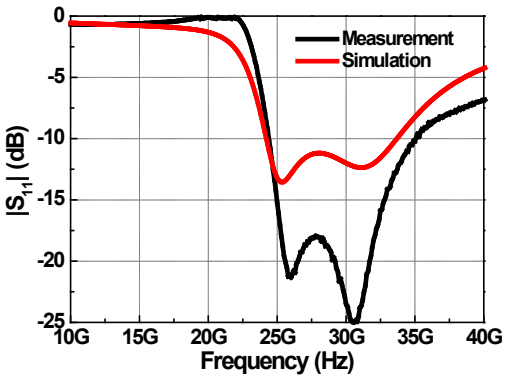


Fig. 4. Chip microphotograph of the proposed RF down-converter.



(a)



(b)

Fig. 5. Measured $|S_{11}|$ at (a) RF input port, (b) LO input port.

characteristics, which do not affect the linearity performance of the down-conversion mixer, are used as measurement buffer. The output impedance of each source follower was designed to be 50 ohm.

III. EXPERIMENTAL RESULTS

The mmWave down-converter composed of a down-conversion mixer and an LO buffer was implemented in a 65-nm CMOS process. Fig. 4 shows the chip microphotograph of the presented mmWave down-converter. The silicon area of the down-conversion mixer and LO buffer excluding PADs is 0.715 mm × 0.55 mm. The mmWave down-converter was measured by on-wafer probing after attaching the down-converter chip to an external printed circuit board. The power consumption of the mmWave down-conversion mixer and LO buffer is 13.7 mW and 10.1 mW from a 1-V supply voltage, respectively. For the measurement, −10 dBm of LO power was applied to the LO input of the LO buffer.

Fig. 5 shows the measured return loss at the RF input, and LO input of the mmWave down-converter, respectively. The return loss at the RF input and LO input is less than −10 dB from 26.5 to 29.5 GHz.

Fig. 6 shows the single-ended output spectrum of the down-converter when the two-tone RF input frequencies

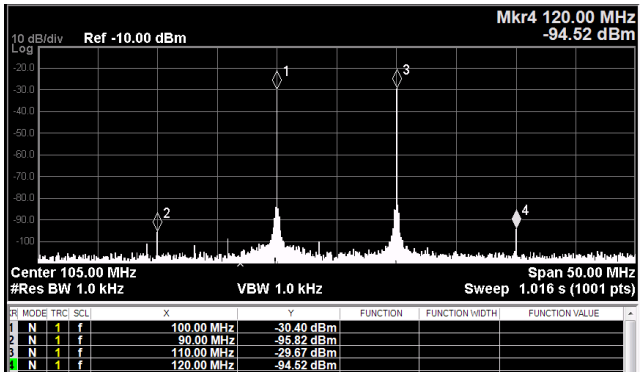


Fig. 6. Measured single-ended output spectrum of the proposed RF down-conversion mixer. RF Input power was set to -30 dBm and total loss by cables and probe tips is approximately 1.5 dB.

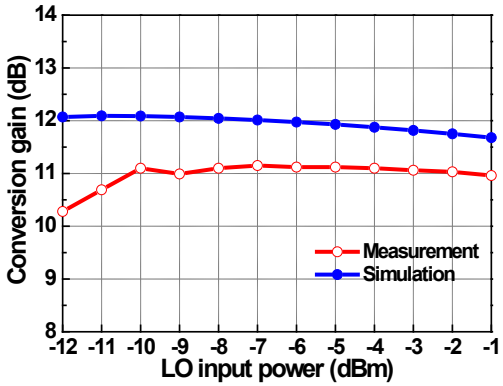


Fig. 7. Measured gain versus LO input power.

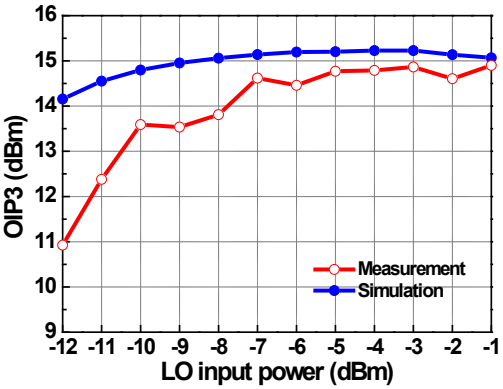


Fig. 8. Measured OIP3 versus LO input power.

Table I MEASUREMENT SUMMARY AND COMPARISON OF PERFORMANCE

	[10]	[11]	[12]	This work
Operating frequency (GHz)	31	26.5-29.5	26-39	26.5-29.5
Conversion gain (dB)	3.4	10.1	3.87 (28 GHz)	11
OIP3 (dBm)	21.4	19.3	4.54 (28 GHz)	13.5
Linearization technique ?	Yes	Yes	No	No
NF (dB)	9.5	9.9	13.62 (28 GHz)	8.9
LO input power (dBm)	3	-7*	5	-10*
Power consumption (P_{DC}) (mW)	21.2 @ 1.5 V (Mixer)	11 / 21* @ 1 V (Mixer + LO buffer)	9.75 @ 1 V (Mixer)	13.7 / 23.8* (Mixer + LO buffer)
Technology	45 nm SOI CMOS	65 nm CMOS	65 nm CMOS	65 nm CMOS
Area	0.8 mm^2	0.18 / 0.28* mm^2	0.4 mm^2	0.2 / 0.39* mm^2
FOM[a] [11]	25.5 @ 31 GHz	24.7 / 12.9* @ 28 GHz	0.37 @ 28 GHz	6.77/3.9* @ 28 GHz

*Value including LO buffer, OIP3 = Gain + IIP3,

[a] $$FOM(dB) = \frac{Gain[abs] \cdot IIP3[mW]}{P_{DC}[mW]} \cdot \frac{1}{(NF-1)[abs]} \cdot f[GHz]$$

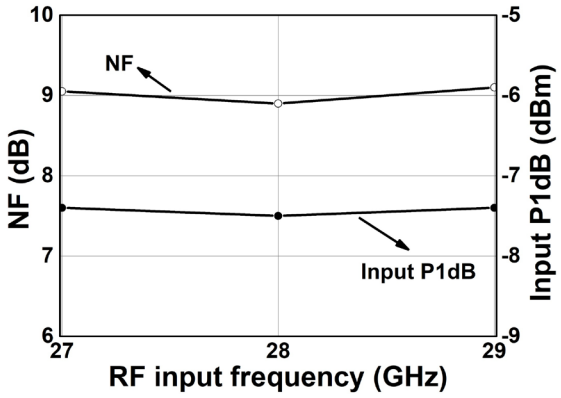


Fig. 9. Measured NF and input P1dB.

are 28.1 GHz and 28.11 GHz, respectively, the LO input frequency is 28 GHz, and the RF input power is set to −30 dBm. Because the total loss due to cables and probe tips in the measurement is 1.5 dB and the gain of the measurement buffer is −4 dB, the conversion gain of the down-conversion mixer is approximately 11.1 dB at the differential output of the down-conversion mixer.

As shown in Fig. 7 and Fig. 8, the measured conversion gain of the down-conversion mixer is larger than 11 dB and the measured OIP3 is more than 13 dBm when the LO input power is over −10 dBm. Fig. 9 shows the measured NF and input P1dB.

Table I summarizes and compares the measured results of the proposed down-converter with those of other published mmWave down-converter. Because the proposed down-conversion mixer does not employ linearization techniques, it has lower linearity than the previously published mmWave down-conversion mixers which employ linearization techniques [10], [11]. As a result, the down-conversion mixer has a lower figure of merit (FOM) but comparable performances while using smaller LO input power compared with the previously published mmWave down-conversion mixers with linearization techniques. On the other hand, it has a higher FOM compared to the down-conversion mixer [12] in which the linearization technique is not applied.

IV. CONCLUSION

A 28-GHz down-converter was implemented and proposed for 5G mmWave mobile applications. The proposed down-converter shows an excellent figure of merit (FOM) compared with previously published down-converters. Therefore, the down-converter could be suitable for 5G mmWave direct-conversion receivers.

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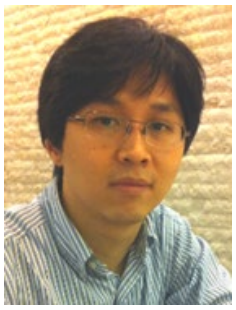

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