Fully Integrated Ka-Band Power Amplifier with Parallel Power Combiner using Single-Winding Transformer

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***Abstract* – This paper presents a Ka-band linear CMOS power amplifier (PA) with a parallel power combiner using single-winding transformer to increase the output power with low loss in 65nm CMOS technology for fifth generation (5G) applications. Two differential cascode unit PAs are combined with the proposed parallel power combiner as a current combining topology. Compared with the conventional transformer power combining techniques, the proposed parallel power combiner can offer high output power with a compact die area.**

Upon simulation with a 28 GHz continuous-wave signal, the proposed PA achieves a saturated output power (P_{SAT}) of 25.0 dBm, output 1-dB compression power ($P_{O,1dB}$) of 22.6 dBm, and peak power added efficiency (PAE) of 34.7%, respectively. A power gain of 28.1 dB is achieved with a 3 dB bandwidth of 5 GHz. This PA achieves one of the highest figures-of-merit (FOM) among the recently reported 5G millimeter-wave (mm-wave) PAs in CMOS.

***Keywords*—CMOS, high efficiency, high output power, Ka-band, Power amplifier (PA), Power combiner, 5G, 65nm**

I. INTRODUCTION

The realization of 5G wireless communication in the mm-wave band has become a highly significant to meet the increasing data traffic demands. Thus, integrated mm-wave transceivers have been studied intensively [1]-[21], [25]-[27]. In the meantime, the transceivers using CMOS are the current trend for high-level integration. Among all the building blocks of on-chip CMOS mm-wave transceivers, the PA is the most critical block. Due to parasitic effect, lossy substrate and low breakdown voltage in advanced CMOS technology, delivering high output power and maintaining high efficiency are challenging in the design of CMOS PA.

Several power combining techniques such as device stacking [1]-[3], on-chip transmission line power combining [4]-[8], and transformer power combining [9]-[21] have been used to achieve high output power in mm-wave band.

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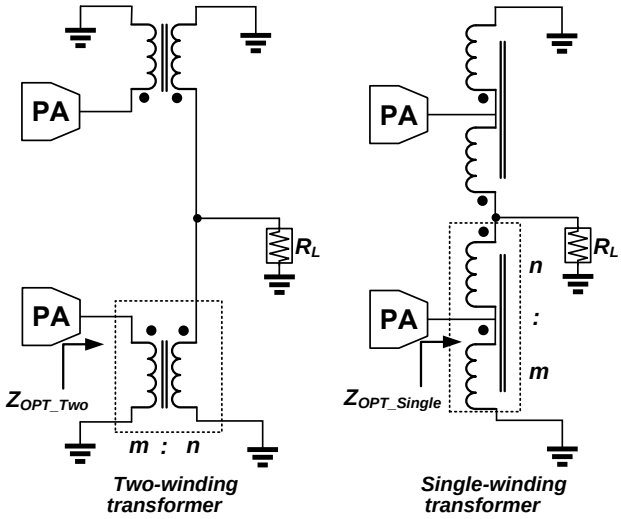


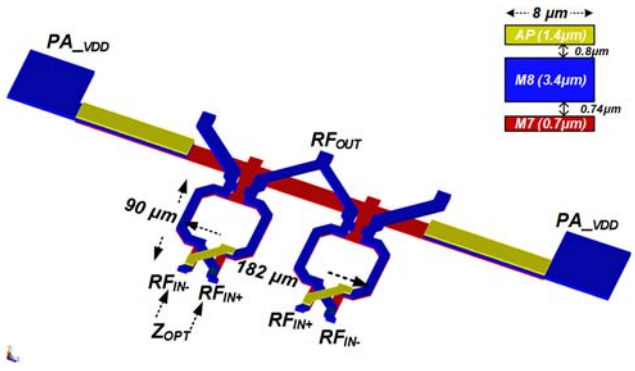
Fig. 1. Structure of parallel power combiner based on an ideal model of a two-winding transformer, (b) proposed parallel power combiner based on an ideal model of a single-winding transformer

Especially, transformer power combining techniques based on a two-winding transformer have been widely used for mm-wave CMOS PAs because they provide impedance transformation function along with the advantages of low loss and compact area.

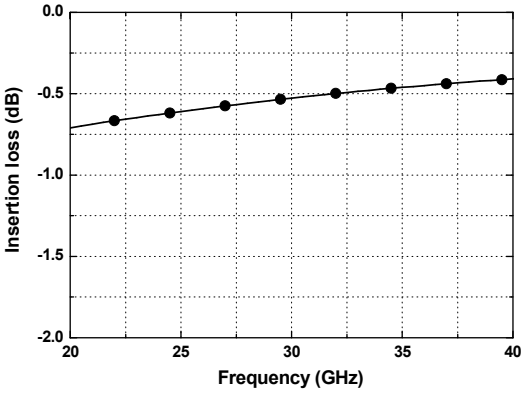
To obtain high output power of PA in the mm-wave band, a parallel power combining topology based on a two-winding transformer has been widely used, as shown in Fig.1(a) [16]-[21]. In this configuration, multiple of two-winding transformers can be combined through parallel connection. In comparison with a series power combining topology [11]-[15], this topology is superior in obtaining symmetric structures and low imbalance performances between paths [20], [27].

In general, to generate high output power in PA using an on-chip transformer, low input impedance of a transformer is required, because the output power generated from a device is inversely proportional to the input impedance of the transformer. However, the parallel combiner increases the input impedance; thus, it is difficult to generate high output power with a parallel power combiner using a two-winding transformer, as shown in Fig.1(a).

An autotransformer, a single-winding transformer, has also been introduced for on-chip PA designs [22]-[24].



(a)



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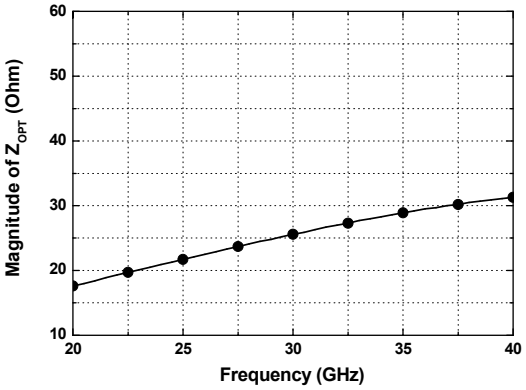


(c)

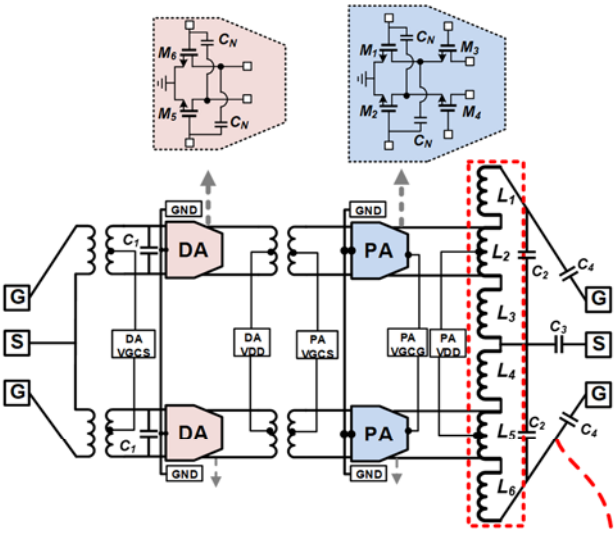
Fig. 2. (a) Exemplary layout of the proposed power combining network. Simulated (b) insertion loss of proposed power combiner, (c) magnitude of Z_{OPT}.

Compared to a typical two-winding transformer, the input impedance of a single-winding transformer is lower if the same number of turns is used for the primary and secondary windings in both single-winding and two-winding transformers. In addition, a single-winding transformer can provide the advantage of passive efficiency with compact size and impedance transformation ratio [22]-[24]. Thus, it is a suitable candidate for the design of PAs using on-chip transformer to achieve high output power with high efficiency and compact size.

In this paper, we propose a fully integrated Ka-band linear two-stage CMOS PA with a compact parallel power combiner using single-winding transformer to obtain high output power with high efficiency and compact design.

The detailed structure of the proposed power combiner

	Driver stage (DA)	Power stage (PA)
Supply VDD (V)	1.2	2.4
Gate width (μm)/ Gate length (nm)	M_5- M_6 83.2 / 65	M_1 - M_4 128 / 65
C_N (fF)	69	98
C_1, C_2, C_3, C_4 (fF)	208, 1054, 950, 250	



Proposed power combiner

Winding diameter (μm) / Width (μm)	77 / 8
size (μm²)	182x 90

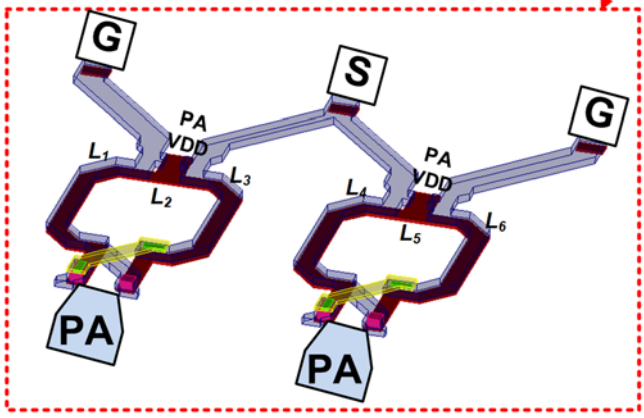


Fig. 3. Detailed schematic of the two-stage CMOS PA with parallel power combiner.

and the circuit architectures of this PA are presented in Section II. Section III presents the post-layout simulation results of the proposed PA and a comparison of the proposed PA with the recent state-of-the-art Ka-band CMOS PAs. Finally, Section IV presents the conclusions of this work.

II. DESIGN OF THE PROPOSED POWER COMBINER AND KA-BAND POWER AMPLIFIER DESIGN

A. Proposed parallel power combiner using single-winding transformer

Fig.1 shows the equivalent ideal model for a parallel power combiner based on two types of transformers, for the single-ended case. As shown in Fig.1, the parallel power combiner with a two-winding transformer comprises two two-winding transformers arranged in a parallel configuration, while the proposed parallel power combiner

consists of two single-winding transformers, similar to the previous configuration. For structure of parallel power combiner using two-winding transformer, a unit amplifier, a PA, is connected to each primary winding of two-winding transformer, while a PA in proposed power combiner is connected to part of each winding in single-winding transformer, resulting in the configuration of autotransformer.

For the two cases of parallel power combiner, each input impedance can be derived using equations (1) and (2) from the equivalent ideal model.

$$Z_{OPT\_Two} = \left(\frac{n}{m}\right)^2 \times R_L \times 2 \quad (1)$$

$$Z_{OPT\_Single} = \left(\frac{m}{m+n}\right)^2 \times R_L \times 2 \quad (2)$$

In equations (1) and (2), m is the number of primary winding turns, n is the number of secondary winding turns, and R_L is typically 50 Ω. For mm-wave applications, one turn is typically used for the primary and secondary windings to achieve high quality factor. Thus, with the condition of one turn for each of the primary and secondary windings ($m = n = 1$) in Fig.1, the calculated input impedance of the two-winding, Z_{OPT_Two}, is 100 Ω, while Z_{OPT_Single} is 25 Ω. Because a single-winding transformer provides lower impedance than a two-winding transformer when the same number of turns is applied, the proposed output combiner can generate high output power with low number of turns. In addition, the primary winding of the autotransformer includes as part of the secondary one, resulting in reducing the total series resistance [22]-[24]. Consequently, the PA implemented using the proposed parallel power combiner can achieve high output power and low insertion loss with compact size.

Fig.2(a) shows an exemplary layout of the proposed parallel power combiner. The size of the layout is 182 μm × 90 μm to achieve optimum power matching impedance. For the design of the parallel power combiner, a top metal layer is mainly used, and the inter-connections in the proposed combiner are implemented with the second top metal layer. Considering the DC current density on the metal, the metal width of the transformer is set as 8 μm. In addition, for the arrangement of the proposed combiner, vertical geometry is adopted to achieve a high magnetic coupling factor. In the initial design stage, to evaluate the performance of the proposed power combiner, electromagnetic (EM) simulations using both the HFSS and ADS momentum were performed. Because the EM simulated results from ADS momentum show a good agreement with those from HFSS at targeted frequency range, in the final design stage, EM simulations using ADS momentum were used considering the design complexity and iteration time. The simulated coupling factor is approximately 0.83 for the power combiner. The simulated insertion loss of proposed power combiner is −0.5 dB at 28 GHz, as shown in Fig.2(b). In other words, it proves that the proposed power combiner has low insertion loss with small die area. Fig.2(c) shows that the simulated magnitude of the load impedance, looking from PA, is approximately 25 Ω. Therefore, CMOS PAs using the proposed power combiner can achieve high power with high efficiency performance and compact die area.

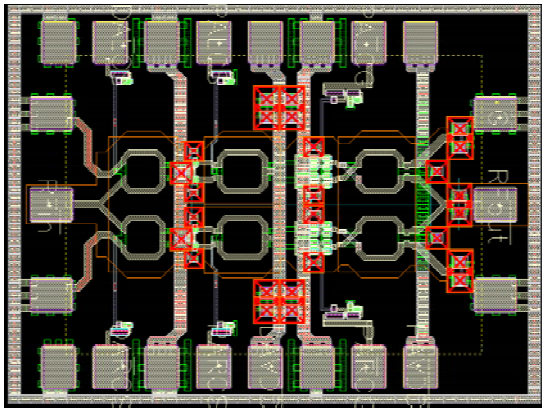


Fig. 4. Layout photograph of the proposed CMOS PA.

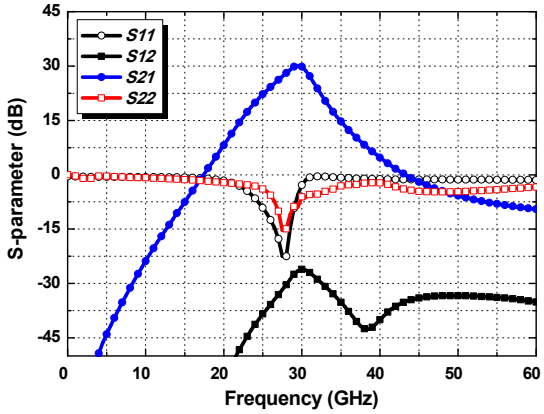


Fig.5. Simulated small-signal S-parameters.

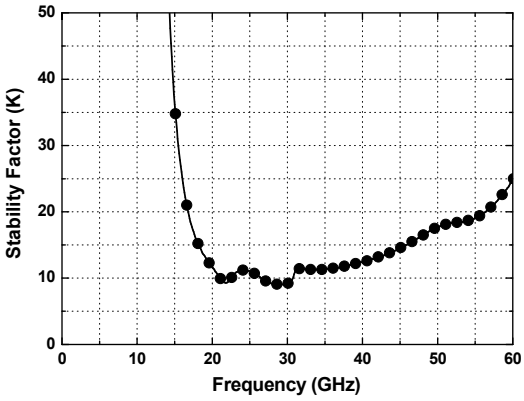


Fig.6. Simulated stability factor.

B. Design of Ka-band CMOS PA

The detailed schematic diagram of the proposed CMOS PA with the proposed parallel power combiner is presented in Fig. 3. Furthermore, detailed design parameters are included in Fig. 3. For the PA design, a two-stage configuration (driver and power stages) is used to provide sufficient gain and power driving. For the design of the DA stage, the DA is adopted using a common-source (CS) topology with size (W/L = 2 × 83.2 μm /65 nm) for M_5 and M_6, which are biased at DA_VDD = 1.2 V. The PA is realized using a cascode topology with identical size (W/L = 2 × 128 μm /65 nm) for M_1, M_2, M_3, and M_4, which are biased at

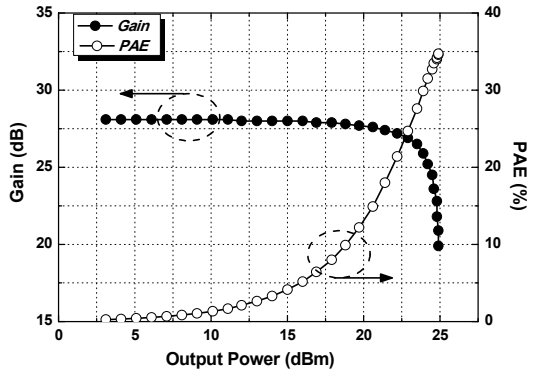


Fig.7. Simulated output power, gain and PAE versus input power at 28GHz.

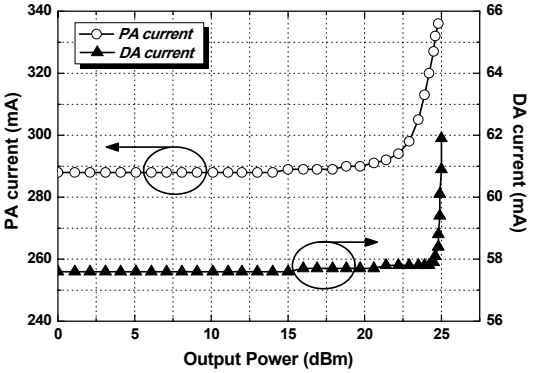


Fig.8. Simulated current consumption of PA and DA stages.

PA_VDD = 2.4 V.

In addition, the PA utilizes neutralized capacitors (C_N) to improve the power gain, reverse isolation, and stability. A two-way transformer-based series power divider is designed to generate two differential signals, two inter-stage transformers are used to drive the four unit PAs. The supply currents are fed into the differential unit.

III. POST-LAYOUT SIMULATION RESULTS

The proposed PA with a parallel power combiner is designed using a 65 nm CMOS technology. Fig.4 shows the photograph of the designed PA. The dimensions of the whole chip are 0.85 × 0.6 mm^2, including the DC supply pad and input and output matching networks; additional off-chip matching elements are not required. The core integration area of the proposed PA is 0.18 mm^2.

In the simulation, the pads and bond wires are included for obtaining high-accuracy simulation results. The simulated S-parameter results are shown in Fig.5. The simulated small-signal gain is 28.6 dB, input return loss is −22.5 dB, and the output return loss is −14.9dB. The simulated stability factor is greater than unity, from 10 MHz to 60 GHz, as plotted in Fig.6. Fig.7 shows the simulated large-signal continuous-wave power-sweep results at 28 GHz. With a 2.4 V supply, the PA achieves a power gain of 28.1 dB, P_{SAT} of 25 dBm, peak PAE of 34.7 %, and $P_{O,1dB}$ of 22.6 dB. This PAE includes the power consumption of the input and driver stages. Fig.7. shows the current consumptions of the PA and DA stages versus the output power at 28 GHz. Initially, the quiescent currents in the PA and DA stages are 288 mA and 58 mA, respectively.The power dissipation is 760 mW under quiescent conditions. As the output power increases, the current consumptions of the PA and DA stage are 342 mA and 60 mA, respectively, in the saturated output power region, as plotted in Fig.8.

TABLE I. Comparison of the proposed PA with the recently reported Ka-band CMOS PAs.

	This Work[#]	[25]	[26]	[27]
Tech. (nm)	65	28	90	65
Freq. (GHz)	28	28	28	28
Gain (dB)	28.1	13.6	16.3	15.6
P_{SAT} (dBm)	25	19.8	26	15.5
$P_{O,1dB}$ (dBm)	22.6	18.6	23.2	13.9
PAE (%)	34.7	13.3	34.1	41
Core area (mm^2)	0.18	0.28	0.24**	0.24
*P.D (mW/mm^2)	1755	341	1658	147
+FOM	97.4	78.7	86.5	76.1

[#]Simulated results
*Power density is denoted as P.D. (P_{SAT}/chip area)
**Estimated core area from the reported photograph.
+FOM=P_{SAT}[dBm]+Gain[dB]+20log(f_c[GHz]) +10log (PAE_{max} [%]).

Table 1 presents a comparison of the performance of this work and that of the recently reported 5G CMOS PAs in the mm-wave band. Thanks to the proposed power combiner and careful design of the PA, the output power, PAE, and power gain are maintained high, resulting in the highest FOM of 97.4 among that of the reported CMOS PAs.

IV. CONCLUSION

In this paper, a Ka-band CMOS PA with a parallel power combiner using 65-nm CMOS technology is proposed. With the proposed power combiner, the PA achieves high output power with high efficiency performance and compact die area. The proposed PA achieves P_{SAT} of 25 dBm in a 0.18 mm^2 core area, resulting in outstanding level 1755 mW/mm^2 Ka-band CMOS PAs. power density at 28 GHz. In comparison with the other recently reported mm-wave CMOS PAs, the proposed PA shows high power and the best overall performance. Thanks to compact size and high efficiency of proposed power combiner, it is a suitable solution for implementations in Ka-band applications.

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