# A 6.4Gbit/s 3-Tap High-Speed IO FIR Driver with LMS Adaptation Algorithm in 65nm CMOS

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***Abstract* - A 6.4Gb/s IO transceiver including an adaptive finite impulse response (FIR) filter has been implemented with 65nm technology. The FIR tap coefficients are adapted using sign-sign least mean square (LMS) algorithm. Eye-openings are improved under time varying conditions by creating a diverse channel loss environment. The transceiver consumes 64mW/lane at 1.2V supply and the chip size is 0.506 $mm^2$. The measured vertical eye-opening has been improved from 152.4mV/1.06V to 356.6mV/699.3mV after pre-emphasis and the measured horizontal eye-opening is 0.484 UI at $10^{-9}$ BER.**

***Keywords*—High-speed IO, SerDes, Transceiver, FIR, driver, variable gain amplifier, sign-sign LMS**

## I. INTRODUCTION

The demand for chip-to-chip communication, which involves processing large amounts of data, has been increasing every year. However, the improvement of physical IO bandwidth and increase of the number of pads are synchronized, leading to a higher data transfer rate per pin. Channel bandwidth limitations caused by parasitic components and integrated circuit packaging result in a non-flat frequency response and inter-symbol interference (ISI). Interference in these transmission channels can be compensated by applying the inverse effect of the interference through the IO transceiver to receive a high-fidelity signal.

One way to apply the inverse effect is applying pre-emphasis to the signal at the transmission end to compensate for the lossy channel. The FIR equalization has the advantage of using a pre-existing driver and eliminating both the pre-cursor and post-cursor. Additionally, as a discrete system, ISI can be removed without noise amplification and clock information can be used in advance. Traditionally the FIR filter tap has been implemented in an adaptation system [1]-[3]. The adaptive FIR filter was designed using the sign-sign LMS algorithm to simplify hardware implementation compared to the LMS algorithm. Pre-emphasis using an adaptive FIR filter has the ability to overcome channel bandwidth limitations by adapting to unknown and uncharacterized channels. In order to design with low power, a half rate structure was used, and it was designed as a voltage mode segmented driver. Voltage mode driver has the advantage of reducing power consumption by 1/4 compared to the current mode logic (CML) type [4], [5]. It aims to create an on-chip memory channel.

The paper is organized as follows. Section II deals with the IO transceiver architecture. Section III covers the sign-sign LMS used for adaptation and describes hardware implementation. Section IV presents the results of experiments. Section V shows the conclusion.

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## II. CIRCUIT

Fig. 1 shows the block diagram of the presented IO transceiver. The Pattern generator (PG) creates a 400 Mb/s pseudo-random bit stream (PRBS) of 16 lanes. The 16:2 Serializer serializes the PG signals into a 3.2Gb/s EVEN/ODD signal in 2 lanes. The tap generator receives the EVEN/ODD signal and generates pre/main/post tap signals respectively. The half-rate FIR driver receives EVEN/ODD tap signals and creates a pre-emphasized 6.4Gb/s non-return-to-zero (NRZ) signal. The signal transmitted from the transmitter (Tx) travels through the channel and suffers from ISI. In the receiver (Rx), a variable gain amplifier (VGA) amplifies the signal with an appropriate gain. The slicer determines 0/1 data from the 6.4 Gb/s NRZ signal through half-rate sampling. The 5:40 deserializer parallelizes 3.2Gb/s of EVEN/ODD data into 16 lanes of 400 Mb/s signals. Receiver signals deliver new tap coefficients to the FIR driver through adaptation logic. It also delivers early/late edge info to CDR (Clock and Data Recovery). The Pattern checker (PC) detects whether the received data is received in the correct pattern and then calculates the bit error rate (BER).

### *A. Transmitter(Tx)*

A serializer is required to convert low speed parallel data into high-speed serial data as shown in Fig. 2(a). The basic structure of the serializer consists of a mux box using D flip-flop and latch as presented in Fig. 2(c). Data is transmitted once per half cycle of the clock, resulting in two data transmissions per clock cycle. Therefore, the first even data goes out at the falling edge of the 180 degree clock (180 degree phase shift clock) and the first odd data goes out at

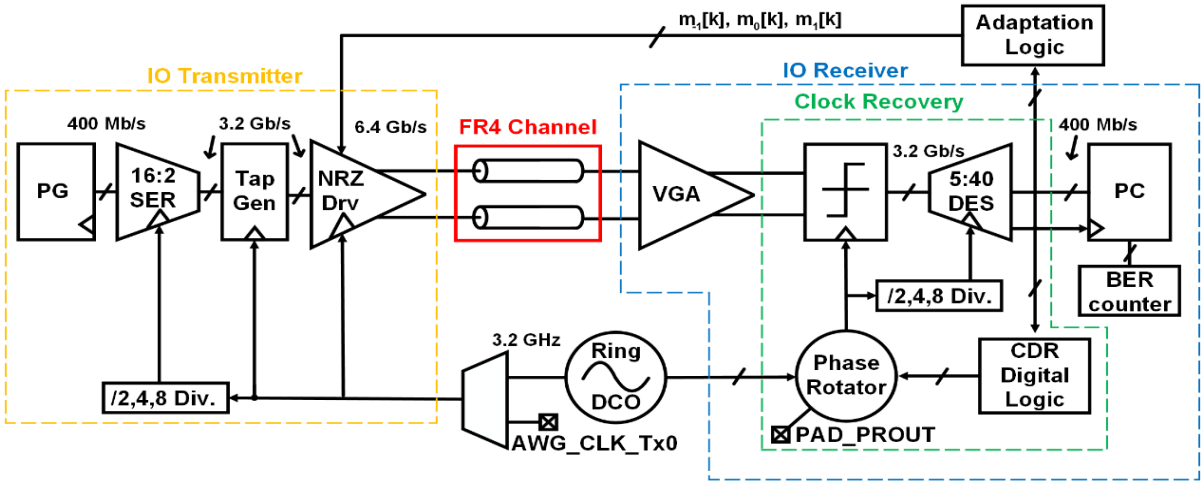



Fig. 1. Proposed IO transceiver block diagram

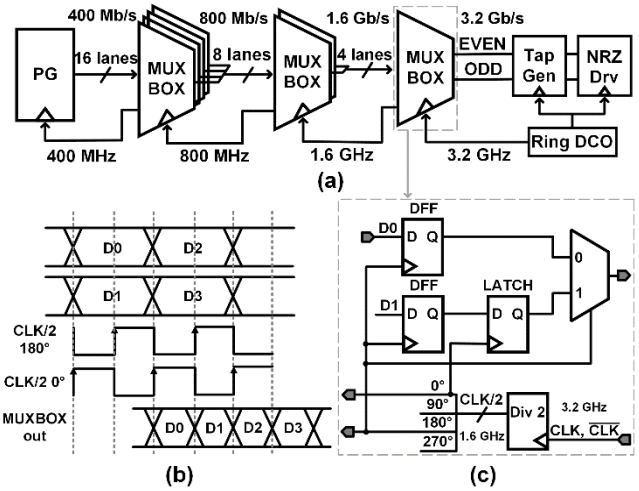



Fig. 2. (a) 3-stage 16:2 serializer block diagram. (b) Mux box serializing timing diagram. (c) Mux box circuit and clock dividing.

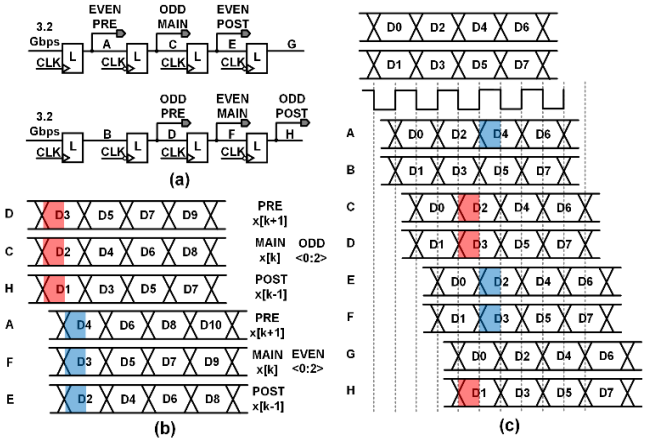



Fig. 3. (a) Tap generator circuit. (b) Aligned tap signal for FIR driver input. (c) Tap generator timing diagram.

the rising edge of the 180 degree clock. Consequently, even and odd data are serialized in one cycle as shown in Fig. 2(b). The serializer receives 16 bits from PG and serializes them into 2 bits to operate the driver at half rate.

A tap generator was configured to send appropriate high speed tap signals in parallel to each pre/main/post tap driver segments as shown in Fig. 3(a). Out of several cascaded stages of latches, the proper nodes where the three tap signals are aligned on the timing diagram were taken out as shown in Fig. 3(b). For ODD data the nodes of D, C, H (Pre, Main, Post) configure the output in parallel, and for EVEN data the nodes of A, F, E (Pre, Main, Post) configure the output in parallel as presented in Fig. 3(c). Odd data and even data are triggered by a difference of half a clock cycle. This configuration is set to send odd/even data to the segmented driver at half rate on the rising and falling edges of the clock.

The adaptive FIR filter consists of pre/main/post driver segments, and the output voltage level of the driver is determined by the influence of all tap segments as shown in Fig. 5 and the truth table of pre-driver logics is presented in Fig. 6. The pre-driver controls the driver segment by receiving show tap coefficient signal from Digital Loop Filter (DLF) and high-speed tap signal from the tap generator. By controlling the number of driver segments through pre-drivers, the number of MOSFET stacked between supply and ground can be reduced. The number of segments is enabled by the size of the value corresponding to the tap coefficient, where power up (PU) turn on a segment. In order to maintain equivalent MOS size between segments the PU signal enabled by thermometer decoder. The sign signal in Fig. 5 is determined according to the sign of the tap coefficient. Data (EVEN / ODD) is a fast signal that moves in giga hertz units, but the PU signal is a slow signal in mega hertz units that is updated slowly and used during adaptation.

### *B. Receiver*

In Rx shown in Fig. 4, the signal received after the channel is amplified to the intended amplitude offset by variable gain amplifier (VGA) in the adaptation loop. Once the data is determined through the 5 slicers, the 5 signals are deserialized, calculated as error signals and integrated for FIR/VGA coefficient adaptation and CDR loop. VGA serves to amplify the received signal through various gains. Fig. 5 shows the 2 - stage VGA with 2-dimensional control. The

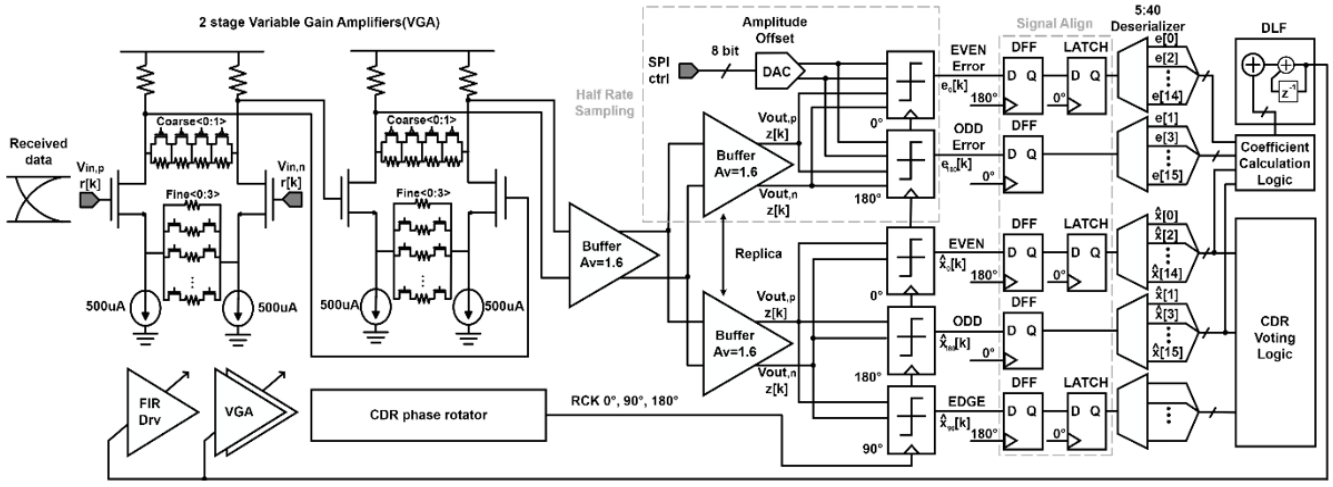



Fig. 4. Receiver circuit diagram and adaptation path.

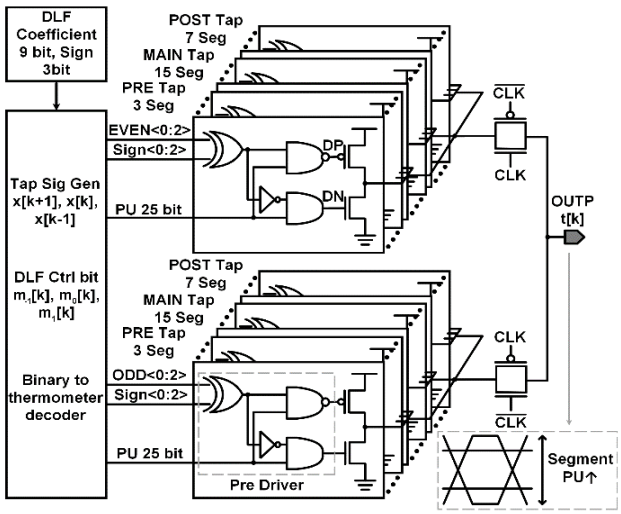



Fig. 5. 4-tap half rate FIR driver and pre driver.

| PU | SIGN | EVEN /ODD | DP | DN | OUTPUT SWING |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | Open |
| 0 | 0 | 1 | 1 | 0 | Open |
| 0 | 1 | 0 | 1 | 0 | Open |
| 0 | 1 | 1 | 1 | 0 | Open |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 |

Fig. 6. Pre driver truth table.

source resistance adjusts the fine gain and the drain resistance controls the coarse gain for wide-range. The drain resistors are connected in series but the source resistors are placed in parallel in order to result in linear gain controls. Fig. 7 presents simulation results of the VGA at 6.4 Gb/s data rate,where minimum and maximum gains span from 1.4 to 2.2 times.

The phase rotator circuit is shown in Fig. 8. The 4 input nodes receive from 0 degree clock to 270 degree clock from

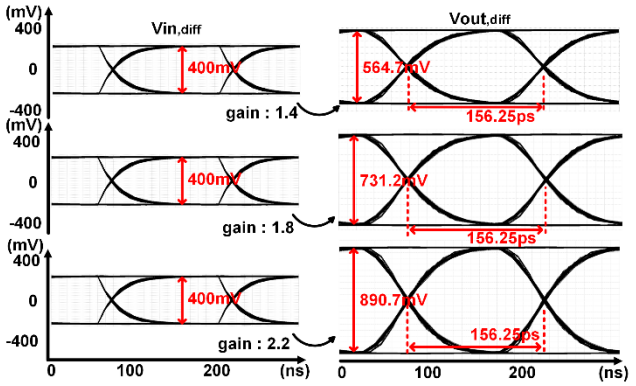



Fig. 7. VGA and Buffer input and output signal swing during gain control.

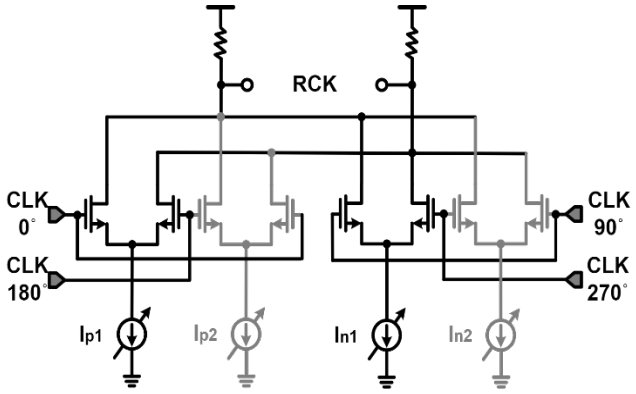
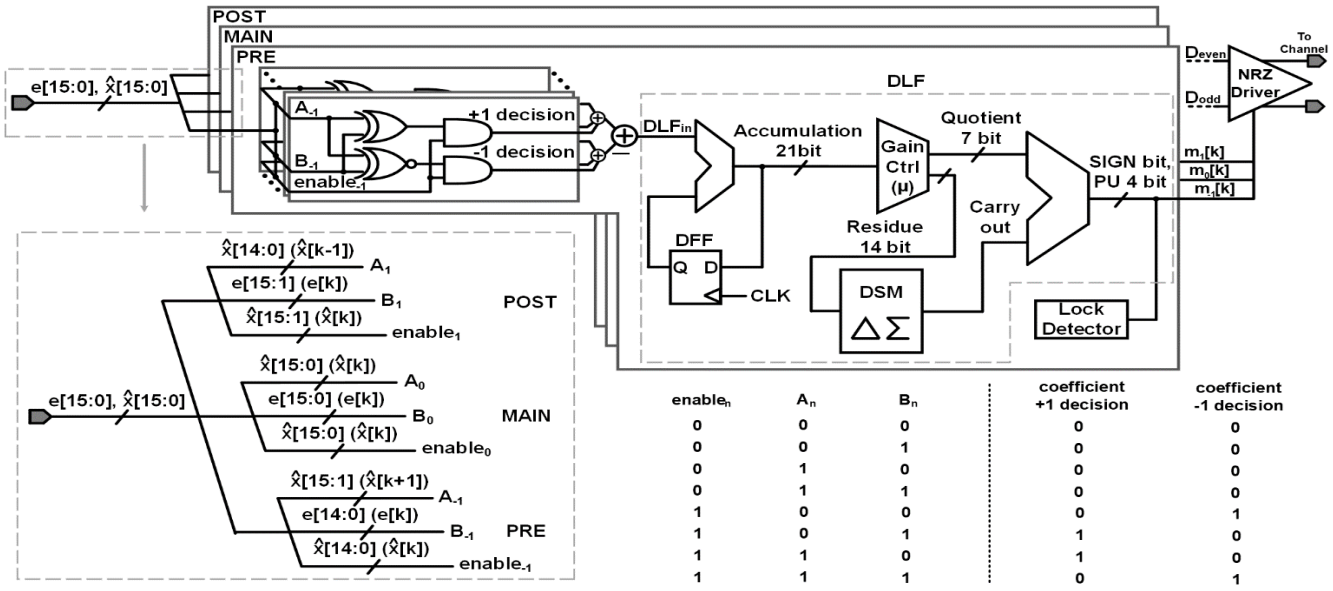



Fig. 8. Phase rotator circuit

a 4-stage ring oscillator. 6-bit current DACs ($I_{p1}$, $I_{n1}$, $I_{p2}$, $I_{n2}$) controls the strength weight of 4 input clock signals interpolates the transition timing of output RCK nodes over 360 degree phase span. And tap coefficient decision logic and truth table is presented in Fig.9.

Slicers are designed with a strong-arm latch topology as shown in Fig. 10(a). The latch compares the voltage-level of the differential inputs at the rising edge of the clock. If DINP voltage is larger than DINN, DOUTP is determined as 1 and vice versa as illustrated in Fig. 10(b). The slicer with offset as shown in Fig. 11(a) operates at half rate and the offset is adjusted with an 8-bit binary resolution from SPI signal. This




| $enable_n$ | $A_n$ | $B_n$ | coefficient +1 decision | coefficient -1 decision |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 |

Fig. 9. Tap coefficient decision logic and truth table.

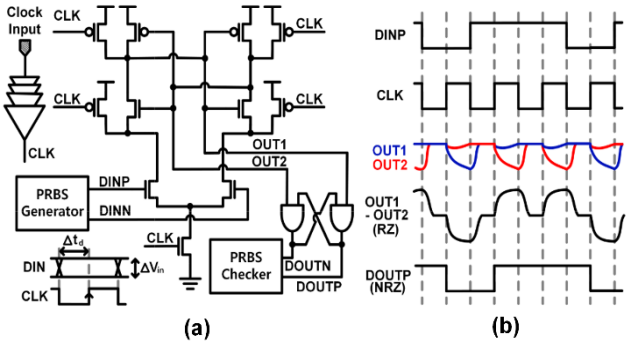



Fig. 10. (a) Strong arm latch circuit. (b) Waveform of signals at strong arm latch.

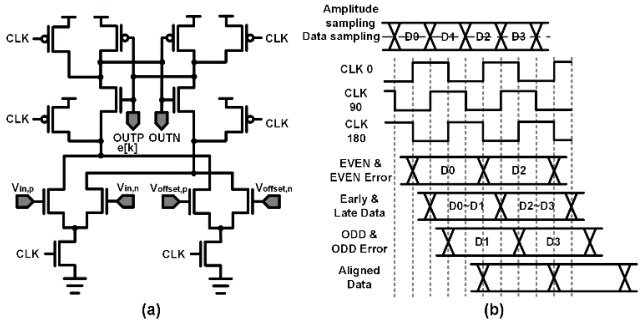



Fig. 11. (a) Strong arm latch circuit with offset. (b) Sampling timing diagram.

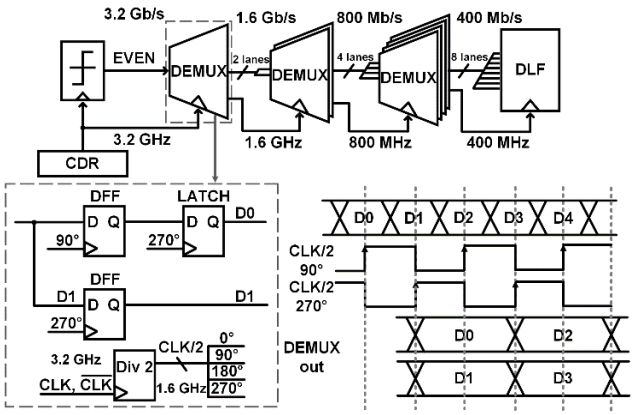



Fig. 12. Deserializer circuit and timing diagram.

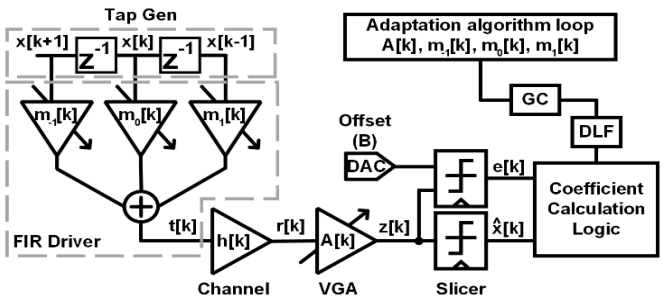



Fig. 13. FIR filter block diagram.

determines the error signal (e[k]) of the data by determining whether it is larger or smaller than the offset value. 0-degree and 180-degree clocks also operate at half rate and In the three slicers depicted in Fig. 6, the slicers with determine whether the data is 0 or 1 to determine $\hat{x}_0$[k] and $\hat{x}_{180}$[k]. The slicer with a 90-degree clock creates an aligned clock phase to the data edge by providing information whether the clock timing is early or late for the CDR block when there is a data transition. Since sampling is performed at independent timings in the slicer, the data is digitally re-aligned through D flip-flop and latch unit timing adjustment before deserialization as shown in Fig. 11(b).

The 3.2 Gb/s serial data from the slicer is converted into 400 Mb/s parallel data of 16 lanes through the deserializer. In DEMUX, data is parallelized using two D flip flops and latch, similar to the mux box of a serializer, as shown in Fig. 12. The slicer creates error data (e[k]) depending on whether the data is greater or less than the offset. Using the sign-sign LMS algorithm, the following coefficients are determined according to the values of $\hat{x}$[k] and e[k]. Since $\hat{x}$[15:0] and

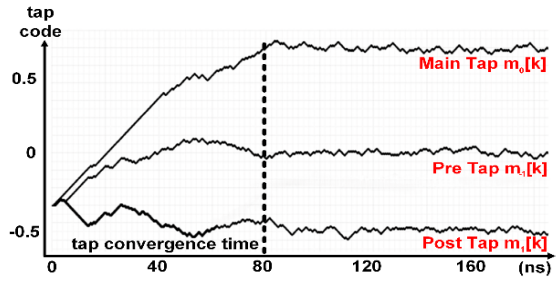



Fig. 14. Simulation result of FIR tap coefficient convergence using sign-sign LMS algorithm.

e[15:0] are parallelized, 16 coefficient decision logics are calculated all at once with the deserialized speed (Fig. 9). The range of the parallelized values spans from -16 to 16. The error value obtained by subtracting the results of the two additions are accumulated to the existing coefficient (m[k]) in DLF to create a new coefficient (m[k+1]). The convergence speed of the coefficient is determined by the gain controller. In general, the larger gain results in the faster convergence speed, but the range of toggling code after convergence becomes wider.

## III. ADAPTATION ALGORITHM

The adaptation loop is based on the LMS algorithm and the tap weight is determined by sign-sign LMS, which enables simpler and digitized hardware implementation. Fig. 13 shows a block diagram with 3-tap FIR filters along with sign-sign LMS. Fig. 14 is the simulation result of each tap coefficient converging when using the sign-sign LMS algorithm. The channel loss was 12dB at the Nyquist rate of 3.2 GHz.

$$t[k] = m_{-1}[k]x[k+1] + m_0[k]x[k] + m_1[k]x[k-1] \quad (1)$$

$$e[k] = z[k] - B\hat{x}[k] = A[k]r[k] - B\hat{x}[k] \quad (2)$$

In equation (1), x[k+1], x[k], and x[k-1] mean pre/main/post tap signals respectively, which corresponds to the designated nodes in Fig. 3. $m_{-1}$, $m_0$, $m_1$ mean the coefficients of pre/main/post tap respectively and are the outputs of the DLF as well, as shown in fig. 12. t[k] is the FIR driver output and pre-emphasized NRZ signal. r[k] is the result of the convolution product of t[k] and h[k] and is the VGA input analog signal of Rx, and z[k] is the r[k] signal amplified by the VGA. $\hat{x}$[k] is the signal sampled as 0/1 by the slicer and the B value is the offset value in the slicer set by the DAC. The LMS algorithm is difficult to implement using analog circuits. Therefore, if each variable is updated in the right direction with digitized sign values, the error signal $e^2$[k] will eventually be minimized, so the digital sign-sign LMS algorithm, which has simpler hardware implementation, was used. Additionally, since x[k] is an unknown value in Rx, it was replaced with $\hat{x}$[k], a value which is determined as 0 or 1 by the slicer and available for the algorithm instead.

$$m_{-1}[k+1] = m_{-1}[k] - 2\mu \cdot sign(\hat{x}[k+1])sign(e[k]) \quad (3)$$

$$m_0[k+1] = m_0[k] - 2\mu \cdot sign(\hat{x}[k])sign(e[k]) \quad (4)$$

$$m_1[k+1] = m_1[k] - 2\mu \cdot sign(\hat{x}[k-1])sign(e[k]) \quad (5)$$

The modified tap weight through the sign-sign LMS algorithm is shown in equation (3) to (5). sign($\hat{x}$[k]) / sign(e[k]) have a value of 1/-1, but $\hat{x}$[k] and e[k] have a value of 0/1. In coefficient decision logic, the coefficient is +1/-1 was calculated independently. The μ value is a variable

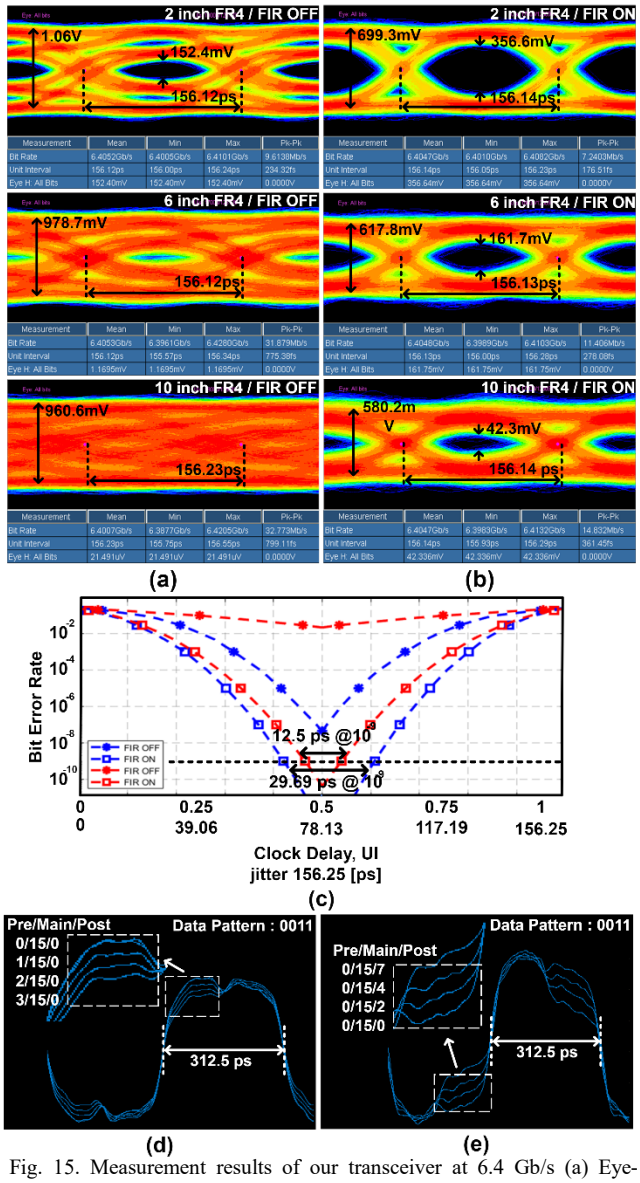



Fig. 15. Measurement results of our transceiver at 6.4 Gb/s (a) Eye-openings at Tx output without using FIR for 2 inch, 6 inch, 10 inch FR4 channel. (b) Eye-openings at Tx output with FIR on. (c) Measured horizontal bathtub improvement 6 inch/10 inch FR4 channel. (d) Measured pre tap weight control (e) Measured post tap weight control

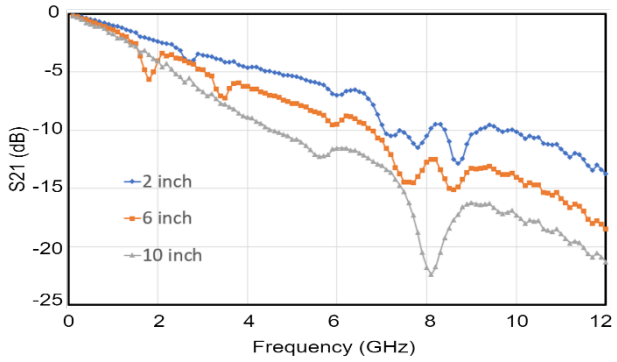



Fig. 16. Measured Channel Loss graph

TABLE I. Comparison results.

| Ref. | *Technology* | Data rate (bit/s) | Supply(V) | FIR tap | Power (mW/ch) | Channel Loss(dB) | Vertical eye(mW) | Horizontal eye(UI) |
|---|---|---|---|---|---|---|---|---|
| [6] | 65nm CMOS | 9.6 | 1 | 4 | 46 | 15.5 | 150 | 0.54 ($@10^{-12}$) |
| [7] | 65nm CMOS | 20 | 1.1 | 4 | 167 | 11 | 300 | 0.82 ($@10^{-12}$) |
| [8] | 28nm CMOS | 6.6 | 1 | 3 | 129 | 22 | 180 | 0.25 ($@10^{-9}$) |
| This work | 65nm CMOS | 6.4 | 1.2 | 3 | 64 | 10.3 | 356.6 | 0.48 ($@10^{-9}$) |

that determines the update rate of each variable and is determined by the MUX selection signal of the gain controller. A large μ value has a fast settling time, but increases the fluctuation range of the convergence value and therefore noise increases. After sufficient iterations, the error value reaches 0 and the adaptive variables converge.

## IV. MEASURE RESULTS

Fig. 15 shows the measurement results of our transceiver at 6.4 Gb/s. Tx eye-openings and BER are measured using Tektronix TDS6154C. Fig. 15. (a) and Fig. 15. (b) show the measured eye-opening when FIR is ON/OFF using 2 inch, 6 inch, and 10 inch FR4 microstrip lines, respectively. The 2 inch FR4 channel has a channel loss of 10.3dB, the 6 inch has a channel loss of 11.7dB, and the 10 inch has a channel loss of 13dB at the Nyquist rate. Without pre-emphasis, the vertical eye opening in the 2 inch channel is 152.4mV/1.06V and for 6 inch/10 inch channels, the eyes were completely closed. With the pre-emphasis on, Vertical eyes are improved to 356.6 mV / 699.3 mV, 161.7 mV / 617.8 mV, and 42.3 mV/580.2mV respectively. Additionally, total jitter improved from 82.2ps to 49.5ps in the 2 inch channel horizontally. The measured horizontal bathtub curve is presented in Fig. 15 (c). When using 2 inch, 6 inch, and 10 inch channels, the horizontal eye-openings were improved by improved by 0.21UI, 0.19UI, and 0.08UI, respectively $10^{-9}$ BER. By inserting the [0011] pattern and piling up eye history, the pre tap and the post tap can be checked to be adjusted and to perform pre-emphasis operation successfully Fig.16 shows the measured channel loss graph. According to this graph, losses of -6.6dB at 2 inch, -8.7dB at 6 inch, and -11.5dB at 10 inch were measured at 6.2GHz. The lack of significant differences for each inch could be attributed to greater losses from other factors such as connector loss. Fig. 17 shows the layout of our IP. Our transceiver has been fabricated in 65nm CMOS process and occupies a chip area of 0.506 $mm^2$. The measured power consumption is 64mW.

Successful transmission and reception of the high-speed data signal was achieved by adapting tap coefficients to various channel loss environments. Table 1 summarizes our Tx performances and compares them with previous work.

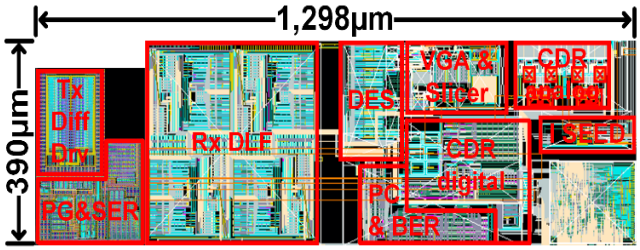



Fig. 17. Proposed IO transceiver layout.

When compared to the results of other papers, this design achieved a higher vertical eye opening and lower scaled power due to the half-rate architecture scheme. The LMS digital backend automatically adjusts the transmitter tap weight for various channel loss conditions.

## V. CONCLUSION

The proposed circuit is an IO transceiver that transmits and receives high-speed data at a data rate of 6.4 Gbit/s, and the Tx FIR driver can remove ISI noise dramatically and increase the data transmission rate. The adaptive FIR filter using the sign-sign LMS algorithm can adapt the FIR coefficient to the unknown channel by finding appropriate weight values automatically.

## ACKNOWLEDGMENT

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