Design of a 128x128 ROIC Array for Development of Uncooled 2.6 μm-wavelength SWIR Imaging Camera

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***Abstract* - This paper details the development and extensive silicon-level verification of a 128 × 128 Readout Integrated Circuit (ROIC) tailored for uncooled Short-Wave Infrared (SWIR) imaging cameras, which operate at a 2.6 μm wavelength. We conducted silicon-level verification of the developed ROIC, enabling a detailed analysis of various performance aspects. This evaluation will help us identify potential explore for further improvements, significantly advancing SWIR imaging camera systems. Our goal is to gain a deeper understanding of performance dynamics to enhance operational efficiency and image quality. The prototype ROIC was manufactured using a 0.18-μm 1P6M CMOS process, featuring an effective pixel resolution of 128 (H) × 128 (V), specifically designed for InGaAs FPAs. The prototype consumes 42.25 mW of power and achieves a frame rate of 390 frames per second. The fabricated chip show that the Noise level is 72.65 μV_{rms} and Pixel-FPN is 21 LSB_{rms}.**

***Keywords*— Short-Wave Infrared (SWIR) Imaging, Readout Integrated Circuit (ROIC), CMOS imager sensor (CIS), Indium Gallium Arsenide (InGaAs) Detectors.**

I. INTRODUCTION

In recent years, there has been a global surge in interest towards Short-Wave Infrared (SWIR) image sensors, primarily driven by their diverse applications across various technological fields [1]-[3]. Particularly, SWIR imaging sensors utilizing Indium Gallium Arsenide (InGaAs) detector arrays have garnered considerable attention [4], [5]. This interest stems from the unique advantages offered by the SWIR optical band coupled with the matured InGaAs Focal Plane Array (FPA) technology. Unlike Mid-Wave Infrared (MWIR) and Long-Wave Infrared (LWIR) imaging, SWIR imaging leverages reflected light, facilitating the integration of various performance enhancement technologies already prevalent in the saturated domain of visible imaging systems [6]-[8].

Over the recent years, significant advancements have been made in the primary performance metrics of InGaAs FPAs, such as reductions in dark current values and improvements in full well capacity [9]. These advancements have enabled the development of compact, low-power uncooled SWIR imaging cameras, a leap forward in the field. Furthermore, among the critical functional blocks constituting SWIR imaging systems, the Readout Integrated Circuit (ROIC) presents opportunities for additional performance enhancements of InGaAs FPAs [10]-[12]. For instance, through ROIC, sensitivity of InGaAs-based pixels can be controllable in both analog and digital domain depending on ambient conditions, while mitigating of pixel fixed pattern noise. Moreover, the technical and physical constraints of the sensor material can be effectively mitigated by incorporating advanced ROIC with correction technologies. These include methods that minimize inherent variations in InGaAs-based pixel characteristics due to temperature changes and stabilize Signal-to-Noise Ratio (SNR) variations based on dark current characteristics at different wavelengths, enhancing overall stability and reliability. This enables the realization of high-resolution, highly sensitive SWIR image sensors optimized in terms of area occupation, power consumption, and operational speed.

In this work, our objective is to develop and validate a 128 × 128 ROIC array specifically designed for InGaAs FPAs, with a focus on facilitating the creation of a 2.6 μm wavelength SWIR imaging camera. We conducted a silicon-level verification of the developed ROIC, enabling a detailed analysis of diverse performance aspects. This evaluation will help to identify potential ways for further enhancements, thereby contributing significantly to the advancement of SWIR imaging camera systems. Finally, we aim to gain deeper insights into the performance dynamics for elevating their operational efficiency and imaging quality.

The structure of the remainder of this paper is organized as follows: Section II details the design aspects of the 128 x 128 ROIC array. Section III presents the experimental findings about the prototype chip. Finally, Section IV provides the conclusion.

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II. CIRCUIT IMPLEMENTATION

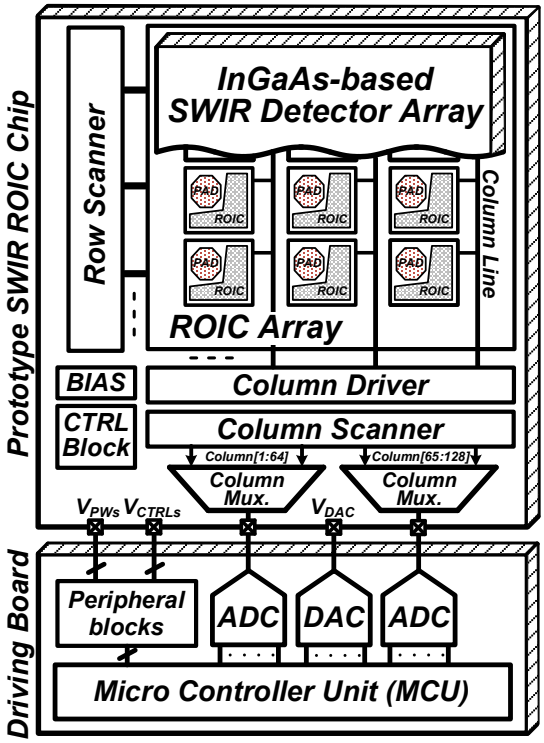

Fig. 1. Overall block diagram of prototype ROIC

Fig.1 illustrates an overall block diagram of the prototype ROIC that is coupled with InGaAs-based SWIR FPA. The prototype ROIC is composed of Capacitive Transimpedance Amplifier (CTIA)-configured ROIC array, a row scanner, a column driver, and a column scanner. These components are supported by bias circuitry and control blocks designed to optimize the ROIC performance. The driving board is constructed using a 4-layer PCB, which includes various components for comprehensive functionality. It is equipped with power supply circuits (V_{PWs}) to ensure stable power delivery, alongside clock control signals (V_{CTRLS}) essential for operating the ROIC chip. Additionally, the board includes an ADC for converting the output analog signals into digital format. For system verification and control, a MCU and a DAC are also integrated into the driving board design.

The processed signals from the ROIC array are conveyed to a pair of Analog-to-Digital Converters (ADCs) on the external driving board via two output channels, facilitated by column multiplexers (Mux). The specifications of the external ADC [13] are as follows: it has a resolution of 14 bits, with an Integral Nonlinearity (INL) and a Differential Nonlinearity (DNL) of ±2.5 and ±0.7, respectively. The Signal-to-Noise and Distortion Ratio (SNDR) is 77.5 dB, while the Spurious-Free Dynamic Range (SFDR) stands at 90 dB. Additionally, the input referred noise of the ADC is quantified at 0.36 LSB. Additionally, a Digital-to-Analog Converter (DAC) provides test signals, allowing the evaluation of the ROIC's unique functionalities and its performance metrics. The external DAC [14] features a 14-bit resolution. Its INL and DNL are both specified at ±2.5. The SFDR is 82 dB. Additionally, the gain error falls

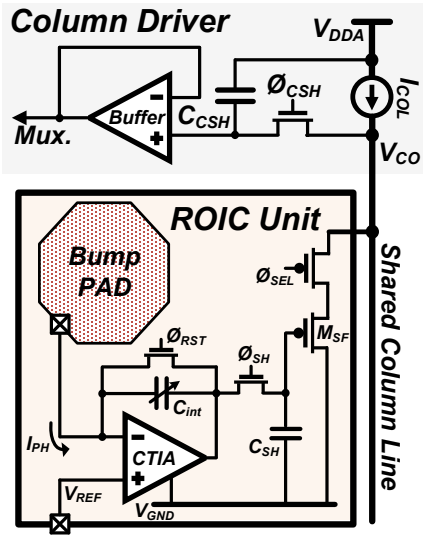

Fig. 2. Simplified schematic of CTIA-configured ROIC unit with column driver

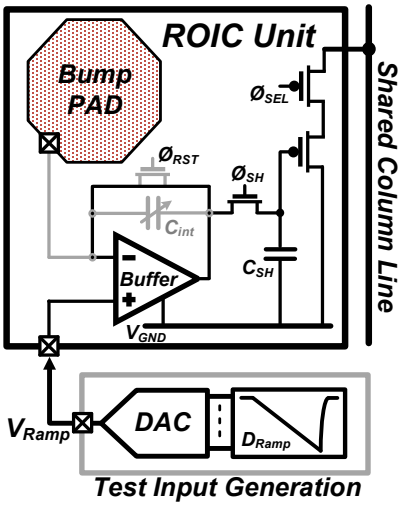

Fig. 3. Simplified schematic of verification mode for ROIC array

within ±1% of the Full Scale Range (FSR), and the offset error is maintained within ±0.025% FSR. Conclusively, the micro controller unit (MCU) is responsible for generating varied operation timings for verification, managing the various control signals, and interfacing with external devices or systems. This ensures the proper signal processing or display of the imagery data acquired by the prototype ROIC.

Fig.2 shows a simplified schematic of a signal readout chain that includes the CTIA-configured ROIC unit (pixel) along with a column driver. The readout signal chain starts with pixel input circuitry followed by the column driver circuit, composed of a bump pad, a CTIA, a global sample-and-hold (S/H) circuit, a column line driver, a column S/H circuit, and a column output driver. The Bump pad is used for flip-chip bonding, connecting the ROIC to another substrate or component. Row and column of the whole ROIC array addressing operations are controlled by the row and column scanner circuits, respectively. The prototype ROIC supports two different readout modes: global shutter mode [15] and rolling shutter mode [16].

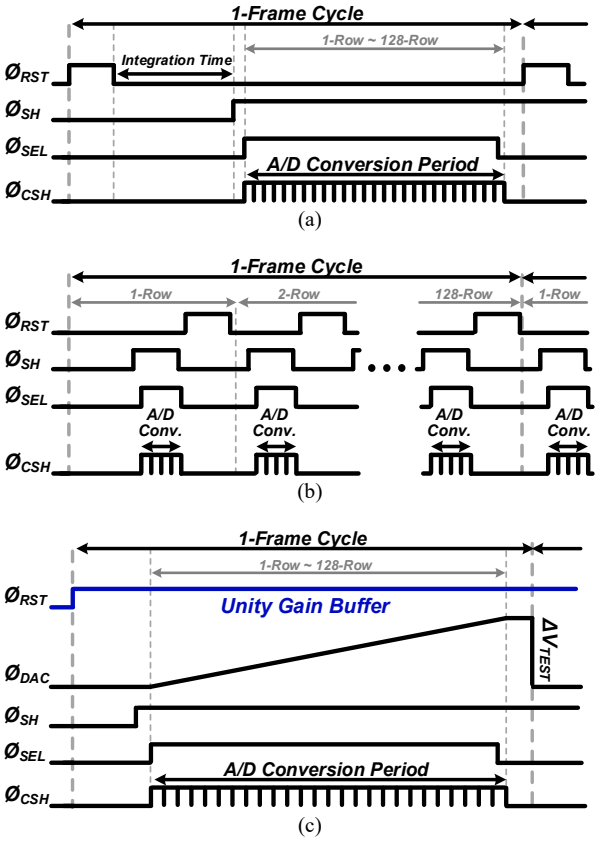

Fig. 4. Simplified operational timing diagram of three modes: (a) global shutter mode, (b) rolling shutter modes, and (c) test mode

In global shutter mode, all pixels in the ROIC array capture light simultaneously. Then, after a fixed exposure time, the ROIC reads out the signal from the entire pixel array. During this mode, the output of CITA is concurrently sampled using a global S/H circuit with the Φ_{SH} and the C_{SH}, to maintain the integrity of the exposure data. Conversely, the rolling shutter mode operates on a sequential exposure basis. Each row of pixels is activated in sequence by the row scanner, which allows for staggered exposure and readout in a row-wise progression. This process initiates from one end of the pixel array and advances systematically to the opposite end. Subsequent to integration, pixel signals are routed to the column readout circuits. The column readout circuitry is structured with multiple parallel columns, each equipped with a column amplifier with the M_{SF} and I_{COL}, a column S/H circuit with the Φ_{CSH} and the C_{CSH}, and a column buffer. After amplification by the column amplifier, the pixel signal is captured and retained by the column S/H circuit, and subsequently buffered. It is then multiplexed via the column switch in a sequential manner at column level controlled by the column scanner. In the final stage, the multiplexed signals are directed off the chip via output drivers.

Fig.3 presents a simplified schematic specifically for the verification mode of a ROIC array, which is essential for testing and performance analysis in SWIR imaging systems. In this mode, the ROIC unit is set to function as a unity buffer, achieved by activating the reset switch (Φ_{RST}). This configuration enables a straightforward evaluation of the

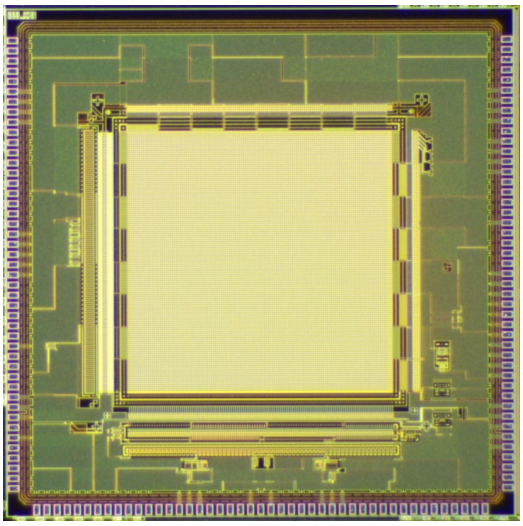

Fig. 5. Microphotograph of the prototype ROIC chip

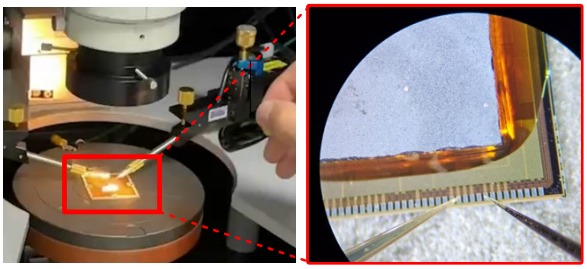

Fig. 6. Test environment of customized InGaAs FPA

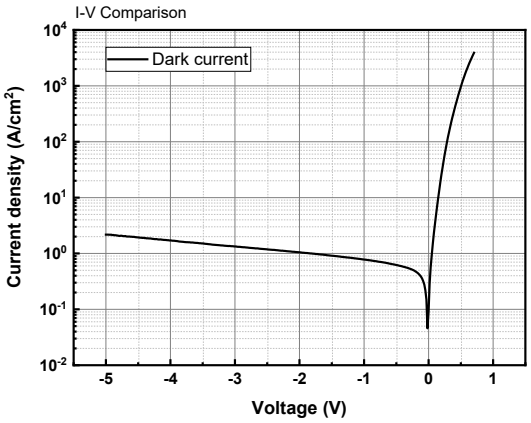

Fig. 7. Dark current density of customized InGaAs FPA in uncooling condition

ROIC's operational characteristics. Test signals are generated using an external 14-bit DAC from the customized driving board, to produce a ramp signal that is applied to the positive node of the CTIA. The pixel's output replicates the test input, thereby facilitating a detailed verification of the ROIC array. By employing this approach, the ROIC design for SWIR imaging can be effectively utilized to address a wide range of operational issues and facilitate comprehensive performance analysis.

Fig.4 illustrates a simplified operational timing diagram for three different modes of the prototype ROIC. In

Fig. 8. Captured test images with varied ramp signal input in test mode

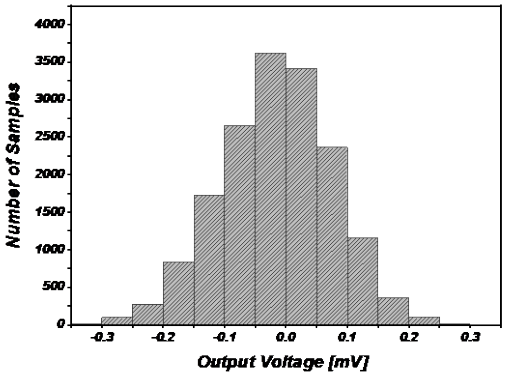

Fig.9. Measured output noise histogram of prototype ROIC

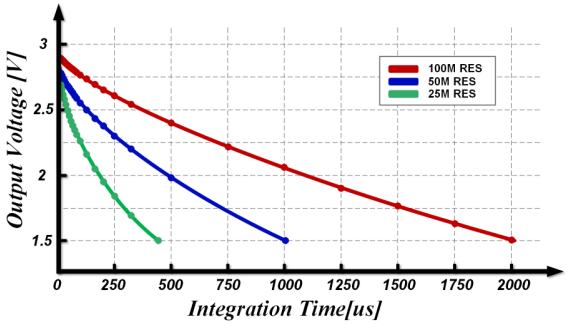

Fig. 10. Characteristic curve of output voltage in relation to the input current magnitude

the case of the Φ_{SH} signal, it operates in an inverted structure, meaning that a "0" indicates Turn On, while a "1" represents Turn Off. In the global shutter mode (Fig.4 (a)), all pixels are simultaneously exposed to light, enabling synchronous image capture, and subsequently, the pixel data is read out in a sequenced manner. Conversely, the rolling shutter mode (Fig.4 (b)) employs a sequential approach, which allows for staggered exposure and readout in a sequential row-by-row manner. In the test mode (Fig.4 (c)), the ROIC is capable of simulating both the global and rolling shutter operations and utilizes a ramp input signal, ΔV_{RAMP}, generated by an external DAC as the test input.

III. EXPERIMENTAL RESULTS AND DISCUSSIONS

The micrograph of the chip is shown in Fig.5. The prototype chip was fabricated using a 0.18-μm 1-poly 6-metal (1P6M) CMOS technology, which occupies an area of 5 × 5 mm^2 with the 128 (H) × 128 (V) pixels array of 20 μm-pitch pixels, the row scanner, the column driver, the column scanner, and column multiplexers. The prototype CIS demonstrates a frame rate of 390 frames/s with the master clock of 20 MHz. The total power consumption is 42.25 mW.

To assess the dark current of a customized InGaAs detector within a 128 × 128 unit, as shown in Fig.6, we conducted measurements on four test pixels at room temperature when it is not exposed to light.

Fig.7 shows the measured dark current density of InGaAs detector in the room temperature. The performance of dark current is approximately 100 times higher than that of Hamamatsu's product [17]-[19]. However, although the dark current level is quite high, considering that our measurements were taken under uncooled conditions, the results are still meaningful and provide valuable insights. We are actively developing methods to reduce ROIC noise, which is a critical step toward realizing high-resolution pixel arrays. We anticipate that with these ongoing efforts, we will be able to develop a competitive SWIR camera with improved performance in the near future.

Fig.8 shows sample images captured from the output of the ROIC in test mode. To validate the operational characteristics of the ROIC, we obtained the output signal corresponding to a given test input through two output channels. This was achieved by shifting the signal by one clock cycle to effectively isolate and examine the ROIC's response. The measured performances of the prototype chip are summarized in Table I.

Fig.9 represents the measured output noise histogram of the prototype ROIC for each pixel, which was utilized to measure the random noise (RN) of the ROIC. In this experiment, 1000 frames were captured in test mode to calculate the standard deviation of noise. When the ROIC operated at its full input range of 1.6 V, the total RN value was measured at 90.3 μV_{rms}. The noise of the external ADC

and DAC are 43.9 μV_{rms} and 30.9 μV_{rms}, respectively. Consequently, the prototype ROIC noise is calculated as 72.65 μV_{rms}.

TABLE I. PERFORMANCE SUMMARY

Parameter	Value
Technology	content
Total area	$5 \times 5\ mm^2$
Pixel type	InGaAs detector
Pixel size	20 μm × 20 μm
Number of pixels	128 (H) × 128(V)
Random noise	72.65 μV_{rms}
Pixel FPN	21 LSB_{rms}
Frame rate	390 fps
Power consumption	42.25 mW

Fig. 10 depicts the characteristic curve of output voltage in relation to the input current magnitude. Measurements were carried out on a test-patterned 1 × 4 ROIC array. For these measurements, input currents were generated using different resistances: a 100 megaohm (MΩ) resistor to produce a current of 100 picoamperes (pA), a 50 MΩ resistor for a 200 pA current, and a 25 MΩ resistor to generate a current of 400 pA. The observations revealed that with each doubling of the input current, there was a corresponding decrease in the output voltage by a factor of two. Furthermore, a linear relationship was observed in terms of the integration time. These findings were instrumental in identifying key design issues within the ROIC and have provided clear guidance on the future research direction needed to improve the alignment and overall performance of the ROIC.

IV. CONCLUSION

In this study, we introduce a prototype design of a 128 x 128 ROIC with the goal of furthering the development of an uncooled SWIR imaging camera operating at a wavelength of 2.6 μm. The developed ROIC was verified in various ways at the silicon level, which allowed for an extensive analysis of its various performance parameters. Utilizing this evaluation environment, we aim to generate and validate innovative concepts for enhancing SWIR imaging performance in diverse ways.

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