# A 28-GHz CMOS Power Amplifier with Ribbon Cell

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***Abstract* - In this paper, we present a ribbon cell CMOS power amplifier in which the structure of the power cell is like a ribbon. As the frequency increases, the output impedance decreases due to parasitic capacitors, so an interstage inductor is used. The interstage inductor used in previous research has the problem of increasing the size of the chip. Ribbon cells use larger interstage inductors through mutual inductance. Therefore, a metal smaller than the desired inductor metal size can be used. This allows the chip size to be designed to be small. It also improves AM-PM distortion and IMD3. It operates at 28 GHz with a 2.4 V supply voltage and achieves IMD3 of -40dBc at 10 dBm output power and -30dBc at 12.3 dBm output power and PAE of 19% and 25% respectively. It has a saturated output power of 18.4dBm and achieves a gain of 11.6dB at a P1dB of 16.4dBm.**

***Keywords*—28GHz, AM-PM, CMOS, IMD3, PA**

## I. INTRODUCTION

Recently, with the development of the Internet of Things (IoT), various types of IoT communication networks are being used, such as smart factories, smart buildings, smart homes, and smart farms. The e-UM 5G application using the 28GHz band supports IoT systems, and a 28 GHz transceiver is required to configure the network, as everything needs to be transmitted and received to communicate. In addition, since communication is performed based on a battery, low power consumption and miniaturization are essential. Therefore, a single-chip transceiver using the CMOS process is suitable.

When developing a single-chip transceiver using the CMOS process, linearization techniques are essential because it is very difficult to secure the linearity of the power amplifier due to the nonlinearity of the transistor. Existing researched techniques include adaptive bias circuits, structures that minimize capacitance changes with additional bias voltage, and Digital Pre-Distortion (DPD) [1-5]. The above linearization techniques have the disadvantage of requiring additional passive elements and circuit connections, resulting in additional area. Therefore, in this paper, we designed a CMOS power amplifier using the Ribbon Cell linearization technique that minimizes the chip area and does not use additional power.

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Manuscript Received Nov. 24, 2023, Revised May 15, 2024, Accepted May 20, 2024

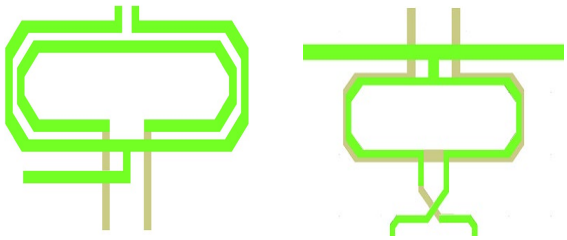


## II.CMOS PA WITH RIBBON CELL CIRCUIT DESIGN

Figure 2 shows the schematic of the proposed CMOS power amplifier. Power amplifiers with a ribbon cell structure operate in a differential cascode structure. A differential cascode structure has been used due to CMOS process issues. The transistor used was NMOS, and the size of each transistor is in Table 2. Additionally, a ribbon cell structure was proposed to improve the linearity of the power amplifier.

### *A. Differential Cascode structure*

The CMOS process is grounded with a bonding wire or metal line. Because there is no ground VIA. Therefore a differential amplifier structure was used to provide a virtual



(a) (b)

Fig. 1. Transmission line transformer matching network
(a) Input TLT design (b) Output TLT design

TABLE I. Transmission line transformer parameters.

| | Input TLT | Output TLT |
|---|---|---|
| Type | Edge Coupling | Broadside Coupling |
| Primary (Metal /Width) | OI / 5um | OI / 5um |
| Secondary (Metal /Width) | IB/ 8um | IB/ 5um |
| Size | 170um x 135um | 160um x 155um |

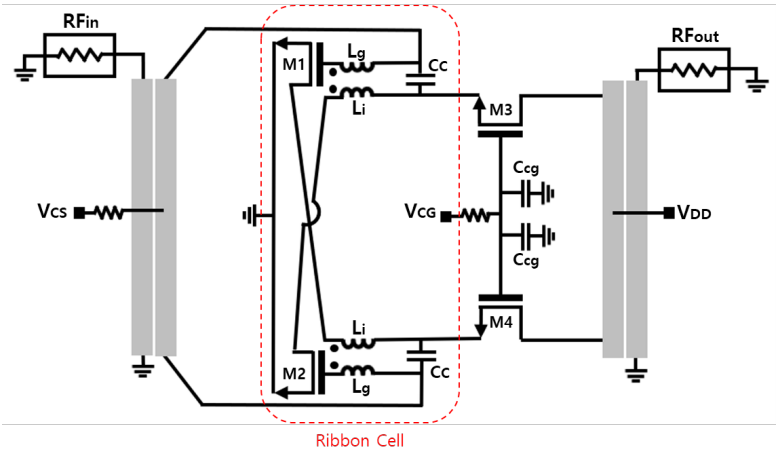



Fig. 2. Schematic of the proposed CMOS Power Amplifier

TABLE 2. Transistor size.

| TR Name | Gate finger width | Number of fingers | Multiplier | Total Gate width | Gate length |
|---|---|---|---|---|---|
| M1~M4 | 2 um | 16 | 8 | 256 um | 0.03 um |

ground. And when a differential amplifier structure is used, conversion between RF and differential signals is required. Therefore, a transmission line transformer (TLT) was used at the input and output to operate as a balun. In addition, the TLT allows the input and output impedance of the power amplifier to be matched. The input and output TLTs are shown in Figure 1 and the parameters are shown in Table 1. The input TLT is an edge coupling type with a size of 160um x 155um and the output TLT is a broadside coupling type with a size of 170um x 135um.

In addition, the proposed power amplifier has a cascode structure. This is because the CMOS process has a low breakdown voltage. The cascode structure provides sufficient voltage to the power amplifier. In addition, the cascode structure can reduce the Miller effect.

### *B. Interstage inductor through Ribbon Cell structure*

As the operating frequency increases, the real and imaginary parts of the drain impedance of a power amplifier using a cascode structure decrease due to parallel parasitic capacitance. However, if you connect a series interstage inductor between the Common Source (CS) amplifier and the Common Gate (CG) amplifier, The impedance of the real and imaginary parts of the drain increases.[7][8] Therefore, mismatch of the power amplifier can be avoided through the series interstage inductor. However, mismatch can be avoided by inserting and connecting a large series inductor, but since the metal length increases to use a large inductance in the layout, the chip size increases and RF path loss occurs. To address the above problems, we propose a power amplifier using a ribbon cell structure. Figure 3 shows the layout of the proposed ribbon cell structure. The series interstage inductor $L_i$ , which connects the drain of the CS amplifier and the source of the CG amplifier, is close to the gate metal line of the CS amplifier. In this layout, there is mutual inductance between $L_i$ and $L_g$ . Figure 4 is equivalently converted to the ribbon cell Structure T - model. It can be expressed as (1). $L_m$ is the mutual inductance. Through the above equation, it can be confirmed

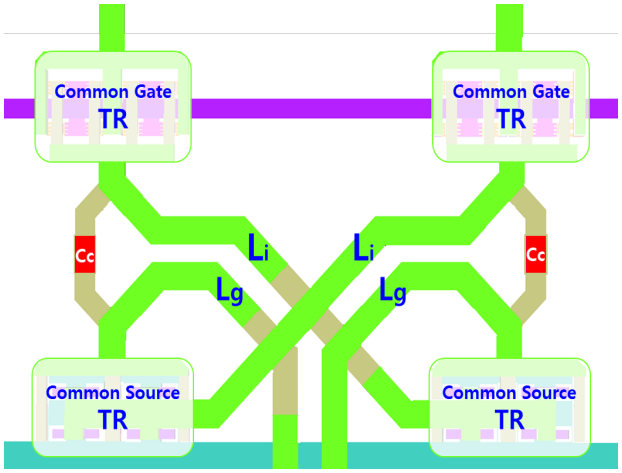



Fig. 3. Layout of the proposed Ribbon Cell

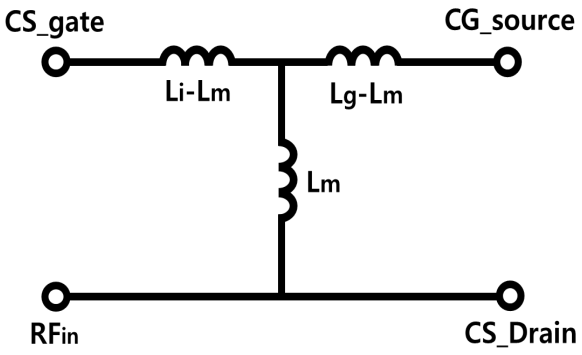



Fig. 4. T-model of Ribbon Cell

TABLE 3. Mutual inductance of ribbon cell

| inductor | pH |
|---|---|
| $L$ | 41.5 |
| $L_i$ | 47.3 |
| $L_g$ | 55 |
| m | 18 |

$$L = L_i - \frac{m^2}{L_g} \quad (1)$$

that there is mutual inductance, and the inductance of Li appears larger due to the mutual inductance. Therefore, the desired value of inductance can be achieved by using a small inductor, resulting in a size advantage. Table 3 shows the mutual inductance used in the proposed power amplifier.

## III. SIMULATION RESULTS

Linearity is improved when a ribbon cell structure is used in a CMOS power amplifier. Figure 5 and Table 4 show the AM-PM distortion and IMD3 simulation results with and without the ribbon cell structure. With the ribbon cell structure, an IMD3 of -40dBc is achieved at 10 dBm output power, and an IMD3 of -30dBc is achieved at 12.3 dBm output power.

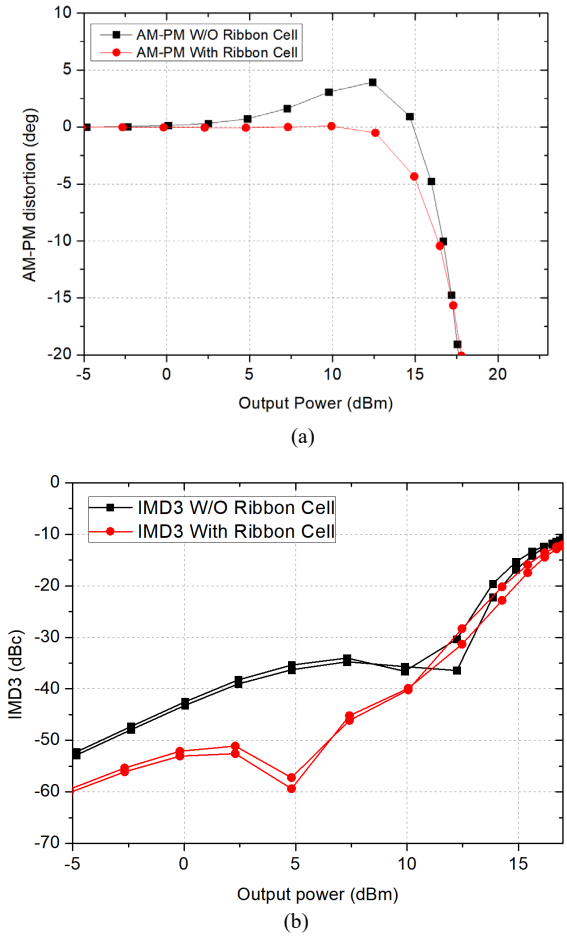



Fig. 5. Simulation results (a)AM-PM (b)IMD3

In Figure 6, it has a PAE of 19% and 25%. Therefore, with the ribbon cell structure, the desired series inductance can be used without increasing the size of the layout due to the inductor, and linearity is improved.

TABLE 4. simulation results of linearity

| | W/O ribbon cell' result | With ribbon cell result |
|---|---|---|
| AM-PM | 3.8 at 12dBm<br>3.1 at 10dBm | -0.38 at 12dBm<br>0.08 at 10dBm |
| IMD3 | -30dBc at 12.3 dBm | -40dBc at 10 dBm<br>-30dBc at 12.1 dBm |
| Linear PAE (IMD3 -40dBc) | - | 19% |

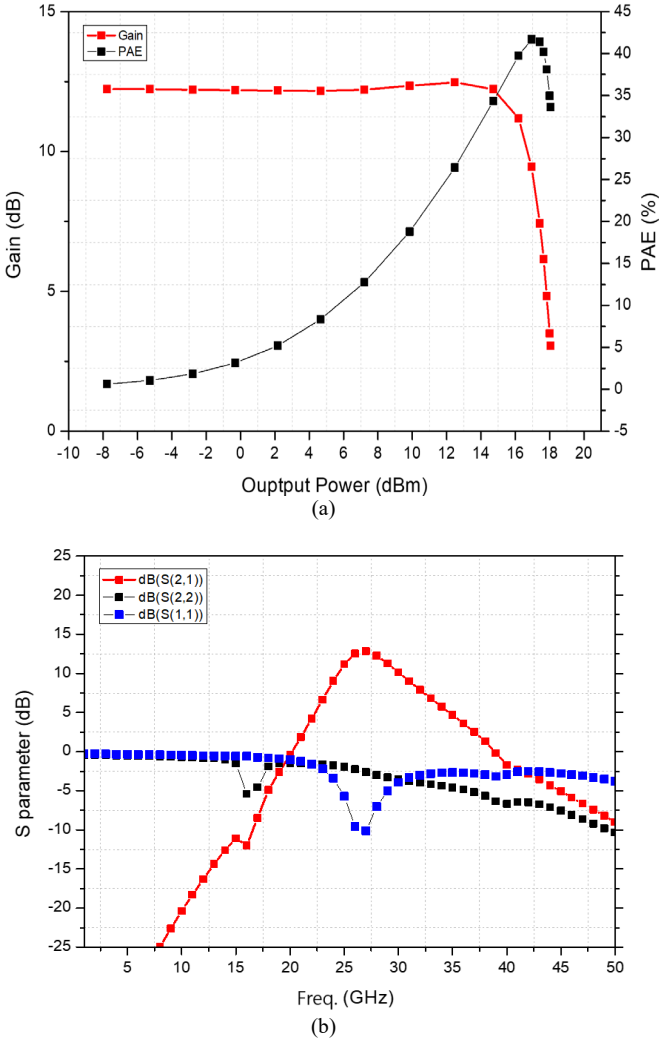



Fig. 6. Simulation results (a)Gain, PAE (b)S-parameter

Figure 6 shows the 1-tone simulation results of a CMOS power amplifier with a ribbon cell structure. At a frequency of a 28 GHz, the gain is 11.6 dB and the peak PAE is 41.8%. The S-parameter results, S(1,1) / S(2,2) / S(2,1), are -7 dB / -3 dB / 12.4 dB at 28 GHz frequency. The results in Figure 7 show that the stability factor is greater than 1 at all frequencies, indicating unconditional stability. Figure 8 shows the layout of the proposed CMOS power amplifier. It

has a size of 595um x 660um including the ESD PAD. Table 5 shows the performance comparison with a 28GHz CMOS PA with linearization.

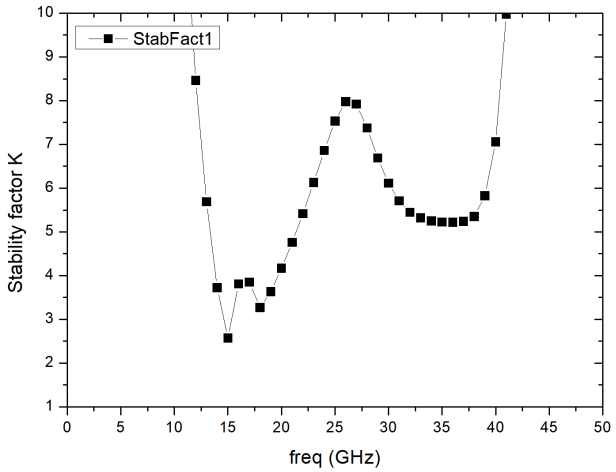



Fig. 7. Stability factor

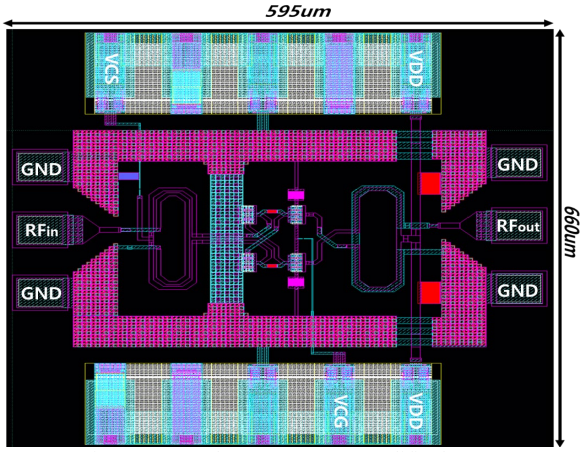



Fig. 8. Proposed CMOS Power Amplifier layout

TABLE 5. Performance comparison with 28GHz CMOS PA with linearization

| | [14] | [15] | **This Work (Simulated)** |
|---|---|---|---|
| Freq (GHz) | 28 | 28 | 28 |
| Linear Power (dBm) | 11 | 7.5 | 12.3 |
| Peak PAE(%) | 43.3 | 27.3 | 41.8 |
| Gain (dB) | 13.6 | 18 | 12.4 |
| # of stage | 1 | 2 | 1 |
| Linearization | 2fo control | Dual power mode S-PCC | Ribbon cell |
| Area*($mm^2$) | 0.78 | 0.5 | 0.4 |
| Process | CMOS 28nm | CMOS 65nm | CMOS 28nm |

*including pads

## IV. CONCLUSION

This paper proposes a ribbon cell structure to improve the linearity of a CMOS power amplifier operating at 28 GHz. As a result of the simulation, the AM-PM is 0.08 degrees at 10dBm and -0.38 degrees at 12 dBm. The IMD3 results are -40 dBc at 10 dBm and -30 dBc at 12.3 dBm, with PAEs of 19% and 25%, respectively. It has a gain of 11.6 dB, a peak PAE of 41.8%, and a stability factor of more than 1, so it is unconditionally stable.

## ACKNOWLEDGMENT

The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), Korea.

This work was supported by the National Research Foundation of Korea(NRF) grant funded by the Korea government(MSIT)(No. 2022R1G1A1003448)

## REFERENCES

[1] T. Joo, B. Koo, and S. Hong, "A WLAN RF CMOS PA with Large-Signal MGTR Method," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 3, pp. 1272-1279, Mar. 2013.

[2] S. Jang, C. Lee, and C. Park, "Differential 2.4-GHz CMOS Power Amplifier Using an Asymmetric Differential Inductor to Improve Linearity," *Journal of the Korean Institute of Information and Communication Engineering*, vol. 23, no. 6, pp. 726-732, Jun, 2019.

[3] N. Ryu, B. Park, and Y. Jeong, "A fully integrated high efficiency RF power amplifier for WLAN application in 40 nm standard CMOS process," *IEEE Micowave and Wireless Components Letters*, vol. 25, no. 6, pp. 382-384, Jun. 2015.

[4] H, Ahn et al., "A Fully Integrated Dual-Mode CMOS Power Amplifier With an Autotransformer-Based Parallel Combining Transformer," *IEEE Micowave and Wireless Components Letters*, vol. 27, no. 9, pp. 833-835, Sep. 2017.

[5] T. Joo, B. Koo, and S. Hong, "A WLAN RF CMOS PA with adaptive power cells," in *Proc. IEEE RFIC Symp.,* Seattle, WA, USA, 2013, pp. 345-348.

[6] C. Fager et al., "A comprehensive analysis of IMD behavior in RF CMOS power amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 1, pp. 24-34, Jan. 2004.

[7] Oh, Juntaek, Bonhyun Ku, and Songcheol Hong. "A 77-GHz CMOS power amplifier with a parallel power combiner based on transmission-line transform er." *IEEE Transactions on Microwave Theory and Techniques* 61.7 (2013): 2662-2669.

[8] Park, Jinseok, Seunghoon Kang, and Songcheol Hong. "Design of a Ka-band cascode power amplifier linearized with cold-FET interstage matching network." *IEEE Transactions on Microwave Theory and Techniques* 69.2 (2020): 1429-1438.

[9] L. C. Nunes, P. M. Cabral, and J. C. Pedro, "AM/AM and AM/PM distortion generation mechanisms in Si LDMOS and GaN HEMT based RF power amplifiers,"

*IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 4, pp. 799-809, Apr. 2014.

[10] J. P. Aiko and T. Rahkonen, "A comprehensive analysis of AM-AM and AM-PM conversion in an LDMOS RF power amplifier," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 2, pp. 262-270, Feb. 2009.

[11] Lee, Seungchan, Jinseok Park, and Songcheol Hong. "A Ka-band phase-compensated variable-gain CMOS low-noise amplifier." *IEEE Microwave and Wireless Components Letters* 29.2 (2019): 131-133.

[12] S. Jin et al., "Enhanced linearity of CMOS power amplifier using adaptive common gate bias control," in *Proc. MTT-S Int. Microw. Symp. Dig*., Seattle, WA, USA, Jun. 2013, pp. 1-4.

[13] H. Song and R. Gharpurey, "Digitally intensive transmitter employing RF pulse width modulation ofr IoT applications," in *Proc. IEEE RFIC Symp*., Phoenix, AZ, USA, 2015, pp. 151-154.

[14] B. Park et al., "Highly linear mm-wave CMOS power amplifier," IEEE Trans. *Microwave Theory and Techniques*, vol. 64, no. 12, pp. 4535–4544, Dec. 2016.

[15] S, Lee Seunghoon Kang, and Songcheol Hong. "A 28-GHz CMOS linear power amplifier with low output phase variation over dual power modes." IEEE Microwave and Wireless Components Letters 29.8 (2019): 551-553.

[16] WANG, Chengzhou; VAIDYANATHAN, Mani; LARSON, Lawrence E. "A capacitance-compensation technique for improved linearity in CMOS class-AB power amplifiers" IEEE journal of solid-state circuits, 39.11: 1927-1937, 2004.

[17] S. Shakib, M. Elkholy, J. Dunworth, V. Aparin, and K. Entesari, "2.7 A wideband 28GHz power amplifier supporting 8×100MHz carrier aggregation for 5G in 40nm CMOS," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, pp. 44–45. Feb. 2017.

[18] W. Lee, j, Yoo and S, Hong. "A 28-GHz CMOS power amplifier linearized by dynamic conductance control and body carrier injection" IEEE Microwave and Wireless Components Letters, 31.9: 1071-1074. 2021.

[19] S. N. Ali, P. Agarwal, S. Gopal, and D. Heo, "Transformer-based predistortion linearizer for high linearity and high modulation efficiency in mm-Wave 5G CMOS power amplifiers," IEEE Trans. Microw. Theory Techn., vol. 67, no. 7, pp. 3074–3087, 2019.

[20] Jeong, Gwanghyeon, Taehwan Joo, and Songcheol Hong. "A highly linear and efficient CMOS power amplifier with cascode–cascade configuration." *IEEE Microwave and Wireless Components Letters* 27.6 (2017): 596-598.

[21] G. Cho, G. Jeong, and S. Hong, "28-GHz CMOS power amplifier linearized with resistive drain-body connection," IEEE Microw. Wireless Compon. Lett., vol. 30, no. 9, pp. 876–879, 2020.

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