An Ultra Low-Power Low-Noise Neural Signal Acquisition Amplifier for ECoG Applications

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***Abstract* – An ultra low-power, low-noise neural recording amplifier for electrocorticography (ECoG) applications is presented. The proposed AC-coupled capacitive-feedback neural amplifier employing a gain-boosted inverter-stacked operational transconductance amplifier with floating-body technique achieves an enhanced input noise performance despite consuming limited power. The designed amplifier IC achieves a closed-loop gain of 40 dB, integrated input-referred noise of 6.3 μVrms within 520 Hz bandwidth while dissipating 15.5 nW of power at 1-V supply voltage. The IC is implemented using 65-nm CMOS process and occupies 0.051 mm² of die area.**

***Keywords*—neural recording amplifier, floating-body, gain-boosting, inverter-stacked OTA, ECoG**

I. INTRODUCTION

Multi-channel neural signal recording systems in brain-machine-interfaces can be used to diagnose and analyze various neurological disorders, with the ultimate goal of improving the understanding of the brain and its highly complex functions [1]-[9].

The recorded neural signals of interest include action potential (AP)/spike, local field potential (LFP), electroencephalogram (EEG), and electrocorticography (ECoG). Among these signals and acquisition methods, ECoG has emerged as an attractive approach and solution to neurological activity recording because it offers better resolution than EEG, and is less invasive than AP/LFP recording [9]. The ECoG signal is the electrical activity of cerebral cortex recorded by attaching flat electrodes directly on the exposed brain surface. It is the sum of the electrical activity of a large number of neurons of about 100-10000 observed and has an amplitude of several hundred μV to several mV in the 1-300 Hz frequency band. Thus, the ECoG signal recording front-end IC requires less operation power in comparison to spike recording due to its narrow signal bandwidth and can acquire neural signals without motion artifacts caused by the patient's movement.

One of the most important blocks in a neural recording system is the neural signal acquisition amplifier, which is usually the first analog signal processing block after the multi-electrode array (MEA). In order to incorporate multi-channel operation, ultra-low-power operation is required in the individual building block to avoid potential damage to the nerve tissue from heat flux due to the excessive power dissipation of the IC. In addition, to accurately record weak neural signals with sufficient signal to noise ratio, a high gain amplification with low input-referred noise performance is critical in the design of the front-end amplifier.

While AC-coupled, capacitive-feedback topologies are widely used as neural amplifiers to block large DC offsets at electrode-tissue interfaces, the core operational transconductance amplifier (OTA) in this closed-loop circuit mostly decides the overall performance of the neural signal amplifier and thus the power-noise tradeoff needs to be carefully addressed in the design process. To achieve good noise performance at low power consumption, many OTA circuit topologies have been presented previously. Topologies such as current-mirror-based OTA [1], folded-cascode [2], [3], complementary current-reuse [4], [5], and inverter-stacking [6] have been proposed in designing the first stage OTA. Current-mirror-based OTA has the advantage of achieving a large output swing with relatively simple design process, but is known to be less power efficient. Folded-cascode architecture is a well-established circuit topology which has a large input-range, but its power efficiency is not as good as the current-reuse OTA. The current-reuse OTA with PMOS and NMOS input pair offer a good balanced performance in key performance parameters but inverter-stacked architecture achieves superior power-noise tradeoff performance, while sacrificing output voltage swing due to the stacks.

In this paper, an AC-coupled, capacitive-feedback neural recording amplifier which employs a power-efficient OTA with improved noise performance is presented for ECoG applications. The OTA is based on a gain-boosted inverter-stacked architecture with floating-body input transistors for enhanced transconductance and power efficiency. Although chopper stabilization is a widely-used technique to up-modulate the low-frequency flicker noise, it greatly increases the complexity of the overall circuit and thus is not employed in this design. Section II discusses the circuit design details of the proposed amplifier. Section III presents the experimental results and the conclusions are given in Section IV.

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Manuscript Received Aug. 11, 2023, Revised Aug. 31, 2023, Accepted Sep. 1, 2023

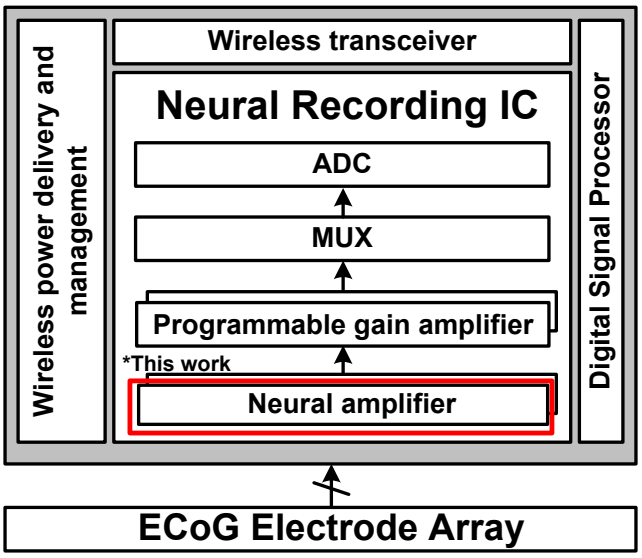

Fig. 1. The block diagram of a general neural recording system-on-chip.

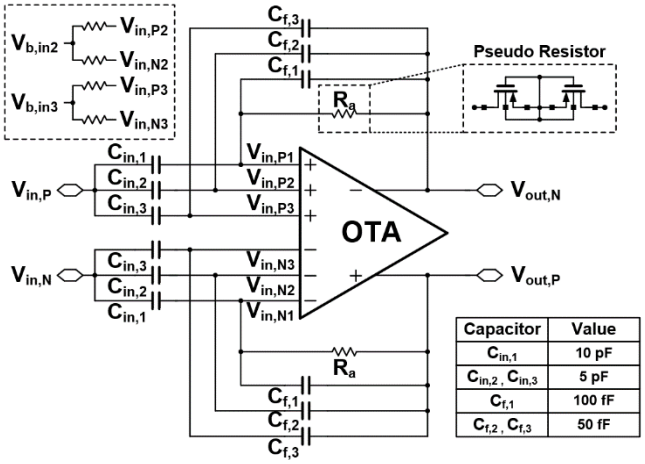

Fig. 2. The circuit schematic of proposed LNA.

II. CIRCUIT DESIGN

The block diagram of a general neural recording IC architecture for recording and processing of neural signals is shown in Fig. 1. The IC is comprised of a neural amplifier as the first stage which is the dominant block that decides the overall noise performance of the recording system. The neural amplifier block usually provides a large fixed gain to boost the weak neural signal at the MEA interface. A programmable gain amplifier (PGA) with tunable gain and filtering functions follows the neural amplifier which enables the AFE to process neural signals with various amplitudes. An analog multiplexer (MUX) block follows the PGA to reduce the number of dedicated analog-to-digital converters (ADC) for power and area reduction. Finally, the ADC is used to digitize the recorded signal for further digital processing and wireless transmission to an external device. This work only includes the single-channel neural recording amplifier.

Fig. 2 shows the closed-loop schematic of the proposed low-noise neural amplifier. As the core OTA has total three

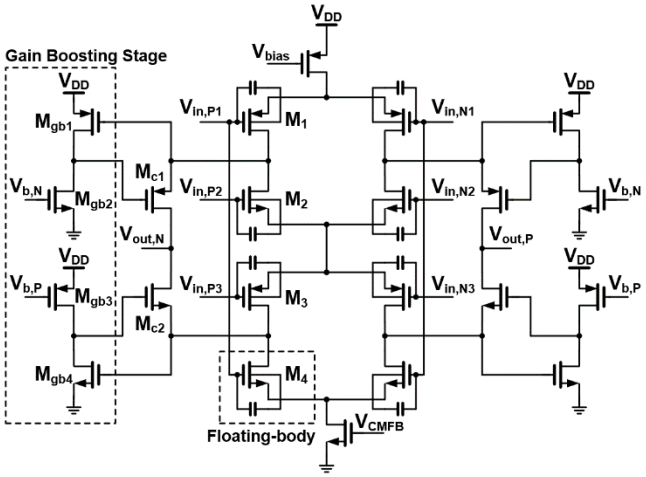

Fig. 3. The core circuit schematic of proposed OTA.

TABLE I. Transistor size of the OTA.

Transistor	Width/Length (μm/μm)
M1	60/3.5
M2	20/10
M3	50/4
M4	22.5/9
Mgb1	2.4/1
Mgb2	0.58/5
Mgb3	2.6/1
Mgb4	0.58/5
Mc1	10/3
Mc2	2/5

pairs of input nodes (M_1+M_4, M_2, M_3 in Fig.3), three pairs of split capacitive feedback loops are used. The closed-loop voltage gain of neural amplifier is set to be at 40 dB, which is determined by the ratio of the total input capacitor C_{in} and the feedback capacitor C_f. The input referred noise of the neural amplifier with capacitive feedback is expressed as;

$$\overline{v_{n,cl}^2} = \left(\frac{C_{in} + C_f + C_p}{C_{in}}\right) \cdot \overline{v_{n,ol}^2} \qquad (1)$$

where C_P is the gate parasitic capacitance of the input transistor and $\overline{v_{n,ol}^2}$ is the input referred noise of the core OTA. Since the capacitors C_{in1} and C_{f1} are connected to two pairs of input transistors M_1 and M_4, the contribution of the parasitic capacitance of the input transistor in the feedback loop is twice of other feedback loops. Therefore, considering the noise contribution from the input transistor parasitic capacitance, the size of capacitors C_{in1} and C_{f1} is set to be twice the value of other capacitors. The values of each capacitors used for the closed-loop feedback are also shown in Fig. 2.

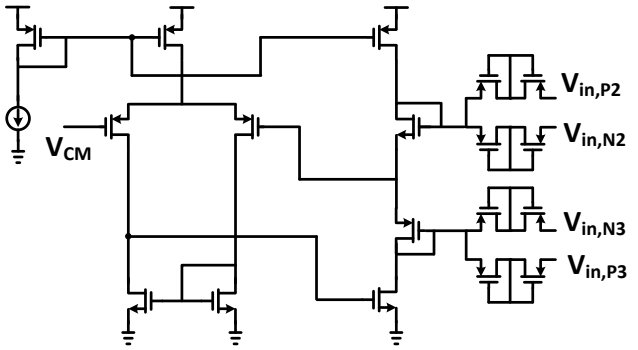

Fig. 4. The circuit schematic of replica-based bias circuit for the core OTA.

Fig. 3 shows the schematic of proposed core OTA circuit. To maximize the transconductance of the input pairs under limited power, the transistors are sized with large W/L ratios and biased in subthreshold. The OTA is designed based on the inverter-stacking scheme proposed in [6]. In this scheme, four pairs of input transistors are stacked and the bias current is four times reused, thus greatly improving the power efficiency of the circuit. The input transconductance is thus boosted by four times with the same current consumption, and can achieve low noise floor and wide bandwidth. The total transconductance Gm of the inverter-stacked OTA is expressed as the following equation;

$$G_m = (g_{m1} + g_{m2} + g_{m3} + g_{m4}) \approx 4g_{m,in} \qquad (2)$$

where g_{mi} is transconductance of input transistor M_i. To further increase the Gm of OTA, the body terminal of all input transistors are AC-coupled to the gate terminal through the capacitor and are DC-floated [8]. Because the body terminal is AC-coupled to the gate terminal, the small-signal voltage of body terminal can swing along the gate voltage through the body to gate capacitance. Thus, by using the floating body technique, the equivalent G_m of OTA increases as;

$$G_m \approx 4g_{m,in} + 4g_{mb,in} \qquad (3)$$

where $g_{mb,in}$ is the body transconductance of input transistor. By using the g_{mb} of input transistor, the equivalent G_m of OTA increases, and the resulting simulated bandwidth is improved by 35% while the input referred noise performances is improved by over 10% at equal power consumption. For the AC-coupling capacitors between the gate and the body terminal, metal-oxide-metal (MOM) capacitor is used. The size of added MOM capacitor is determined by trade-off between active area and OTA performances. In this design, a 250 fF capacitor is used for each input transistor.

In order to obtain a sufficiently large open-loop gain using deep sub-micron process, gain boosting technique is applied to the inverter-stacked architecture. At the gain boosting stage, a common source stage with an active current source load was used for simple circuit configuration. The sizes of the transistors used in the OTA core is presented in Table I.

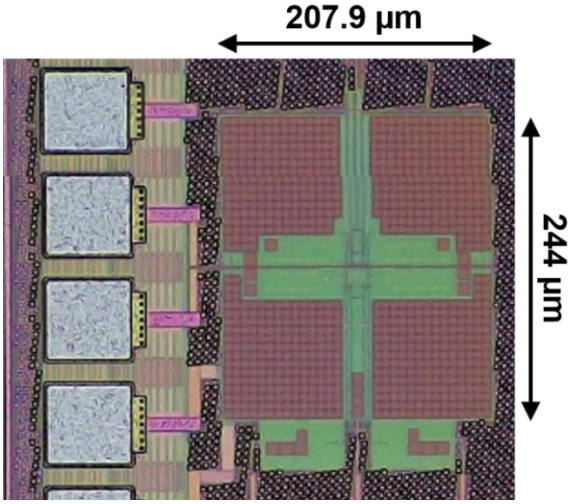

Fig. 5. The chip micrograph of proposed neural amplifier.

The overall input-referred noise of the proposed OTA is expressed as;

$$\overline{v_n^2} = \overline{v_{n,th}^2} + \overline{v_{n,1/f}^2} = \frac{8kT\gamma}{G_m} + \left(\frac{K_f}{C_{ox}4WL} \cdot \frac{1}{f}\right) \qquad (4)$$

where $\overline{v_{n,th}^2}$ and $\overline{v_{n,1/f}^2}$ are the thermal noise and 1/f noise, respectively. T is temperature, k is Boltzmann's constant, K_f is a process-dependent parameter, and γ is excess noise constant. By using the floating-body technique, the equivalent G_m of OTA is increased, and the thermal noise of OTA is reduced. Since the noise contribution from the input transistors dominates the entire noise floor, the noise contribution of cascode and gain boosting devices is ignored.

For the gate bias of the input core transistors in the middle part of the stack (M_2, M_3), a replica-based bias branch shown in Fig. 4, is used to generate accurate voltages to ensure robust operation despite process, voltage, temperature (PVT) variation. For the common-mode feedback (CMFB) circuit, a resistor-averaged topology is utilized to stabilize the common-mode voltages.

III. RESULTS AND DISCUSSIONS

The proposed neural amplifier is designed and fabricated using 65-nm CMOS process. An on-chip unity-gain buffer is included for testing. The IC is assembled using chip-on-board packaging and measured on a FR4 printed-circuit-board. Fig. 5 shows the micrograph of the fabricated chip and the active area is 0.051 mm².

Fig. 6 shows the measured frequency response of the neural amplifier. The amplifier has 40 dB of mid-band voltage gain, with 0.3 Hz of high-pass cutoff frequency and 520 Hz of low-pass cutoff frequency. The -3 dB bandwidth of LNA is sufficient to cover the bandwidth of the ECoG signal.

Fig. 7 shows the input-referred noise spectrum. The integrated input-referred noise within the -3 dB bandwidth is about 6.3 μVrms, and the input-referred noise within the 1 Hz to 300 Hz ECoG signal band is 5.1 μVrms.

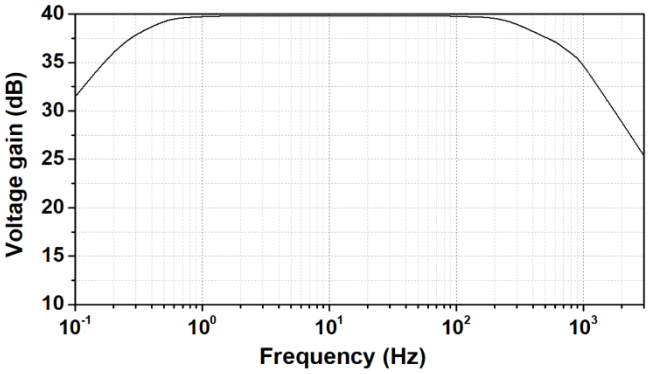

Fig. 6. Measured closed-loop gain response.

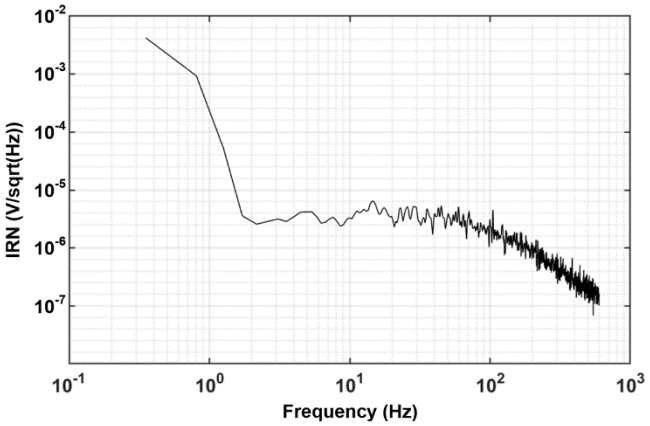

Fig. 7. Measured input-referred noise response.

TABLE II. Performance summary of the designed neural amplifier.

Parameter	This work	[11]	[12]	[13]
Supply (V)	1	2.5	1	0.6
Gain (dB)	40	-	40	36.9
BW (Hz)	520	1k	150	250
Input referred noise (μVrms)	6.3	2.78	112 nV/ sqrt(Hz)	6.52
Power (nW)	15.5*	2.98μ	1.08μ	28
Noise efficiency factor	1.33**	2.35	-	2.64
Power efficiency factor	1.77**	13.8	-	4.18
CMRR (dB)	>80*	76	82	55
PSRR (dB)	>80*	82	68	67
Area (mm^2)	0.051	0.0023	0.085	-
Process (nm)	65	65	65	65
Application	ECoG	ECoG	ECoG	ECG

*Simulated value, **Calculated with simulated power consumption

Table II shows the measured performance summary and compares with other neural recording amplifiers operating at low frequency bands, implemented using similar process technologies. The noise efficiency factor (NEF) and power efficiency factor (PEF) [1] parameters are used to compare the neural signal recording amplifier noise-power trade-off performance. The total current consumption of the proposed LNA is 15.5 nA, achieving 1.33 and 1.77 of NEF and PEF, respectively. In comparison to similar works, the proposed neural amplifier achieves enhanced noise-to-power trade-off performances.

IV. CONCLUSION

The ultra low-power gain-boosted inverter-stacked OTA with floating-body is proposed for improved input-referred noise performance. The designed closed-loop neural signal acquisition amplifier employing the proposed OTA achieves 40 dB of voltage gain, 6.3 μVrms of input referred noise, and 520 Hz of -3 dB bandwidth while consuming 15.5 nW of power consumption at 1-V supply. The amplifier is implemented using 65 nm CMOS process and occupies 0.051 mm^2 of die area.

ACKNOWLEDGEMENT

This research was funded by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Science and ICT (MSIT), (NRF-2018R1C1B6003088). The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC).

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