A Low-jitter Ring-DCO-Based Digital PLL Using P/I-Gain Co-Optimization and Optimally Spaced TDC for Flicker-Noise Reduction

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***Abstract* – This work presents a low-jitter ring-oscillator-based digital PLL (RO-DPLL). To achieve low jitter, the proposed RO-DPLL used calibration techniques to optimize the gain of the Proportional-path (*P*-path) and Integral-path (*I*-path) in the digital-loop-filter (DLF) simultaneously. Since the effect of flicker noise increases as the frequency increases, the frequency drift of the RO-DPLL becomes more severe in the operation of the RO-DPLL. Thus, it is critical to calibrate the gain of the *I*-path to an optimal value because *I*-path of DLF compensates for the frequency error of the PLL. Moreover, the optimally-spaced time-to-digital-converter (OS-TDC) with the threshold calibrator provides sufficient information, supporting the efficient operation of the calibrators. Due to the use of the *P*/*I*-path co-optimization (PICO) and OS-TDC with calibrator, the proposed RO-DPLL achieved the rms jitter of 343 fs and the reference spur of –65dBc. And, its $FoM_{jitter,N}$ was –258.5 dBc, comparable to the state-of-the-art RO-based analog PLLs.**

***Keywords* — Ring digitally-controlled oscillator (RDCO), digital phase-locked-loop (DPLL), time-to-digital converter (TDC), proportional-path, integral-path, digital-loop filter (DLF), rms jitter, flicker noise, thermal noise**

I. INTRODUCTION

To meet the stringent specification of advanced applications, moderns SoCs are integrating lots of PLLs into a single silicon chip. In the case of 5G transceivers, they need multiple PLLs for the implementation of the complex scheme such as carrier aggregation, and multiple-input and multiple-output (MIMO). As the data rate increases, a greater number of the PLLs are required, resulting in a significant silicon area. Moreover, due to the harsh jitter specification of the advanced applications, a low-jitter *LC*-oscillator-based charge-pump PLL (CPPLL) is treated as the sole option for the clock generator even though they are area-hungry options. Fig. 1(a) shows a general architecture of the *LC*-oscillator-based CPPLL. Since this architecture includes lots of passive components in its analog loop filter and *LC* oscillator, thus it is necessary to secure a large silicon area.

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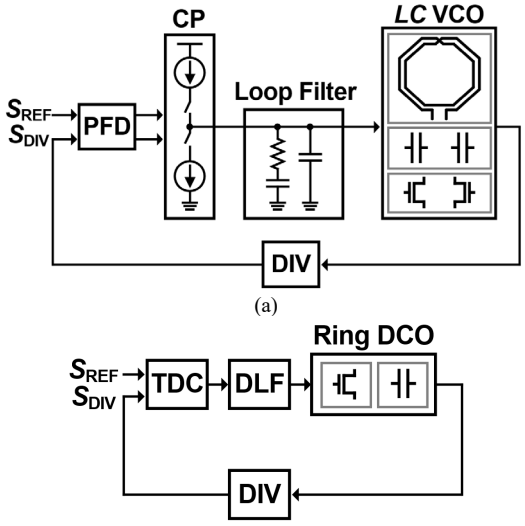


Fig. 1. Basic architecture of (a) *LC*-oscillator-based analog PLL and (b) ring-oscillator-based digital PLL.

To overcome this problem, ring-oscillator-based digital PLLs (RO-DPLLs) with jitter reduction techniques are recently emerging as alternatives. Fig. 1(b) shows a basic architecture of the RO-DPLL, which uses fewer passive components compared to its *LC*-oscillator- based counterparts. The ring oscillators (ROs) have another advantage such that they can be scaled down to new CMOS technology nodes, unlike *LC*-oscillator. Despite such merits of the RO, the reason why it cannot easily replace *LC*-PLLs is its poor phase noise. The Figure-of-merit (FoM) of typical ROs is much worse than that of *LC*-oscillators, by more than about 20 dB. Fig. 2 shows a simple block diagram of the oscillator containing two major noise sources, i.e., the thermal noise, $\tau_{n,Therm}$, and the flicker noise, $\tau_{n,Flick}$. The sum of these two noises, $\tau_{n,DCO}$, is accumulated per the period of the oscillator. As shown in Fig. 2, the phase noise of $\tau_{n,DCO}$ reveals that the energy of $\tau_{n,Flick}$, is concentrated at low-frequency offsets near DC, while the noise component of $\tau_{n,Therm}$ has the same magnitude at frequencies from low to high. The frequency when the level on the phase noise of the $\tau_{n,Therm}$, and the $\tau_{n,Flick}$ are the same is called the flicker corner frequency, f_c, and it can represent the noise performance of the oscillator. The smaller f_c is, the better FoM the oscillator has. Fig. 3 shows the f_c of the 3-stage ring oscillator across output frequency on the same power condition (P_{DC} = 3.8

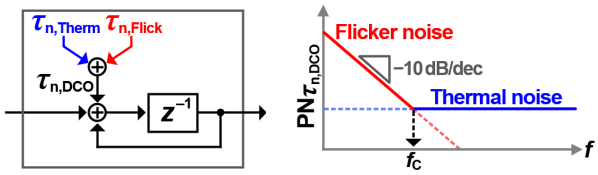


Fig. 2. Simple block diagram and phase noise of oscillator.

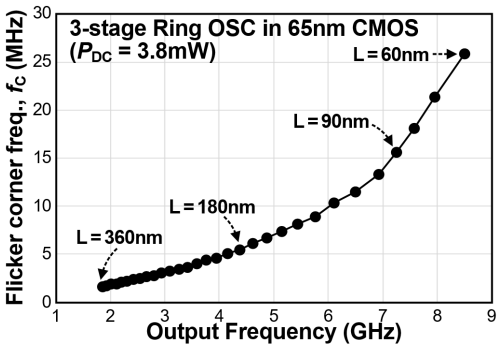


Fig. 3. Flicker corner frequency of 3-stage ring oscillator across output.

mW). To increase the output frequency of ring oscillators, the transistor length of unit delay cells must be minimized. However, as shown in this simulation graph, the reduction in the transistor length inevitably increases f_c and this effect is more significant as the length is further reduced.

In this paper, we propose a low-jitter RO-DPLL with special calibrators that can remove the flicker noise of the ring digitally-controlled-oscillator (RDCO) as well as thermal noise [1]. Noted that the noise sources with the flicker noise contribute to not just the momentary phase shift but the permanent frequency drift of the oscillator, we proposed a new calibration method to optimize the frequency tuning in the operation of the PLL. The proposed RO-DPLL controls both the gain of proportional-path (P-path) and integral-path (I-path) in the digital loop filter (DLF), with two individual LMS-based calibration logics to settle gains at the optimal point, while the conventional calibration method considers only the component of the thermal noise and thus the gain of P-path. Since the gain of I-path is responsible for the decision of the magnitude of the frequency tuning, the proposed calibration technique dramatically reduces the thermal noise and flicker noise simultaneously. In addition, the use of the optimally spaced TDC (OS-TDC) provides more information on timing errors for removing flicker noise [1]. All spacings between the thresholds of the TDC, τ_{TH}s, are optimized in the background using the τ_{TH}-calibrator.

II. PROPOSED RO-DPLL USING CALIBRATOR

A. Conventional RO-DPLL Calibrating Only P-path Gain

To effectively reduce the phase noise of the oscillator and, consequently, overall output jitter in conventional digital PLLs, various phase-noise minimization techniques have been presented [2, 3, 4]. One popular method is to adjust the *P*-path gain of the loop, K_P, to the optimal value, $K_{P,OPT}$, where the rms jitter is minimum [5, 6]. Fig. 4 (a) illustrates the conventional architecture of a DPLL using a calibrator of

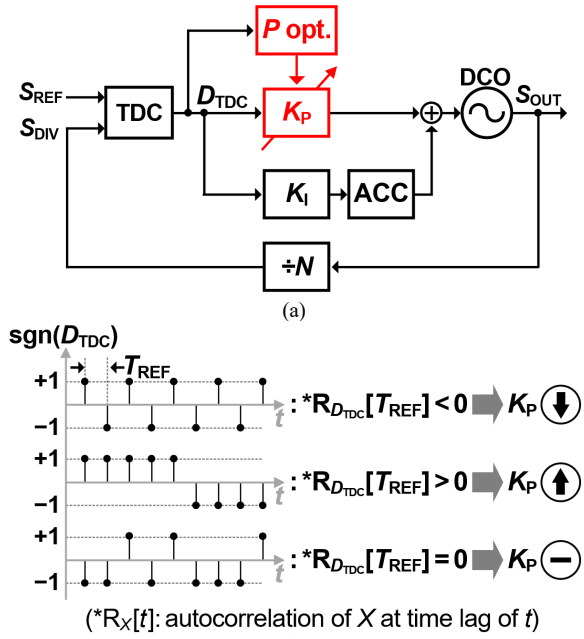


Fig. 4. (a) Conventional architecture of DPLL with only *P*-path optimization (b) detailed implementation concept of the calibration.

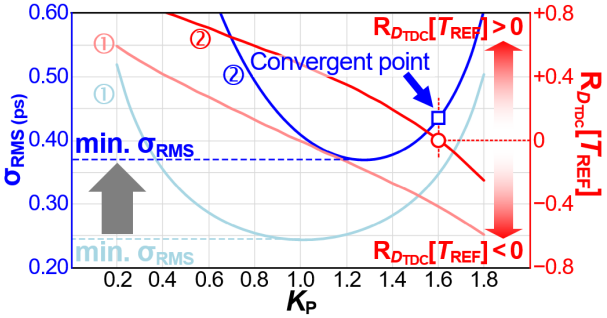


Fig. 5. RMS jitter according to K_P with 2 different f_c when assuming the oscillator with 8GHz of output frequency, –133dBc/Hz@100MHz of phase noise; f_c = 1 kHz for case ① and f_c = 20 MHz for case ②.

K_P. The calibrator, with information from the output of the time-to-digital converter (TDC), D_{TDC}, which indicates which signal is faster between the reference signal, S_{REF}, and the divider signal, S_{DIV}, determines the magnitude of K_P. Fig. 4 (b) shows further details on the implementation concept of the K_P calibrator. The K_P optimization logic utilizes the autocorrelation of the TDC output at the time lag of the reference clock period as a criterion to optimize K_P. Based on the polarity of the autocorrelation, the calibrator decides whether K_P is larger or smaller than $K_{P,OPT}$, and makes adjustment for K_P accordingly. However, this method has a limitation to fully suppress flicker noise due to the low-frequency-concentrated noise components of the flicker noise. Fig. 5 shows the rms jitter of the output signal of the PLL, to investigate impact of the flicker noise on the aforementioned jitter minimization, according to K_P with 2 different flicker corner frequencies, i.e., f_c = 1kHz and f_c = 20 MHz for CASE ① and ②, respectively. As shown in Fig. 3, since the RO can have the f_c more than 10 MHz at 7 GHz of output frequency, so it is reasonable to set the f_c to 20 MHz especially for the design of the RO. In these

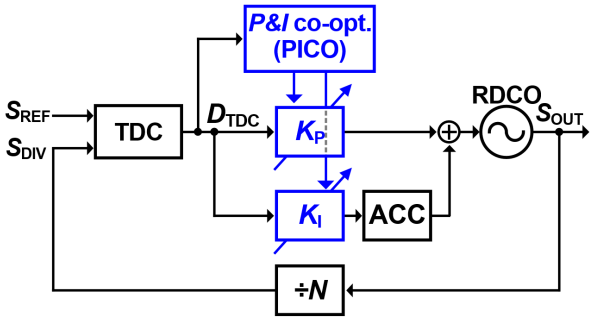


Fig. 6. Architecture of DPLL with the proposed calibration method to co-optimize *P*-/*I*-path gain of the DPLL simultaneously.

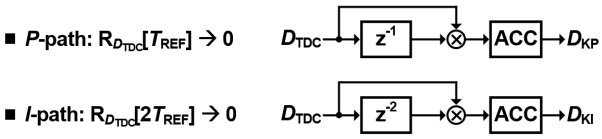


Fig. 7. Implementation of *P*-/*I*-path co-optimization (PICO).

simulations, we used the PLL with 8 GHz of output frequency, 64 of dividing number (N), and 2^{-8} of K_P. The DCO has -133 dBc/Hz at 100MHz in its phase noise. For CASE ①, where the thermal noise dominates the overall jitter of the ring DCO, calibrating K_P such that the autocorrelation is zero results in a settled point of the K_P very close to the minimum jitter point. However, for CASE ②, where the flicker noise contributes significantly to the overall jitter, the simulation result differed in two observations. First, the achievable rms jitter was considerably degraded due to large flicker noise. Second, the large flicker noise invalidated the criterion of the conventional jitter minimization algorithm, causing the convergent point to deviate from the minimum jitter point. This discrepancy occurs because the conventional method considered thermal noise rather than flicker noise. So, this simulation suggests that to minimize the rms jitter of RO-DPLLs, even with a large flicker noise, the jitter minimization algorithm must be revised to be capable of considering flicker noise as well as thermal noise.

B. Proposed RO-DPLL with the P-/I-path Co-optimization (PICO) and Design methodology of the PICO

Since it was well known that most of the energy of flicker noise exists at low-frequency offsets near DC and the flicker noise serves as one of the major reasons for the frequency drift in the PLL [7], the newly designed algorithm should calibrate the *I*-path gain, K_I, to correct frequency drifts differently from conventional methods that only consider the *P*-path optimization. So, in this work, we propose a RO-DPLL using the proportional and integral-gain co-optimization (PICO) technique. Since the proposed PICO can optimize K_I even for a high frequency of the f_c, the overall rms jitter can be reduced to the global minimum value. As a result, the proposed PLL using the PICO can achieve a very low jitter at a very high output frequency while it uses a very small silicon area. Fig. 6 shows the simple architecture of the proposed work with the PICO.

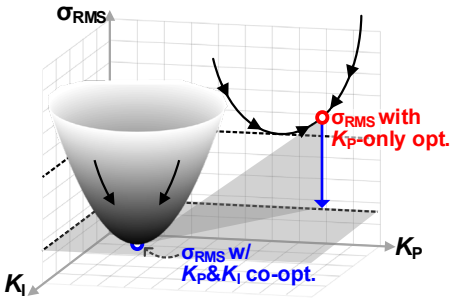


Fig. 8. Jitter minimization due to the use of the PICO at high flicker corner frequency (f_c = 20 MHz).

The optimization of K_P is the same as the aforementioned conventional method. It adjusts K_P such that the timing errors detected in the current period, $\tau_{ERR}[n]$, and the next period, $\tau_{ERR}[n+1]$, have no correlation. In other words, the autocorrelation of τ_{ERR} at T_{REF} becomes zero and it can be expressed as

$$E[\tau_{ERR}[n]\cdot\tau_{ERR}[n+1]] = R\tau_{ERR}[T_{REF}] = 0 \quad (1)$$

In addition, to minimize the flicker noise, the PICO also adjusts K_I such that the flicker-induced frequency drift, f_D, does not affect the timing error of the next cycle, $\tau_{ERR}[n+1]$. It can be satisfied by ensuring the cross-correlation between these two variables to be zero as follows:

$$E[f_D[n]\cdot\tau_{ERR}[n+1]] = 0 \quad (2)$$

Since the $f_D[n]$ is proportional to the difference between consecutive timing errors, it can be simplified as

$$f_D[n] \propto (\tau_{ERR}[n] - \tau_{ERR}[n+1]) \quad (3)$$

Through those previous equations, the $f_D[n]$ of the equation (2) can be replaced with the $\tau_{ERR}[n]$ and $\tau_{ERR}[n+1]$. And the equation (2) can be expressed with the linear superposition of the two autocorrelations of τ_{ERR} as follows:

$$R\tau_{ERR}[T_{REF}] - R\tau_{ERR}[2T_{REF}] = 0 \quad (4)$$

As the first term of the equation (4) becomes zero when K_P is optimized, the condition of K_I optimization can be satisfied by adjusting K_I such that the autocorrelation of τ_{ERR} at $2T_{REF}$ becomes zero. Fig. 7 shows the calibration logic of the PICO consisting of a multiplication between TDC output and its delayed version, and an accumulator. Those accumulators in the calibration logics have different gain to prevent the potential convergence issue of the K_I and K_P. By setting the gains quite differently, they do not interrupt the convergence each other. Moreover, the gains of accumulator are also small enough not to affect to the operation of the main loop of the PLL. The PICO generates the digital code to control the gains for the *P*-path and *I*-path, i.e., D_{KP} and D_{IP}, respectively. Fig. 8 shows the jitter minimization according to the value of the K_P and K_I. Even when the f_c is 20 MHz, the proposed RO-DPLL with PICO significantly reduces overall rms jitter to the global minimum value, which is different from the result of the CASE ② in Fig. 5.

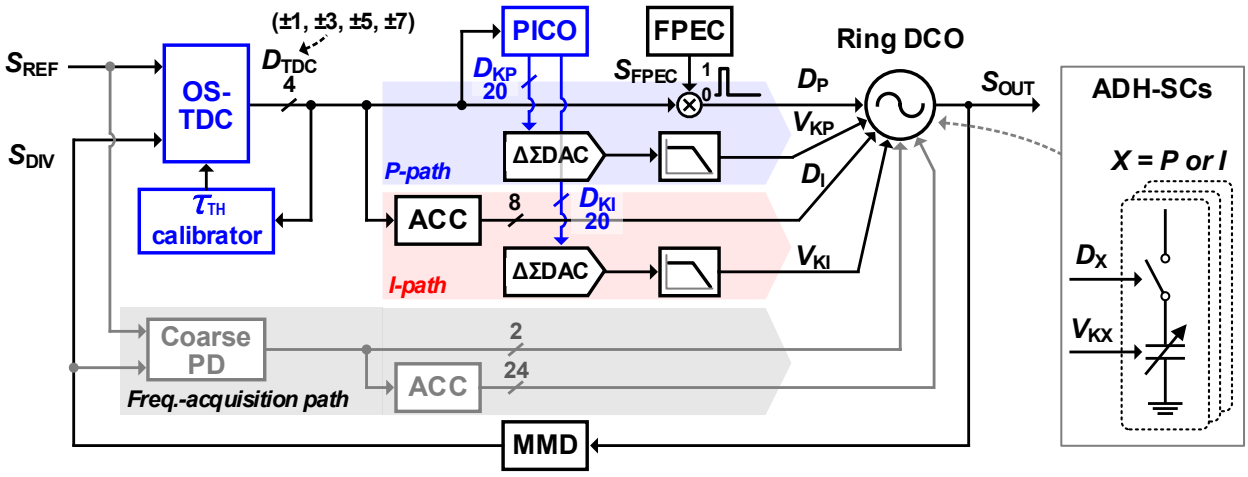


Fig. 9. Overall architecture of the proposed ring-oscillator-based digital PLL with the PICO.

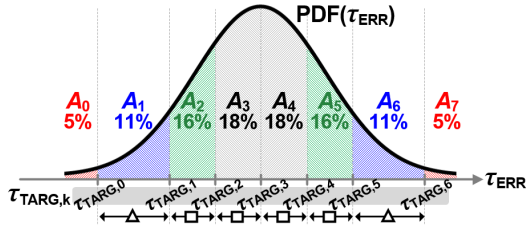


Fig. 10. Optimal thresholds of the TDC to minimize the quantization error of the TDC.

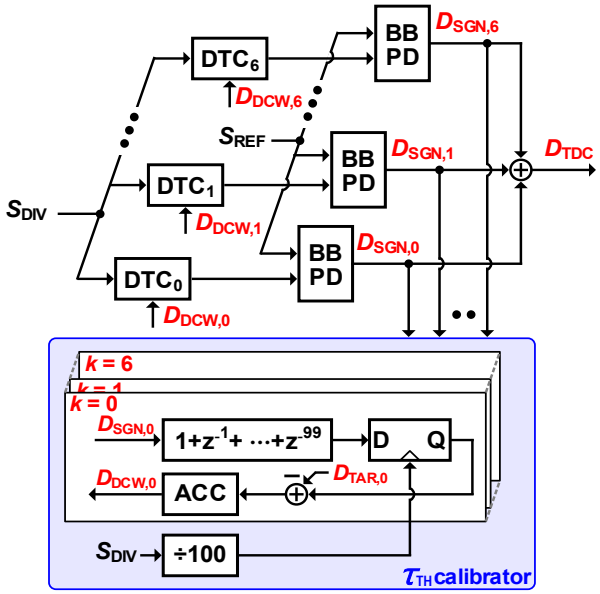
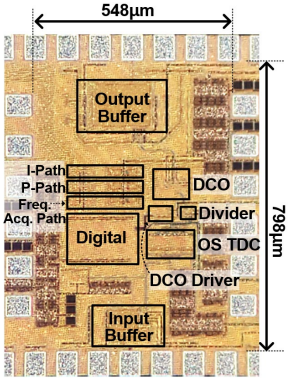


Fig. 11. Implementation of the OS-TDC with the τ_{TH} calibrator.

C. Overall Architecture of the Proposed RO-DPLL and Optimally-spaced Threshold TDC

Fig. 9 shows the overall architecture of the proposed type-II RO-DPLL with the PICO. The 5-stage ring DCO utilized 14 bits and 20 bits cap bank, implemented with analog-digital-hybrid switched capacitors (ADH-SCs), for *P*-path and *I*-path varactors, respectively [8]. The ADH-SC comprise a MOS capacitor and a switch and it helps the digital control code of *P*-path and *I*-path, i.e., D_P and D_I, respectively, to tune accurately the frequency of the ring DCO. As the main ideas to remove the effect of the flicker noise, the proposed architecture includes the PICO and the optimal-spaced TDC (OS-TDC). First, to use the PICO can effectively suppress the flicker noise as well as white thermal noise of the ring DCO. The PICO takes the digital output, D_{TDC}, as input errors to decide the direction of the calibration and generates 20bits-digital-codes to control K_P and K_I, i.e., D_{KP} and D_{KI}, respectively. Those codes enter into each delta-sigma-modulator digital-to-analog converter (ΔΣM-DAC) and its finely calibrated output voltages after passing the low-pass-filter are finally used as the control voltage of the varactors in the ring DCO, i.e., V_{KI} and V_{KP} for *I*-path and the *P*-path, respectively. Second, due to the help of the τ_{TH} calibrator, the OS-TDC with optimal thresholds can provide useful information to calibrate K_P and K_I right and fast. The OS-TDC quantizes a timing error between S_{REF} and S_{DIV} with the division to 7 regions and provides D_{TDC} to the following digital loop filter consisting of the *P*- and *I*- paths. [8, 9] Moreover, the frequency acquisition path serves as a frequency-locking-loop (FLL) to quickly change the initial frequency of the oscillator to the target frequency, and, after the frequency locking, it doesn't work until another frequency jump appears. Along with the frequency acquisition path, the fast phase error correction (FPEC) technique was also implemented in this work. The FPEC technique boosts the *P*-path gain in a very short time, thus resulting in the effect of the fast phase-realignment [10].

Indeed, a TDC with a larger number of thresholds, N_{TDC}, can further reduce the rms jitter since the quantization error becomes smaller. However, too large N_{TDC} would increase area and power significantly without dramatic improvement. Thus, we chose the number of thresholds of the TDC to 7, considering the noise and consumption design resources at the same time. Fig. 10 shows the probability density function (PDF) of the τ_{ERR}. When the thresholds of the TDC, $\tau_{TH,0\text{-}6}$, are optimal as $\tau_{TARG,0\text{-}6}$ at which the quantization error of the TDC is minimum, areas of PDF(τ_{ERR}), $A_{0\text{-}7}$, correspond to 5%, 11%,16%,18%, 18%, 16%, 11%, 5%, respectively. At this point, by comparing the averages of the output BBPDs with the values, all τ_{TH}s can be calibrated such that their average matches the aforementioned percentages. Fig. 11 shows the detailed implementation of the OS-TDC with τ_{TH} calibrator.



(a)

Power Consumption (mW)	
DCO + Driver	4.10
Divider	0.49
Digital Logic + Loop Filter	1.59
OS TDC	0.30
Total	6.48

(b)

Fig. 12. (a) Die photograph (b) Power-breakdown table.

The OS-TDC consists of a total of 7 pairs of the BBPD and the DTC, and compares S_{REF} and the delayed version of the S_{DIV}, generating D_{TDC}. For the τ_{TH} calibrator, it generates 7 different digital codes to control each DTC to have the wanted thresholds where the probability of D_{TDC} is similar to the ideal case in Fig. 10. To estimate the average of the BBPD output, a 100-tap FIR filter was used. By accumulating the difference of the sampled value from the target value, $D_{TAR,0\text{-}6}$, (which is 5, 16, 32, 50, 68, 84 and 95) the $\tau_{TH,0\text{-}6}$ can be adjusted to be optimal. Since the distances between τ_{TH}s are very small in the order of hundreds of femtoseconds, the seven DTCs were designed to be identical. But, we also considered the worst-case local mismatches and we set the dynamic range of the DTC to several picoseconds.

III. MEASUREMENT RESULTS

The proposed RO-DPLL was fabricated in a 65-nm CMOS technology, while occupying 0.075 mm^2 of the silicon area and consuming 6.5mW of the power. Fig. 12(a) shows the die photograph of the proposed work. Fig. 12(b) shows the power breakdown. The ring DCO and its drivers for *P*-path and *I*-path consumed 4.10 mW. Moreover, the power consumption of the divider, digital logic, and OS-TDC was 0.49, 1.59, and 0.3 mW, respectively. Fig. 13 shows the measured phase noise of the 7.68-GHz output signal (f_{REF} = 120 MHz, N = 64). Since the transistor length of the ring DCO's delay cells were designed the minimum to maximize the output frequency, the flicker corner was very high as 19 MHz. Since a wide loop bandwidth due to the FPEC suppressed the free-running phase noise of the ring DCO greatly, the K_P-only optimization was able to suppress the rms jitter considerably. Then, when the PICO was fully turned on to calibrate both K_P and K_I, since it can suppress the flicker noise significantly, 100-kHz phase noise and rms jitter were dramatically reduced to –115.0dBc/Hz and 373fs. Fig. 14 shows another measured phase noise at other frequency of 7.872 GHz (f_{REF} = 123 MHz, N = 64). When the PICO was turned on, the rms jitter of the proposed work achieved 364 fs of. Fig. 15 shows the measured spectrum at the 7.68 GHz output signal with f_{REF} and N are 120MHz and 64, respectively. The reference spur level was –65 dBc.

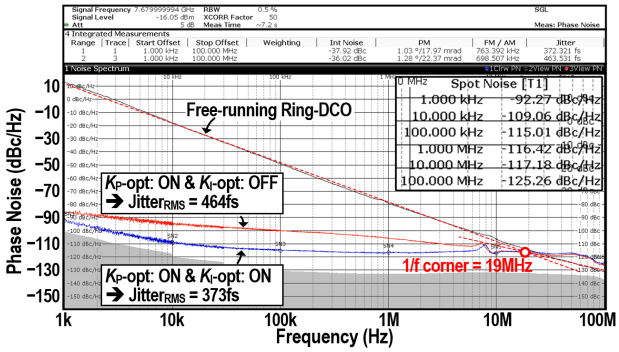


Fig. 13. Measured phase noise of 7.68 GHz output signal when f_{REF} and N are 120 MHz and 64, respectively.

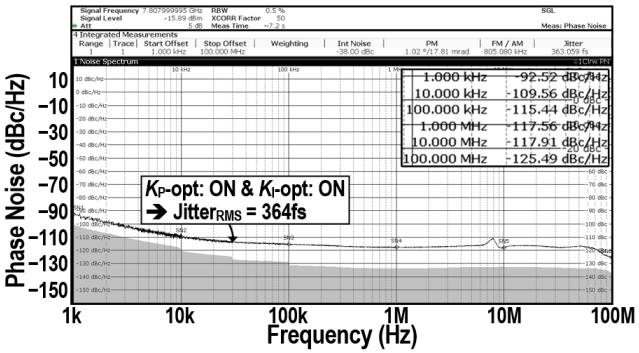


Fig. 14. Measured phase noise of 7.872 GHz output signal when f_{REF} and N are 123 MHz and 64, respectively.

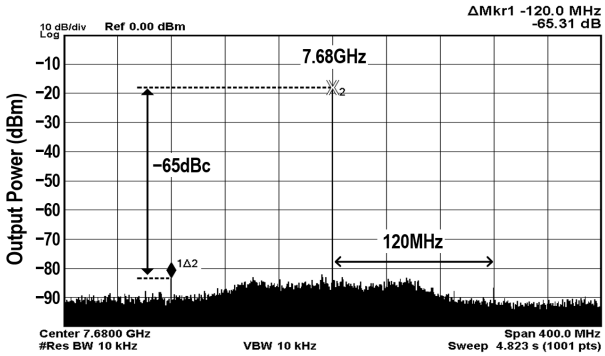


Fig. 15. Measured spectrum with 7.68 GHz output signal (f_{REF} = 120MHz and N = 64).

IV. CONCLUSION

In this paper, we proposed the low-jitter RO-DPLL with the PICO and OS-TDC with the τ_{TH}-calibrator. Due to the suppression of both the flicker noise and the thermal noise by the PICO and the OS-TDC, the rms jitter and the reference spur of the proposed RO-DPLL was reduced to 373 fs$_{rms}$ and –65 dBc, respectively. Overcoming the highest flicker noise corner at the highest output frequency, this work achieved a very low –240.5 dB of the FoM$_{jitter}$. Moreover, despite the high output frequency and multiplication factor, this work has the excellent performances of FoM$_{jitter,N}$, i.e., –258.5 dBc, comparable to the state-of-the-art ring-oscillator analog PLLs.

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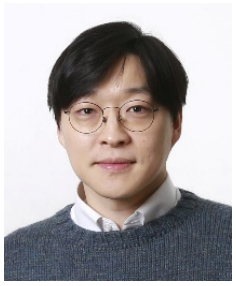

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